A Regulator-Free 84dB DR Audio-Band ADC for Compact Digital Microphones

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Abstract — **A 20kHz audio-band ADC with a single power-supply pad is implemented for a digital electret microphone. The designed low-noise preamplifier not only relaxes the ADC design requirement but also provides an excellent interface for the electret capacitor. A low power 4th-order switched-capacitor (SC) ΣΔ modulator (ΣΔM) converts the analog signal into 1b digital. Under the single power-supply pad, the switching noise effect on the signal quality is estimated via post simulations with simplified parasitic models. Performance degradation is minimized by time-domain noise isolation (TDNI) with sufficient time-spacing between the sampling edge and the output transition. A prototype ADC was implemented in a 0.18 µm CMOS process. It operates under a minimum supply voltage of 1.6 V with total current of 420 µA. Operating at 2.56 MHz clock frequency, it achieves 84 dB dynamic range and a 64 dB peak signal-to-(noise + distortion) ratio. The measured power supply rejection at a 100 mV_{pp} 217 Hz square wave is -72 dB without any supply regulation.**

I. Introduction

Electret capacitor microphones (ECM) are currently being widely used in various applications from low-end toys to high performance multimedia equipment. Traditional JFET-based analog ECMs [1] have long been popular owing to their compactness and low cost. However, the performance limitations of analog ECMs, such as poor power supply rejection (PSR) and low immunity to external on-board noise, are troublesome in today's many high-end applications. Such problems can be alleviated by moving the A/D converter from the external CODEC into the microphone canister [2, 3] and, thus, by sending the A/D converted digital signal through the board. This type of microphone is referred to as a *digital microphone*.

For the development of ADCs for digital microphones several design challenges must be confronted. One critical requirement is that the ADC must be compact so as to be integrated in a microphone canister, the diameter of which is as small as 4mm in recent products. This requirement forces designers to reduce the number of I/O pads and to remove external components such as capacitors for DC blocking or power supply regulation. Minimizing the number of pads without external capacitors is a challenging constraint in a mixed-signal design, because analog and digital circuits might need to share an unregulated power supply and ground. Under this condition, the switching noise from digital components can seriously degrade the analog signal quality.

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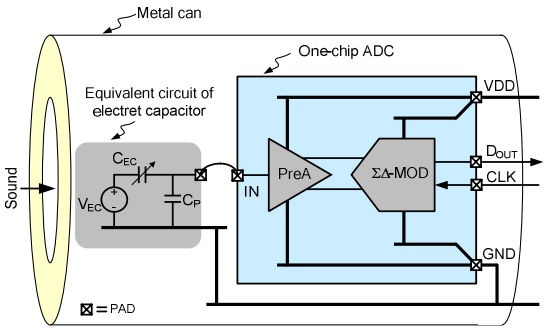

Figure 1. Architecture of a digital microphone

In the present work, a compact high performance one-chip audio-band ADC is implemented for digital microphones.

II. Architecture and Circuit Implementation

Figure 1 shows the digital ECM architecture designed in this work. The prototype consists of a low noise preamplifier (PreA) and a fourth-order switched-capacitor (SC) sigma-delta modulator (ΣΔM). The prototype ADC has only five I/O pins for chip compactness: signal input, clock input, 1b digital output, power supply (VDD), and ground (GND). Note that the PreA and ΣΔM share common VDD and GND pads without any regulators or external components.

For low power 20 kHz full audio bandwidth, which is twice that of [3], careful noise design is essential, including a low noise preamplifier, a power efficient higher order ΣΔM, and estimation and reduction of switching noise coupling.

A. Preamplifier and ΣΔ Modulator

This work utilizes a gm-opamp-RC configured preamplifier [4], as shown in Fig. 2. The front-end transconductor (G_1) takes the voltage signal from the electret capacitor (EC), utilizing its high input impedance, and converts the signal into current, which is then converted again into voltage by the following trans-impedance amplifier. The feedback capacitor (C_1) cuts off high frequency noise.

A folded-cascode transconductance amplifier is designed for G_1 with a PMOS input pair to deal with the signal below ground level. Source degeneration resistors (R_S) are inserted in the input pair to extend the linear input range. Thus, the transconductance of G_1 is

$$G_m = 1/\left(R_S + 1/g_{m1,2}\right) \quad (1)$$

where $g_{m1,2}$ is the transconductance of M_1/M_2.

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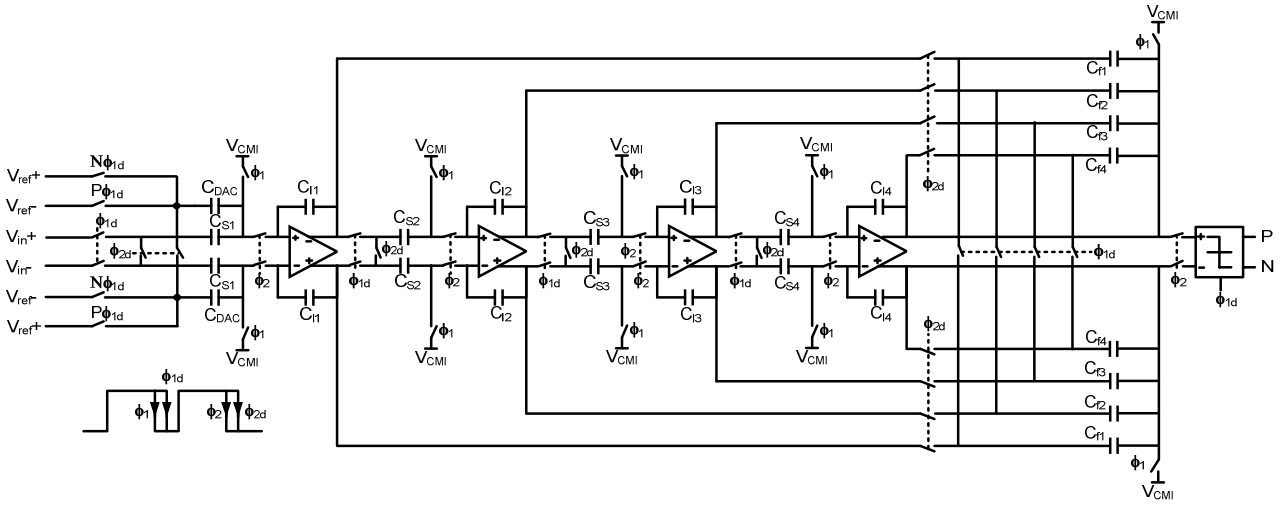

Figure 3. Schematic of 4th-order ΣΔM

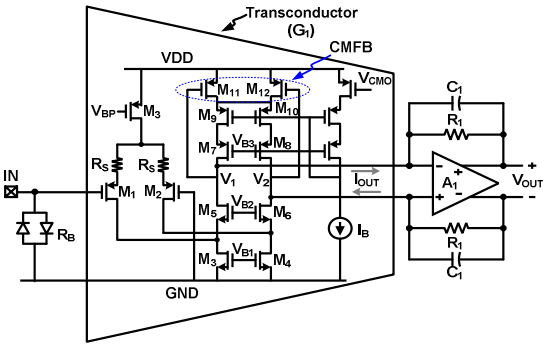

Figure 2. Gm-opamp-RC configured preamplifier

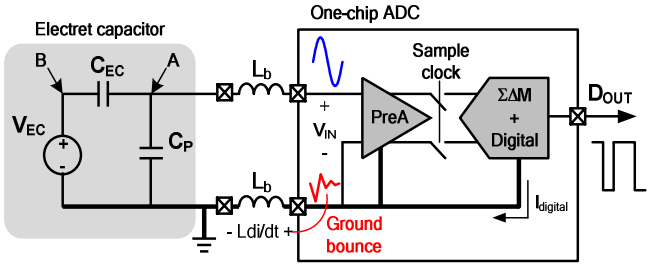

Figure 4. Input signal degradation by the internal ground bounce

The opamp A_1 for the transimpedance amplifier has a two-stage configuration with a telescopic 1st stage for high DC gain and a common source configured 2nd stage to provide a wide swing range. The signal gain of the whole preamplifier is depicted as

$$A_{preA} = R_1 / \left(R_S + 1/ g_{m1,2} \right) \quad (2)$$

in the audio band and the value in this design is 15dB. Note that R_S desensitizes A_{preA} to the PVT variation by reducing its dependency on $g_{m1,2}$. R_S can be determined by the linearity and noise trade-off. As R_S is increased, accordingly higher linearity will be achieved. However, a larger R_S results in higher noise [5]. Fortunately, the linearity requirement for the microphone application is not as strict. Generally, 1% THD is acceptable for an input of 100mVpp. Thus, in the present design, higher priority is given to lower the noise and the determined R_S value is about $2/g_{m1,2}$.

Owing to the virtual ground at the input terminals of A_1, the output voltage change of G_1 is negligible. Thus, a simple common-mode feedback with triode transistors M_{11} and M_{12} is designed along with proper biasing, as shown in Fig. 2. In order to realize zero current through the feedback resistor (R_1), both output common-mode levels of G_1 and A_1 are designed to be the same.

The input DC level of G_1 is at ground by the two zero-biased junction diodes (denoted as R_B in Fig (2)), which provides almost tera-ohm order resistance [6]. Special care is required with this high impedance node design in terms of layout and I/O pad, because any capacitive noise coupling or leakage current through this node can readily alter the signal integrity.

A single-bit 4th-order feed-forward ΣΔM has been designed for the A/D converter, as shown in Fig. 3. For better immunity to PVT variation and for flexible clock usage in many different applications, a SC ΣΔM has been chosen. PMOS input folded-cascode opamps with SC common-mode feedback circuits are used for integrators. An on-chip BGR is designed for a 1.25 V reference and a unity-gain buffer drives the reference voltage for the feedback capacitors. This reference driver adapts an on-chip RC damping circuit (as shown in Fig. 5(a)) to eliminate the large external capacitor. Ground level is used for a negative voltage reference, Vref-, for design simplicity and power savings.

B. Switching Noise Isolation

As noted earlier, in this design, only a single pad is assigned for the power and ground, respectively. Under this condition, switching noise that arises from digital switching is directly coupled to the analog circuits through the shared supply and ground rails as well as through a common

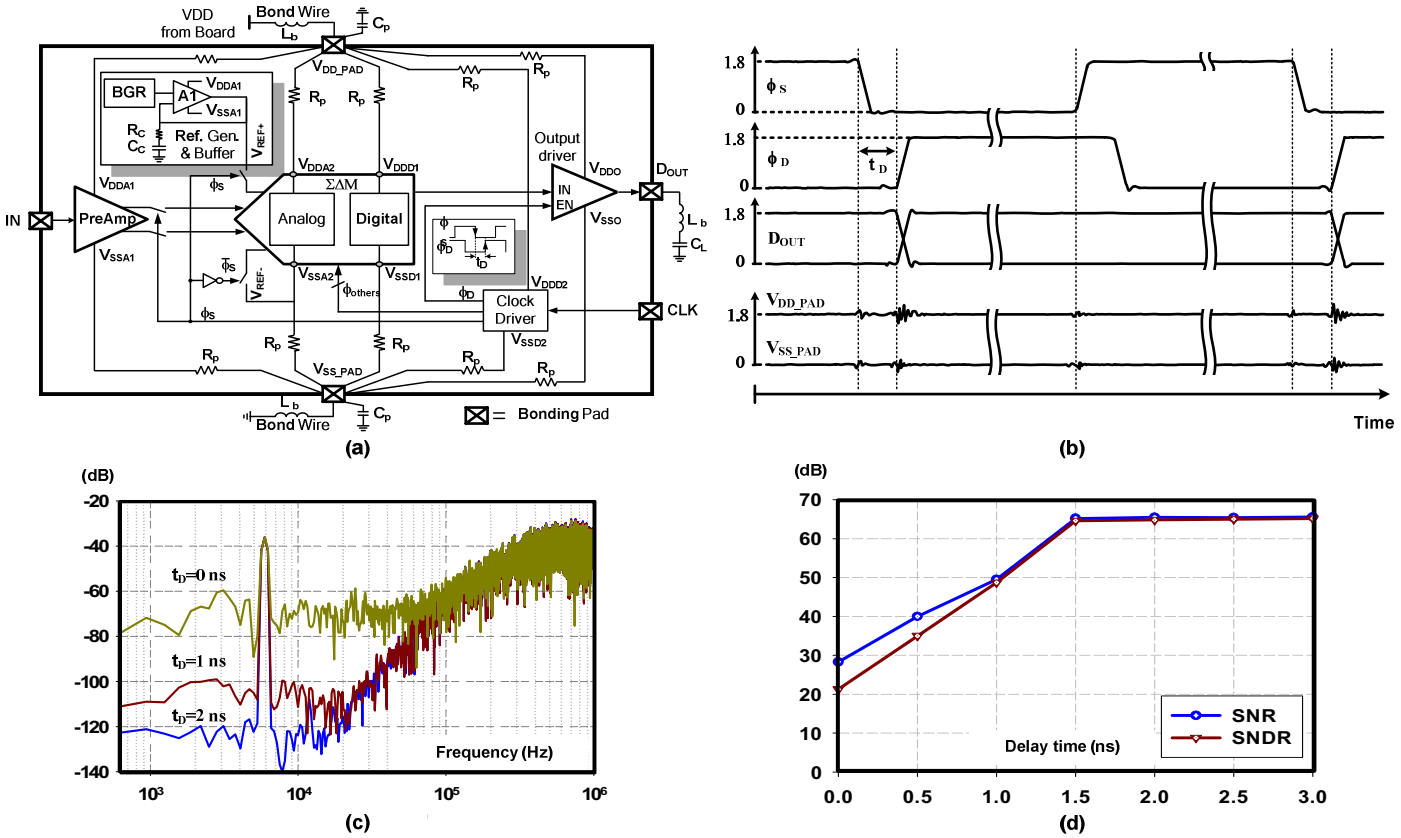

Figure 5. (a) Block diagram of prototype with power/ground routing plan, (b) Transient waveforms, (c) FFT of ADC output, and (d) Simulated SNR/SNDR

substrate, which can seriously degrade the signal integrity. Traditionally, this problem could be alleviated by separating internal supplies by inserting designated regulators for analog and digital building blocks. However, this regulator-based supply isolation technique is still not a perfect solution, because the ground and substrate remain strongly coupled. In the case of a single-end signal, this situation is more problematic. In our design, the signal from the EC is single-ended, as shown in Fig. 4, and thus the input signal to the preamplifier, V_{IN}, is seriously affected by the internal ground bounce. Exacerbating this, the regulator solution makes circuit design difficult due to the reduced internal supply, increased power consumption, and chip size. Therefore, in this design, the analog and digital circuits share supply and ground pads without regulators. Instead, time-domain noise isolation (TDNI) [3] is adopted with efficient noise coupling estimation. In addition, power/ground routings for each building block are distributed separately from the pads, as illustrated in Fig. 5(a). It is known that the switching noise occurring at the sampling instant seriously degrades the performance of the sampled system [7]. Since the output driver is the biggest switching noise source in this design due to its largest switching current, the output data transition instant is intentionally delayed after the analog sampling edge. This can be simply implemented by delaying the output driving clock using an inverter array instead of a D flip-flop, as in [3]. To guarantee signal integrity from the switching noise, the required delay time (t_D) of the output driving (rising edge of ϕ_D) from the input sampling (falling edge of ϕ_S) is found by post simulations with estimated external parasitic components such as bond wire inductance (L_b), pad-to-board capacitance (C_P), and output load capacitance (C_L). The values employed for L_b, C_P, and C_L are 2 nH, 2 pF, and 20 pF, respectively. Simulated transient waveforms at a certain value of t_D are shown in Fig. 5(b). No time scale is shown in the figure, because some parts of the waveforms are cut out for better display. At the beginning of output data (D_{OUT}) change, high frequency supply bouncing appears at the supply and ground rails (V_{DD_PAD} and V_{SS_PAD}), and the sampled signal can be seriously distorted if the input sampling is done before this noise vanishes. By varying t_D values from 0 to 3 ns with 0.5 ns step size, the ADC performances were simulated and compared. The FFT results of the ADC output for a 6 kHz 20 mV_{pp} input signal for the cases of t_D = 0 ns, 1 ns, and 2 ns are shown in Fig. 5(c). With t_D = 0, the FFT result shows a very high noise floor, and as t_D increases, the noise floor returns to normal. Fig. 5(d) shows the simulated SNR/SNDR of the full design for the same signal. At t_D = 0, the SNR drops to as low as 30dB. As t_D increases, the performance enhances, and for t_D > 1.5ns, the performance settles to a stable value of 65dB. Considering that device mismatches in differential circuits were not modeled in the simulation, a t_D of 4 ns was chosen in

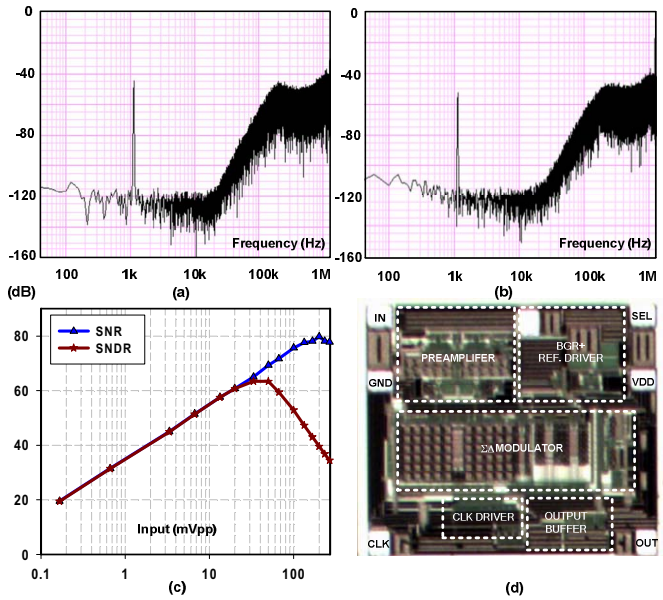

Figure 6. FFT results for (a) direct input (b) input via an EC model; (c) SNR/SNDR vs. Input signal, and (d) Chip photograph

the design. In order to compensate for the absence of consideration of the mismatch, all the circuits are placed as symmetrically as possible in the layout. Such fully balanced circuits will improve the power supply rejection as well.

III. Experimental Results

The prototype ADC for digital ECM was implemented in a 0.18 µm CMOS process. The chip was tested in two ways. First, in order to test the performance of the ADC core itself, the signal source was directly given to the input of the preamplifier (node A in Fig. 4). Second, the input signal was connected via 2.5 pF series and 2.5 pF shunt capacitors to emulate the effect of the electret capacitor (node B in Fig. 4). The measured FFT results for the two test benches at a 1 kHz 20 mV_{pp} sinusoidal input are shown in Figs. 6(a) and Fig. 6(b). The signal magnitude of the case with the electret capacitor model (Fig. 6(b)) is 8dB lower than that that of the case with direct input (Fig. 6(a)). Considering 1.2 pF input capacitance of G_1, the 8dB gain drop corresponds well with the expected result. When the input is given via an EC model, the ADC performance is very sensitive to the surrounding noise. Thus, the test was performed with the board in a shielding box. Nevertheless, Fig. 6(b) shows a 1.5dB higher noise floor than Fig. 6(a). This degradation can be the result of poor shielding condition, and thus better performance might be achieved if the chip is assembled in a real ECM canister. The measured SNR/SNDR versus direct input is shown in Fig. 6(c). At a 1.8 V supply and 2.56 MHz sampling frequency with a signal bandwidth of 20 kHz, the proposed ADC achieves a peak SNDR of 64.0 dB and DR of 84 dB with an A-weighted filter. The degradation of SNDR at large input signal is mainly by the nonlinearity of the preamplifier. But, note that the prototype shows almost the state-of-the-art performance among many voice application products. The

TABLE I. Performance Sumarry and Comparison

Parameters	This design	[2]	[3]
Process	CMOS 0.18µ	CMOS 0.5µ	CMOS 0.18µ
Supply	1.8V	1.8 V	1.8 V
Bandwidth	20kHz	11kHz	10kHz
Clock Freq.	1 – 5 MHz	1.404 MHz	2.56 MHz
Peak SNDR	64.0 dB	62.0 dB	62.0 dB
DR	84.0 dB	80.0 dB	78.0 dB
PSR	-72 dB	NA	NA
Power	420 µA	1.7 mW	450 µA
Chip size	750 x 770 μm^2 (including pads)	1.2 mm^2 (including pads)	400 x 600 μm^2 (exclud. pads)

measured power supply rejection (PSR) at a 217 Hz 100 mV_{PP} square wave is -72 dB. These results verify that a carefully designed fully differential circuit with time-domain noise isolation without regulators can be sufficient for commercial microphone specifications. The chip operates under supply voltage down to 1.6 V with little performance degradation. Total current consumption is 420 µA. The chip size including pads is 750 µm x 770 µm. Fig. 6 (d) shows a photograph of the ADC. The input pad is placed far away from the digital circuits and digital signals so as to minimize noise coupling. Two additional pads are utilized for test purposes. Performance summary and comparison are shown in Table I.

IV. Conclusions

A 20 kHz full audio-band A/D converter with a 84 dB dynamic range was implemented for high performance compact digital microphones. Microphone-oriented design directions such as preamplifier architecture and SC sigma-delta modulators with an overhead-free noise isolation method enable a low power high performance one-chip ADC with no supply regulation.

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