Low power, high linearity wideband receiver front-end for LTE application

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Abstract— **This paper presents a low power wideband receiver front-end implemented in 0.18 um CMOS technology for LTE application. The front-end includes a low-noise amplifier and a quadrature passive current commutating mixer. The inductive peaking LNA is designed using common gate topology for wideband matching with low power consumption. A noise cancellation technique is adopted for the LNA to achieve NF lower than 3dB. A variable gain transconductance amplifier is realized to expanse receiver dynamic range. The tranconductance cell with dynamic bias is designed for high linearity mixer performance. The receiver front-end operates from 0.7 to 2.7 GHz covering all frequency band of 3GPP LTE standard. The front-end shows 38 dB voltage conversion gain, 4.5 dB DSB NF, -10 dBm in-band IIP3 and -6 dBm out-of-band IIP3 while consuming 15 mA from a 1.8 V supply.**

Keywords − **CMOS receiver front-end, wideband, low power, LTE, 4G wireless communications, SAW-less receiver**

I. INTRODUCTION

LTE (3GPP Long Term Evolution) is the latest standard to provide mobile broadband service for fourth-generation wireless communications. LTE supports both frequency-division duplex (FDD) and time-division duplex (TDD), as well as a wide range of system bandwidths in order to operate in a large number of different frequency bands allocated from 0.7 to 2.7 GHz. In addition, LTE standard supports a large number of channel bandwidths that vary from 1.4 MHz to 20 MHz [1]. Therefore, the receiver design to cover all-band LTE application are challenged as receiver implementations in Software-Defined Radio (SDR) and/or multi-standard multi-band in aspect of high requirement in out-of-band interference rejection.

In a FDD system, the leakage from the transmitter appears at the receiver input as a strong interference leading to high requirements in out-of-band IIP2 and IIP3 performances. To alleviate this issue, conventional architectures adopt SAW filters before LNA or mixer to suppress the Tx leakage. However, off-chip inflexible SAW filters are hard to integrate into a receiver that covers all LTE bands. Alternative LC filters with limited Q factor can partly suppress the Tx leakage but the chip is bulky for multi-band implementations. Another low power approach is to design high linearity receivers using current mode architecture [2, 3]. In this architecture, the swing of signal in radio frequency is kept small by using a low noise voltage-to-current converter (trans-conductors). Conversion gain is preformed with a trans-impedance amplifier (TIA) with first-order low-pass filter characteristic thus providing good out-of-band IIP2 and IIP3. This approach has a disadvantage in aspect of noise figure when applied to wideband receivers. In practical, the low RF power gain in this approach is limited to suppressed noise from flowing stages.

This paper describes a low power, high linearity wideband receiver for 0.7 – 2.7 GHz frequency operation. By separating the wideband low noise amplifier (LNA) and transconductance amplifier (TA), the low NF of 4.5 dB is achieved while the IIP3 is maintain as high as -6 dBm based on a TA dynamic biasing linearization technique.

II. SPECIFICATIONS

Developed from UMTS (Universal Mobile Telecommunications System), LTE standards set a NF requirement of 9 dB [1]. From that, the different supported channel bandwidths and modulation schemes have difference sensitivity level making LTE terminal flexible to data communication depending on the distance to the base station. A reversed calculation of NF form reference sensitivity, bandwidth, modulation and SNR_{min} always has the NF of 9 dB. For example, the required minimum sensitivity of QPSK1/3 at 10 MHZ bandwidth is -94 dBm, SNR_{min} is 1 dB [1]:

$$P_{in,\,min} = -174\ \text{dBm/Hz} + NF + 10\log BW + SNR_{min}$$
$$NF = 174 + P_{in,\,min} - 10\log BW - SNR_{min}$$
$$= 174 - 94 - 10\log(10^7) - 1 = 9\ \text{dB} \quad (1)$$

A margin of 4 dB for the insertion loss of the duplexer and RF module is given leading to the NF requirement of 5 dB for our receiver.

In a linearity test of 10 MHz bandwidth case, the wanted signal is 6 dB higher than sensitivity level as of -88 dBm is used with two tone unwanted signals in adjacent channels N+1 and N+2 of -46 dBm. Assume that the 3rd order intermediation term contribute 25% to SNDR.

Therefore,

$$P_{IMD3} = P_{in} - SNR_{min} + 10\log(0.25) = -95\ \text{dBm}$$
$$P_{IMD3} = 3P_{blocker} - 2IIP3$$
$$IIP3 = (3P_{blocker} - P_{IMD3})/2$$
$$= [3x(-46)-(-95)]/2 = -21.5\ \text{dBm} \quad (2)$$

IIP3 requirements for different channel bandwidths considering required SNRs can be calculated similarly. The results are about 21 dBm for all of the cases [1].

In the LTE FDD systems, due to Tx leakage -30 dBm, the out-of-band IIP3 is -10 dBm for 10 MHz channel bandwidth up to -6 dBm in the case of 1.4 MHz channel bandwidth.

For IIP2 requirement, a typical value of Tx power leakage at LNA input is -30 dBm or -33 dBm for two tones modulated. The lowest signal come with – 110 dBm input power (as of 1.4 MHz bandwidth)

$$IIP2 = (P_{Tx,leak} - P_{in}) + P_{Tx,leak}$$
$$= (110 - 33) - 33 = 44 \text{ dBm} \quad (3)$$

Among the LTE bands, 700-MHz bands have the duplex spacing of only 30 MHz thus making the design of LTE receiver is most stringent requirement in linearity, both IIP3 and IIP2, compared to any other standard when RF SAW filters are removed from receiver chains [3].

III. Receiver Architecture and Circuit Designs

A. Receiver architecture

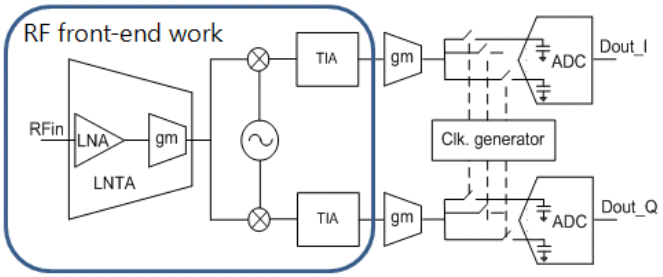

Figure 1. LTE receiver architechure with baseband charge-domain sampled filter

Figure 1 shows the block diagram of the full band LTE receiver. The receiver consists of an RF front-end and a baseband analog discrete-time signal processing stage. Direct conversion architecture is adopted for high flexibility, low power targets. After frequency down converted in RF front-end, the received signals are processed by discrete-time charge domain sampled filter and then applied into ADCs. The gain varied charge sampled filter is programmable by sampling frequency and capacitor bank for channel bandwidth variation in LTE specifications. Compared to traditional continuous-time baseband filters, the discrete-time counterparts have advantages in aspect of flexibly, reconfiguration, and robustness in process, temperature and voltage variation, especially in the trend of CMOS scaling down.

In this work, we concentrate on the design of a wideband RF receiver front-end, because most of challenging requirements (NF, IIP3, IIP2) in LTE standard are appeared early at RF front-end. Note that, if the noise or inter-modulated signal is folded into baseband frequency of a direct conversion receiver, there is no solution to take them out from the degrade SNDR of the system. The RF front-end includes a wide band LNA and a current passive mixer.

B. Circuit designs

1) Low noise amplifier

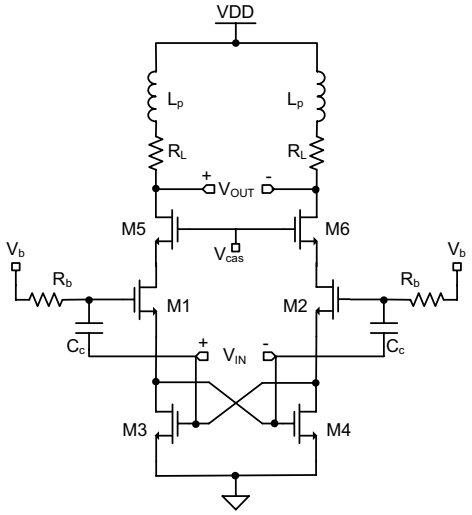

Figure 2. Siplified schematic of the wideband LNA

Wideband LNAs with noise cancellation have been preferred to designs of low cost multi-band multi-mode receivers [3, 4]. In those topologies, by sending the critical noise sources through an out-of-phase feedforward path, the output noise is significantly reduced at the summing nodes.

The simplified LNA circuit is presented in Figure 2. In order to achieve LTE requirement of IIP2, the circuit was implemented in differential scheme. The designed LNA is a version of [4] with adjustments to overcome gain drop at high frequencies when the LNA is loaded by an array of TA cells. First, the operation bandwidth is extended by placing peaking inductors at noise insensitive nodes [3]. Second, DC coupling is used to connect the common gate inputs to the negative *Gm* stage. In addition, the cross coupling capacitors in common gate pairs are done with only 2 pF MIM capacitors. These measures are to reduce the input capacitance of the LNA helping high frequency operation capability. In simulation, the LNA covers a frequency range of 300 MHz to 3.5 GHz with S11 < -12 dB, NF from 2.7 to 3.4 dB, voltage gain of 18 to 20 dB and IIP3 up to 0 dBm while dissipating only 3.2 mA current.

2) Mixer core and transimpedance amplifier

The mixer in for LTE receiver has a stringent noise figure and flicker noise requirement. Therefore, a passive current commuting mixer is implemented, as can be seen in Figure 3. A large trans- conductance gain guarantees low NF, while AC coupling capacitor prevents DC-current flow through mixing switches to reduce low flicker noise. Beside the similar purpose of bandwidth maintenance as LNA, the coupling capacitor between TA and switching pair is only 1 pF MIM help to suppress the second-order distortion from RF part come to baseband region thus improving IIP2 performance.

Without RF SAW filter, the mixer is required to work under large signal interferences. It is necessary of frequency down converted signal amplification with out-of-band

rejection. The transimpedance amplifier (TIA) constructed from an opamp and feedback resistors and capacitors terminates the switching pair in low impedance driving to high linearity TA operation. The IF signals are achieved high gain after the low-pass filter formed by feedback resistors and capacitors. The opamp for TIA is a conventional two-stage amplifier with high output swing.

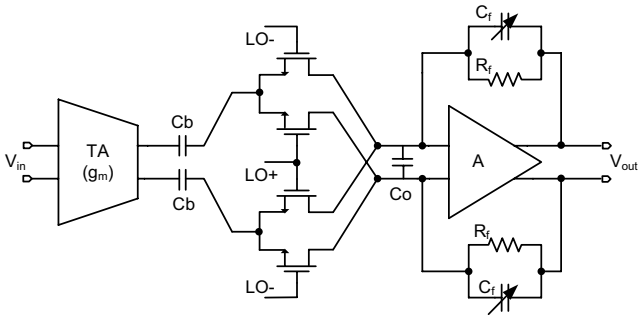

Figure 3. Current commutating passive mixer

To improve out-of-band linearity performances (IIP2 and IIP3) further, an addition capacitor is placed at the input of the TIA. However, due to low impedance at the TIA input, a huge capacitance is needed in the case of closed interferences. For an acceptable size, two 10- pF MIM capacitors with back-to-back connection are designed. With those capacitors, IIP3 and IIP2 are improved 1 and 3 dB, respectively.

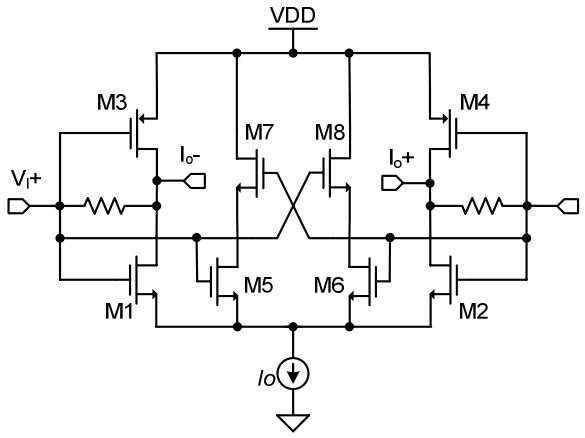

Figure 4. TA with dynamic biasing linearlization technique [5]

The passive mixer is made with an array of binary weighted TA cells based on self-bias inverter with dynamic bias [5] that provide scalable transconductance gain. The TA circuits have advantages in low noise, high linearity with low power consumption.

The 4-bit control capacitor bank is designed to program low-pass frequency poles of TIA from 0.75 MHz to 10 MHz of half channel bandwidths in the LTE standard. In order to maintain cut-off frequency under gain variation, feedback resistors are fixed, only TA cells are programmed by ON/OFF control.

IV. SIMULATION RESULTS

The receiver front-end is implemented in a 0.18 μm CMOS process. The circuit consumes 15 mA current from a 1.8 V supply for quadrature paths.

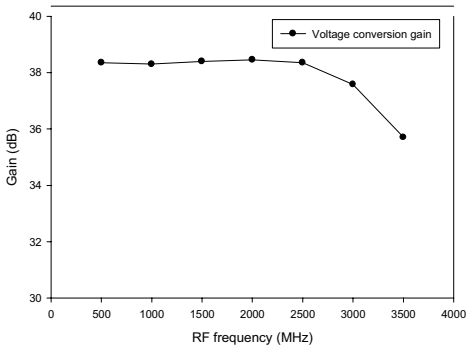

Figure 5. Simulated voltage coversion gain

Figure 5 shows the simulated voltage conversion gain of the receiver front-end verse RF frequency. The 3dB band-width is simulated up to 3.5 GHz. A flat gain of 38.4 dB is recognized from 500 MHz to 3 GHz thank to inductor peaking technique in LNA and using small AC coupling capacitors.

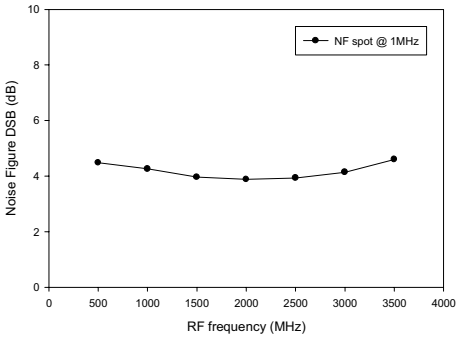

Figure 6. Noise figure at 1MHz IF frequency

Noise performance of the receiver front-end is depicted in Figure 6. The minimum DSB NF is 3.9 dB at middle of the interested frequency range. The NF is increased to 4.6 dB at 3.5 GHz due to gain drop, while it is also increased to 4.5 dB at 500 Mhz. This phenomena can be explained by the gain of LNA is lower at low frequency and peaked at 2 GHz.

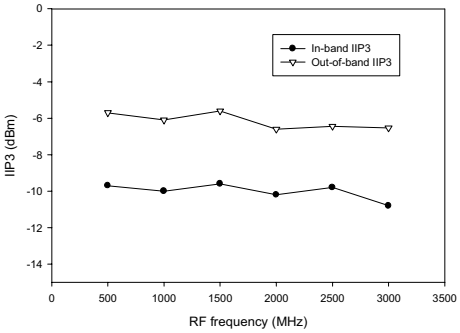

Figure 7. Simulated in-band and out-of-band IIP3

The inter-modulation tests are simulated with two tone inputs. For in-band IIP3, at f_{LO} band, we choose the signals at f_{LO} + 2 MHz *and* f_{LO} + 3 MHz. Offest frequencies of 23 and 45 MHz are given for out-of-band IIP3. Simulated in-band IIP3 and out-of-band IIP3 are -10 dBm and -6 dBm, respectively, as shown in Figure 7.

TABLE 1. PERFORMANCE SUMARY

Parameter	Specification	This work	Unit
Frequency	700 – 2700	500 – 3000	MHz
Gain	35	38	dB
NF	5	4 – 4.5	dB
IIP3 (in-band)	-21	-10	dBm
IIP3 (out-of-band)	-10	-6	dBm
Power	40	28	mW
Technology	-	CMOS 0.18	μm

V. CONCLUSIONS

A low power, high linearity receiver front-end is designed for operation frequency 700 – 2700 MHz. Low noise and high linearity performances are achieved with proper gain allocation for LNA and mixer accompanied with noise and distortion cancellation techniques. The receiver front-end has flexibility in channel bandwidth capable to be applied in full band LTE applications and SDR prototypes without RF SAW filters.

ACKNOWLEDGMENT

This work was sponsored by ETRI SoC Industry Promotion Centre, Human Resource Development Project for IT SoC Architect.

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