Current-Reused Single-Ended Current-Output Multiplier as a Core Circuit in a UWB Pulse Detector

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***Abstract*—This paper presents a low-complexity high-modularity low-voltage correlator for a 4.35-GHz coherent ultra-wide band impulse radio (UWB-IR) radar transceiver. The core circuit of the correlator is a current-reused four-quadrant multiplier with single-ended current-output. The correlator, which is implemented in a 0.18-μm CMOS technology, operates under 1.2 V while dissipating current of 186 μA. It is capable to generate output in response to UWB input pulses carried by 3.45-GHz wave at a pulse repetition frequency (PRF) of 8 MHz and with amplitude of 80 mVpp.**

***Keywords*—Current-reused, single-ended, multiplier, UWB, correlator**

I. INTRODUCTION

FCC allocated 3.1~10.6 GHz band as the spectrum of the ultra-wideband impulse radio (UWB-IR) system. Besides for data communication applications, the spectrum has also been frequently reported for being used for radar application [1]. To support its ranging capability, the radar usually adopts coherent detection architecture, whose demodulation process requires not only the phase or frequency of the received signals but also that of the transmitted signals.

Correlation-function based pulse detection is one of mostly implemented techniques in a UWB-IR coherent radar system. In this architecture, the correlation function is electronically performed by a correlator to detect the correct incoming pulse by correlating it to the template of the transmitted UWB pulse.

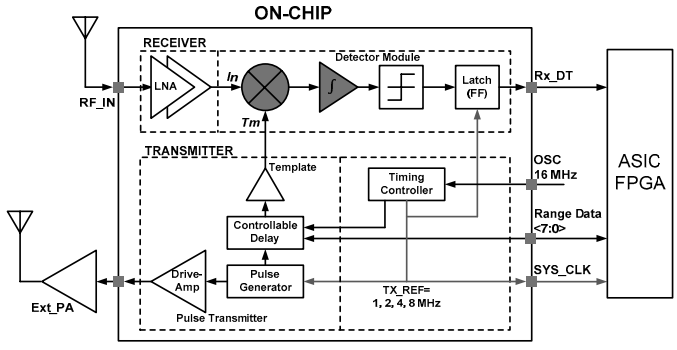

Figure 1. A coherent UWB-IR radar transceiver architecture

Fig. 1 shows the proposed coherent UWB-IR radar transceiver developed by our team. The analog correlator in the radar utilized a Gilbert-multiplier. The radar is designed to transmit 4-ns wide multi-cycle triangular-pulse with a -10 dB bandwidth of 520 MHz centered at 4.35 GHz, and have four selectable pulse repetition frequencies (PRF); i.e. 1, 2, 4 and 8 MHz.

The correlator in the receiver in Fig. 1 is drawn with shaded blocks, which consists of the multiplier and integrator blocks. The correlator is formed by connecting the multiplier output to the integrator input so that it resembles straightforwardly the correlation function as

$$v_o = K_I \int v_1 . v_2 \, dt, \qquad (1)$$

where v_o is the integrator output signal, v_1 and v_2 are the multiplier input signals coming from the LNA and the template generator, respectively *In* and *Tm* in the case of the one in Fig. 1, while K_I is an integration constant with suitable dimension.

An analog multiplier and capacitor are frequently used to implement a correlator to perform the multiplication and the integration function, respectively [2]-[4]. Since both input signals of a correlator are bipolar and their phases vary over time each other, there can be four phase combinations; i.e. (v_1, v_2), (v_1, $-v_2$), ($-v_1$, v_2) and ($-v_1$,$-v_2$). To cover all possible combinations, a four-quadrant multiplier is required for the correlator. The multiplier of this architecture is almost always fully differential, which means that they have two differential pair inputs, i.e. v_1 and v_2 pairs, and usually have also a differential pair output. To construct a correlator based on this multiplier architecture, additional stages may be needed to convert the differential output to single output.

This paper introduces a low-complexity high-modularity low-voltage correlator developed based on a current-reused four-quadrant multiplier with single-ended current-output.

II. CORRELATOR DEVELOPMENT

A. *Single-Ended Current-Output CMOS Multiplier*

Multipliers utilizing the non-linearity of MOSFET have been frequently reported. Ref. [5] discusses this type of multipliers and also introduces a new fully differential four-quadrant multiplier which is constructed with four sub-circuits as shown in Fig. 2. Transistors M_1~M_4 which are in linear region are the core of the multiplier, while transistors M_5~M_8 operate in saturation region to function as voltage followers.

Fig. 2 shows that the currents resulting from each phase combination of inputs are distinctively separate. The resulting currents I_1, I_2, I_3 and I_4 respectively correspond to the phase combinations of voltage inputs (v_1,v_2), (v_1,$-v_2$), ($-v_1$,$-v_2$) and ($-v_1$,v_2).

The multiplication result is obtained by summing and subtracting the currents entering the drain of the transistors M_5~M_8 with a certain order given by [5]

$$I_o = (I_1 + I_3) - (I_2 + I_4) = 4Kv_1v_2, \quad (2)$$

where $K = \mu_0 C_{ox} W/L$ is the notation for MOSFET (M_1~M_4 in this case) transconductance parameter.

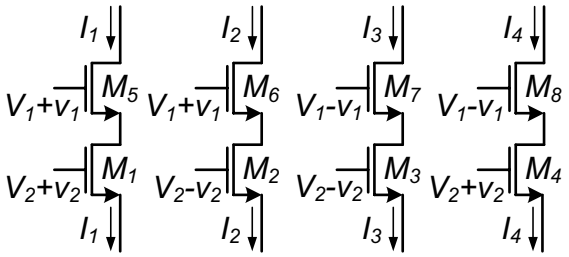

Figure 2. Constituting sub-circuits of the multiplier in [5]

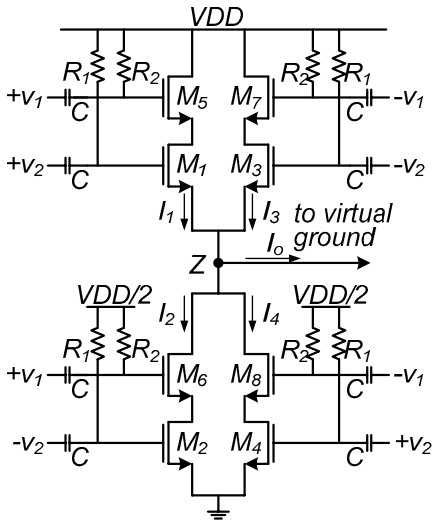

Figure 3. Current-reused multiplier with single-ended current-output

Referring to Fig. 2, by following Kirchhoff's current law (KCL), the currents coming out from the lower ends of the sub-circuits are equal to the currents entering into the upper ends. Therefore, (2) can also be implemented by stacking the sub-circuits which generate I_1 and I_3 onto the other sub-circuits which generate I_2 and I_4, and then tapping the current difference from the common connection node of all constituting sub-circuits. This arrangement, which has been introduced by our team in [6] and shown in Fig. 3, results in a multiplier with single-ended current-output. The biasing condition is also shown in the figure to emphasize that the corresponding transistors have to be biased equally. For this reason, the implementation of the multiplier requires a CMOS technology with triple-well process. The multiplier used in the experiment has been implemented using transistors with the size of *W/L*= 10*1.5 μm/0.18 μm, resistors R_1 and R_2 with high value resistance, and capacitors *C* of off-chip SMD.

The selected multiplier offers following advantages: (i) it has deterministic DC-output voltage, i.e. *VDD*/2 ideally, due to the symmetry of the upper- and lower-side sub-circuits; (ii) the DC-output voltage stays unchanged when the transistor conductance, *K*, is increased, e.g. by increasing *W/L* ratio, to generate higher output current as expressed by (2). These features are not available in the conventional differential-multiplier, e.g. [7] and [8]. In both cases, if *K* is increased, the DC-output voltage drops and the multiplier may turn off or its dynamic range is significantly reduced.

B. The Proposed Correlator

To keep the proper operation of the multiplier, its load must not shift the biasing voltage at the multiplier output (node *Z* in Fig. 3) away from *VDD*/2. This requirement is easily fulfilled when the multiplier is utilized as a part of the proposed correlator shown in Fig. 4 in which the multiplier is loaded with a capacitor as a current integrator. The capacitor, therefore, does not shift the DC quiescent point of the multiplier. The gain block in Fig. 4 is optional, but has to be of high input impedance.

As an integrator, the capacitor processes the resulted current as its input and produces voltage as its output. Therefore, the capacitor functions also as a current-to-voltage converter. As the output of the proposed correlator is in voltage, further processing of the signal can be suitably performed using CMOS based circuits.

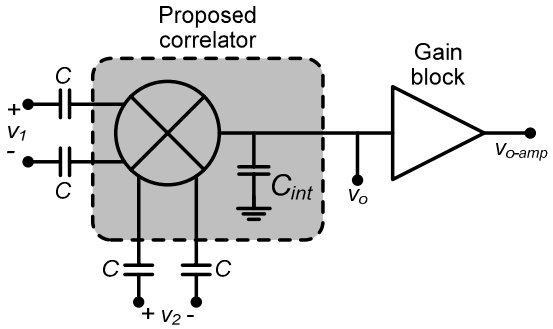

Figure 4. The proposed correlator with a gain block

C. Significant Feature of the Proposed Correlator

An analog correlator basically consists of a multiplier and an integrator. To capably trigger or drive the stage next to it, a gain block may be added, as shown in Fig. 4. In conventional multiplier based correlators, e.g. in [2] and [3], these blocks, i.e. the multiplier, integrator and gain block, are inseparable. Adopting the multiplier shown in Fig. 3 makes the constituting blocks of the correlator distinctively separable, enabling lower complexity and more independent optimization for individual block. It can also lead to possibility for low voltage and low power implementation of the correlator. Moreover, since the proposed correlator is only capacitively coupled to the input signal sources, the correlator or the detector module in Fig. 1 in general is also of high modularity.

III. EXPERIMENT SETTING AND EXPERIMENTAL RESULTS

A. Experiment Setting

To test the capability of the proposed correlator in detecting UWB pulses, the transmitter part of a custom-made UWB-IR radar transceiver which has been previously implemented by our team was utilized as a pulse generator. The PRF of the radar was set to the highest rate, i.e. 8 MHz. The generated

pulse was then fed to a balun to create differential pulses which were later connected to both inputs of the correlator accordingly.

The voltage output of the correlator is later amplified by a high input-impedance gain-block which functions also as a buffer to the measuring instrument. For the experiment, the gain block was implemented with an off-the-shelf SMD opamp. Fig. 5 shows the configuration of the experiment. The nodes where the signals were observed are annotated with circled numbers.

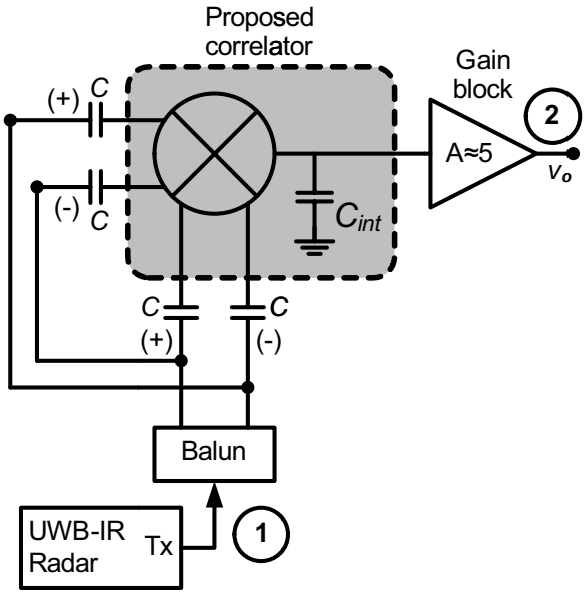

Figure 5. Experiment setting

B. *Experimental Results*

The pulse generator in the radar transmitter has been designed to emit 4-ns wide multi-cycle triangular pulses with -10 dB bandwidth of 520 MHz centered at 4.35 GHz. However, from the measurement, the -10 dB bandwidth that could be achieved was only around 400 MHz as shown in Fig. 6. Correspondingly, the narrowest pulse width achieved was only around 15 ns.

The shape of the pulses emitted by the radar transmitter in time-domain, which is fed to both inputs of the correlator, is plotted in Fig. 7 at the upper row. The amplitude of the input pulses is around 80 mVpp. The circled 1 (①) on the figure indicates that it was measured at the node ① in Fig. 5.

Fig. 7 also plots at the lower row the output of the correlator which was measured at the node ② in Fig. 5. The amplitude of the output pulses can reach up to 10 mV. Fig. 7 shows that the correlator is capable in converting bipolar pulses into unipolar pulse which means that the proposed correlator can perform the correlation function expressed in (1). Delay between input and output pulses in Fig. 7 was mainly caused by coaxial cables used in the measurement.

Fig. 8 shows the micrograph of the correlator IC used in the experiment. The IC has been implemented in a 0.18-μm CMOS technology with triple well process. The effective area of the correlator IC is 115 μm X 50 μm. The correlator operates under 1.2 V and dissipates current of 186 μA.

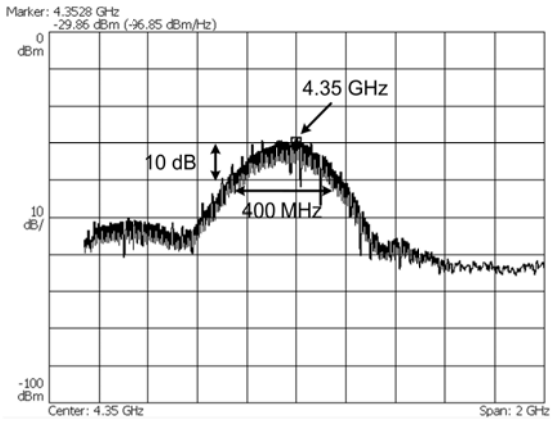

Figure 6. The frequency spectrum of the input UWB pulses at a PRF of 8 MHz

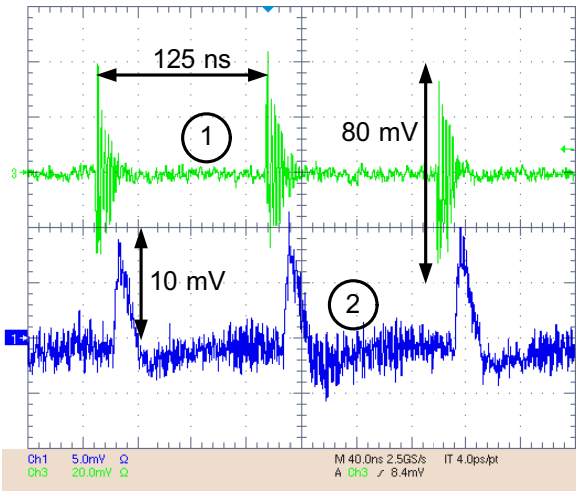

Figure 7. The shapes of ① the UWB pulses at the correlator input and ② the pulses at the correlator output in time-domain

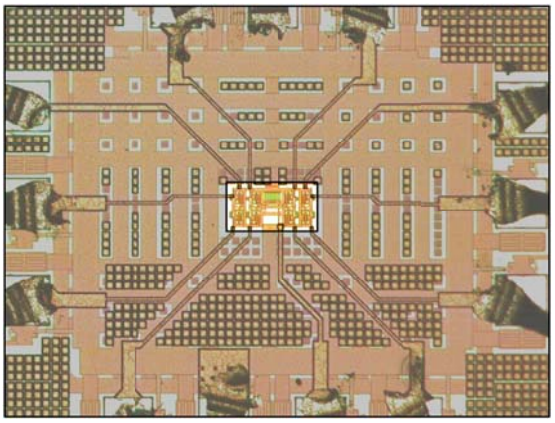

Figure 8. The micrograph of the correlator IC

IV. Discussion

The correlator which has been implemented in the detector module of the radar transceiver shown in Fig. 1 is designed to detect post-amplified UWB pulse with minimum amplitude of 40 mVpp, by correlating it to the template pulse with minimum amplitude of 250 mVpp. The product of these signals is higher than that of the signals used in the experiment, i.e. 80 mVpp X

80 mVpp. Therefore, the proposed correlator is noticeably promising to improve the receiver performance if it is implemented as a part of a new detector module on a single IC to replace the former version.

Moreover, several deficient conditions on the experiment also open up opportunities for the proposed correlator to have better performance. For example, the input impedance of each input pair of the correlator was conditioned for 50-Ω source impedance. However, in the measurement, both input pairs were directly paralleled, as shown in Fig. 5, creating input impedance of 25 Ω which was mismatched to the balun output impedance so that leading to lower output amplitude.

Furthermore, the capacitance value of the capacitor used as the integrator was relatively overly high; decreasing it could further increase the output amplitude. Likewise, the gain block used in the experiment had relatively low gain, which can be easily made much higher when the gain block is implemented as an integrated part of the detector module in a single IC.

The UWB pulse width used in the experiment was around 15 ns which is much wider than the targeted width, i.e. 4 ns. Therefore, the correlator was not tested with an accurate pulse. However, Fig. 7 shows that the width of the output pulse is quite similar to that of the UWB input pulse, which means that the proposed correlator is capable to respond at the speed of the input pulse's changing rate. Therefore, it is convincingly reasonable to infer that the proposed correlator can also detect 4-ns wide UWB pulse carried by 4.35 GHz wave.

V. CONCLUSION

An experiment on the proposed correlator, which adopts a four-quadrant multiplier with single-ended current-output, has been performed. The proposed correlator has been proven capable to detect UWB-IR pulse carried by 4.35 GHz wave. It suggests that the proposed correlator, which consists of a multiplier, an integrator and a gain block, is greatly promising to implement in 0.18-μm CMOS technology with triple-well process as a part of the detector module for the next version of the proposed UWB-IR radar transceiver.

ACKNOWLEDGMENT

This work was sponsored by ETRI SoC Industry Promotion Center, Human Resource Development Project for IT SoC Architect, and the CAD tools have been supported by IDEC of KAIST.

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