A High Linear Low Flicker Noise 25% Duty Cycle LO I/Q Mixer for a FM Radio Receiver

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***Abstract*— In this paper, a low power, low flicker noise and high IIP3 I/Q mixer for 76-108MHz EURO/US/Korea/Japan FM radio receiver applications is presented. The proposed mixer includes a transconductance (Gm) stage, a current mode passive switching stage driven by a 25% duty cycle LO, a transimpedance amplifier (TIA), and a 25% duty cycle LO generator. Simulation results show a 9.2dB DSB noise figure at 50kHz, 13dBm IIP3, and 23dB voltage gain, respectively, while drawing only 800uA including a LO generator from a 1.2-V supply in a standard 65nm CMOS technology.**

I. INTRODUCTION

Handheld electronic products such as smart phones, MP3 players, portable multimedia players (PMPs), and voice recorders are currently seeing widespread use. These products have a variety of mounted add-on functions as well as unique features. One of the popular add-on functions is a FM radio receiver. However, the integration of many features into a small portable device presents challenges with respect to achieving good performance under low power consumption. A direct conversion receiver (DCR) and low-IF receiver are frequently employed due to the simple architecture with low power consumption [1]. However, 1/f noise is a significant issue in this architecture, because the down-converted signal is located below the 1/f noise corner.

The mixer is one of the critical blocks affecting 1/f noise performance [2]. The mixer can be divided into two categories: active and passive mixers. In active mixers, the switching stage commutates not only AC current but also DC current, resulting in poor 1/f noise performance. Among efforts to improve the 1/f noise performance one of the popular methods is the current bleeding technique, which provides low DC current at the switching stage to reduce the 1/f noise [3]. A switched bias technique is proposed in [4]. Despite these efforts, in the case of active mixers, it is difficult to avoid the trade-off between 1/f noise and linearity, which is also an important performance in mixers [5]. Furthermore, the linearity of the mixer limits the whole linearity of the receiver front-end and is effectively scaled down by the gain of LNA. Therefore, it is essential to attain high linearity with low 1/f noise, which is difficult in active mixers. On the other hand, this can be realized with a passive mixer, as there is no trade-off between 1/f noise and linearity, due to the absence of DC current in the switching transistor.

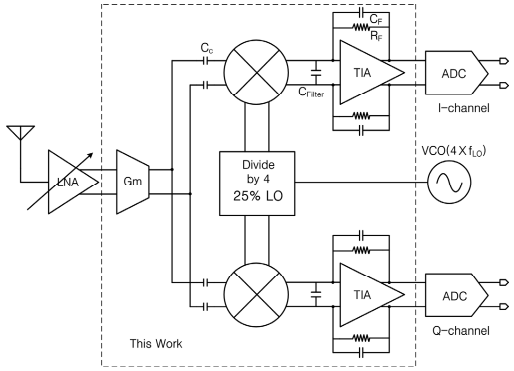

Figure 1. Block diagram of the FM radio receiver architecture.

In this paper, a high linear and low flicker noise I/Q passive mixer with a 25% duty cycle LO for a FM radio receiver is reported. Section II presents the architecture of the mixer. Section III describes the circuit blocks comprising the mixer. Section IV discusses the simulation results and section V concludes.

II. ARCHITECTURE

Fig. 1 shows a FM radio receiver architecture adopting the proposed I/Q mixer. The mixer is located after the LNA and down-converts the RF signal to a low-IF signal. A 150kHz center frequency is chosen for the intermediate frequency (IF) so as to attain high integrity and low power consumption of the baseband circuitry, TIA, and ADC. The bandwidth of a FM broadcasted signal is 200kHz. Therefore, down-converted signals will locate at 50-250kHz. Under these conditions, 1/f noise significantly affects the overall system noise. Widely used active mixers suffer from high 1/f noise and poor linearity, especially when the supply voltage is low. On the contrary, a current driven passive mixer can provide relatively

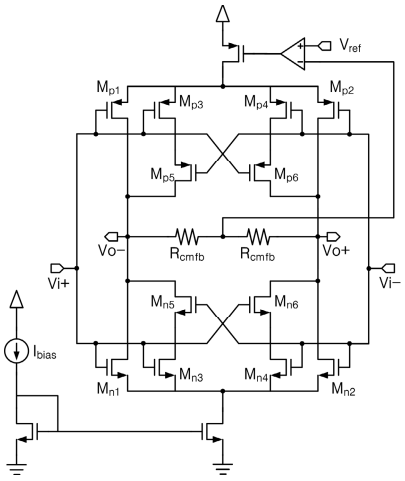

Figure 2. Simplified schematic diagram of the proposed Gm stage.

good linearity and inherent low 1/f noise performance, since it has low impedance following the switching stage, which reduces voltage swing at its input and output. Furthermore, the switching stage only commutates AC current, not DC current. Therefore, the above FM radio receiver architecture is adopted.

III. CIRCUIT BLOCKS

The current driven passive mixer is comprised of a Gm stage, switching core, and TIA. The divide by 4 circuit, which include LO buffers generates non-overlap 25% duty cycle rail to rail rectangular wave signals.

A. Gm stage

Fig. 2 shows a schematic of the proposed Gm stage, which converts the amplified RF voltage following LNA to current. It consists of a differential pair and a common-mode feedback circuit to keep the output voltage as half of VDD. It is necessary to increase the transconductance of the Gm stage because the loss at the following passive switching stage degrades the overall mixer NF. In this application, the power consumption is also a critical issue due to the battery operation. In order to achieve high gain with low power consumption, proposed Gm stage adopts current reused complementary input which boosts up transconductance by 2 times. Another advantage of complementary input is that input nMOS and pMOS can have same DC bias level so that input capacitors for DC bias level separation between nMOS and pMOS are not required that may occupy quite large chip size due to the input RF frequency which is located at few hundred MHz.

In a current driven passive mixer, the Gm stage is the main building block affecting linearity, because voltage to current conversion process of the Gm stage produces significant nonlinearity [1]. On the other hand, the switching stage only commutates AC current with no voltage swing, and current to voltage conversion is performed by the RC feedback. To improve the linearity of the Gm stage, the g_m" cancellation technique presented in [6] was employed. In [6], third order nonlinearity of nMOS inputs is cancelled out by auxiliary nMOS transistors that operate in the triode region. In this design, the complementary structure consists of nMOS and pMOS input stage, which have different gm" cancellation

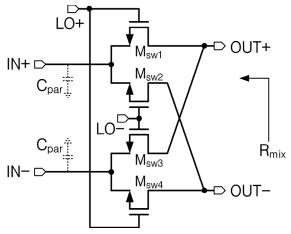

Figure 3. Simplified schematic of the switching stage.

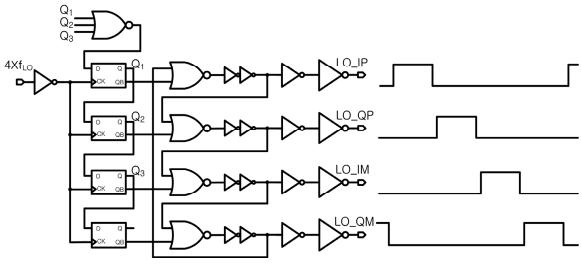

Figure 4. 25% duty cycle LO generator with LO wave forms.

points. Therefore, it is difficult to cancel out the nonlinearity of both the nMOS and pMOS simultaneously by only the auxiliary nMOS transistor. In order to resolve the above problem, a new Gm stage adopting the g_m" cancellation technique for both the nMOS and pMOS input is proposed. Even though there are four stacked saturated transistors, the linearity is not degraded. Because the output of the Gm stage is connected to the low impedance node of the TIA, the voltage swing at the output is small. Each transistor performs the following role. $M_{n,p1\text{-}2}$ act as the main amplifier and are biased at the saturation region, providing negative g_m". $M_{n,p3\text{-}4}$ act in the deep triode region, providing positive g_m". $M_{n,p5\text{-}6}$ help $M_{n,p3\text{-}4}$ to operate in the triode region by reducing the drain-source voltage (V_{ds}) of $M_{n,p3\text{-}4}$. Finally, the negative third order nonlinearity of the main transistors ($M_{n,p1\text{-}2}$) is cancelled out by the positive third order nonlinearity of the auxiliary transistors ($M_{n,p3\text{-}4}$).

Due to the current reused complementary input and adoption of nMOS and pMOS g_m" cancellation technique separately, the proposed Gm stage achieves high linearity while consuming small current consumption (400uA).

B. Switching stage with 25% LO generator

Fig. 3 shows the switching stage driven by a 25% duty cycle LO, which performs actual frequency down-conversion. The double balanced structure consists of transistors $M_{sw1\text{-}4}$ and is used to reduce LO to IF leakage. Transistor size shows a significant impact on the mixer performance [7]. If the size is too small, the on resistance will be large and will increase the voltage swing across the switching quad, which reduces the mixer linearity. In contrast, if the size becomes too large, the NF will be increased by the TIA noise amplification phenomenon [1]. The TIA output noise is given by

$$v_{nout,TIA}(f) \approx \left(1+\frac{2R_F}{R_{mix}}\right)\cdot v_{n,TIA}(f) \qquad (1)$$

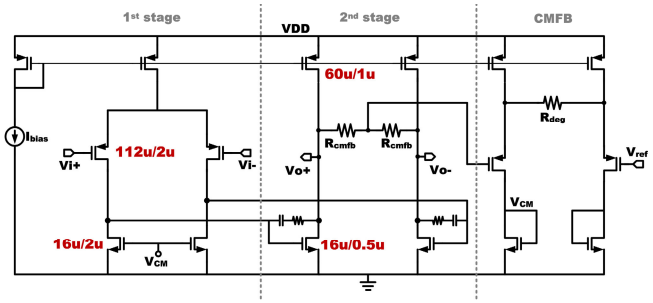

Figure 5. Schematic of the OTA.

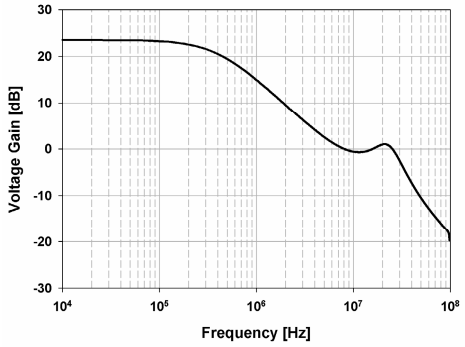

Figure 6. Simulated gain versus IF frequency.

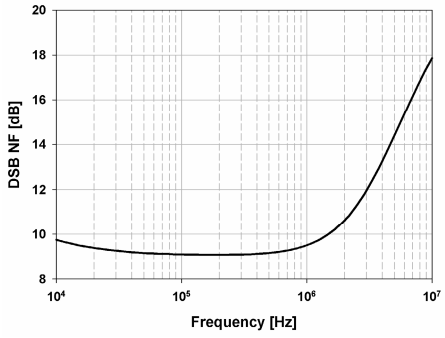

Figure 7. Simulated DSB noise figure versus IF frequency.

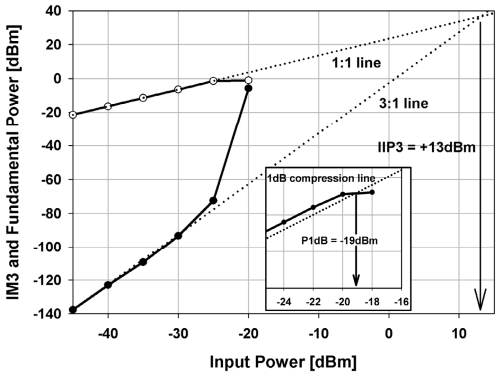

Figure 8. Simulated in-band IIP3, P1dB performance.

where $v_{n,TIA}(f)$ is the input referred TIA noise and R_{mix}, as shown in Fig. 3, is the output impedance of the switching stage and is given by

$$R_{mix} = \frac{1}{4 f_{Lo} C_{par}} \tag{2}$$

TIA noise will be amplified if the parasitic capacitance C_{par} , as shown in Fig. 3, of the Gm stage's output and switching transistors is increased. The conventional 50% duty cycle LO driven I/Q mixer experiences a time interval when the I path and Q path simultaneously are on. This problem has two disadvantages: the output impedance of the switching stage, R_{mix}, will be lowered due to the loading of the other channel; and the output current of the Gm stage is divided between the I and Q paths. Ultimately, these two issues lower the gain and increase the NF of the I/Q mixer. The above problems can be resolved by using a 25% duty cycle LO, since the I or Q path will be turned on respectively that can supply full RF current to each path [8].

Fig. 4 shows the 25% duty cycle LO generator and LO waveforms. In order to prevent the switches from being turned on at the same time, the waveforms do not overlap. A gradual increase inverter type LO buffer is adopted due to rail to rail driving and short rising/falling time. The simulated rising and falling times are about 50ps. Due to advanced process technology and low frequency operation, the 25% duty cycle LO generator with LO buffers consumes about 50uA average current.

The switching stage is AC coupled with the Gm stage by a coupling capacitor C_c, as shown in Fig. 1. Without using C_c, the different DC bias level between the Gm stage and TIA generates DC current, which worsens the 1/f noise. Another function of C_c is to prevent low frequency second order nonlinear current of the Gm stage.

C. TIA

TIA consists of an operational transconductance amplifier (OTA) with a feedback RC. The TIA provides low impedance to the switching stage output, causing the mixer to operate in current mode. The TIA input impedance is given by

$$Z_{in}(f) \approx \frac{2}{A(f)} \frac{R_F}{1 + 2\pi f R_F C_F} \tag{3}$$

where $A(f)$ is the open loop gain of the OTA [5]. Due to limited OTA bandwidth, high frequency components suffer high impedance, and consequently the TIA input has a large voltage swing, which can degrade linearity. In order to filter out unwanted high frequency components, C_{Filter} is inserted, as shown in Fig. 1. Feedback R and C form a first order filter that attenuates out of band blockers [9]. Another function is I to V conversion, which results in an output voltage swing in the mixer. The 10KΩ optimized value of feedback resistors is chosen to address the tradeoff between gain and linearity.

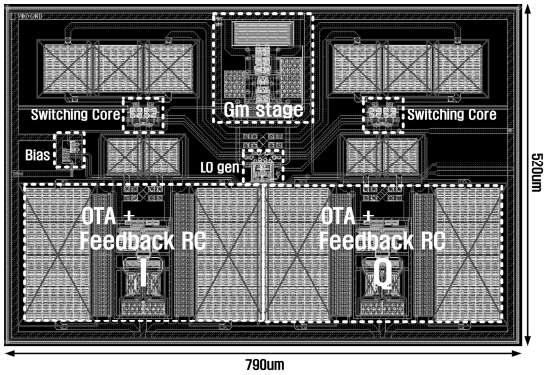

Figure 9. Layout of the I/Q mixer.

Considering signal bandwidth and layout size, feedback capacitors are chosen. In order to maintain TIA input impedance as low as possible, the OTA should have high gain. For large swing at the output, the OTA's output should have almost a rail to rail swing. Considering the above requirements, a two stage OTA was designed as shown in Fig. 5. Due to the noise amplification mechanism noted earlier, the TIA should be designed with low noise, especially 1/f noise. Therefore, nMOS and pMOS transistors of the OTA's first stage should have long channel length [10]. In this design, each TIA consumes 175uA.

IV. Simulation Results

The proposed I/Q mixer was simulated in 65nm CMOS technology. Fig. 6 shows the voltage gain of the mixer. The simulated voltage gain is close to 23dB. The 3dB bandwidth of the mixer is 400kHz, considering signal bandwidth and in-band gain roll-off by a first order filtering function. There is out-of-band peaking at around 20MHz. This feature is caused by the use of very large input transistors in the OTA [10]. Fig. 7 shows the simulated double-sideband NF (DSB-NF). The highest NF in the signal band is 9.2dB at 50kHz. A 1/f noise 3dB corner exists below 10kHz, and consequently 1/f noise has a reduced effect on wanted signals. Fig. 8 shows the in-band IIP3 and P1dB of the mixers. To simulate the in-band IIP3, a two tone signal comprising 100.1MHz and 100.13MHz was applied. IIP3 components then fall at 70kHz and 160kHz while the wanted signal falls at 100kHz and 130kHz when 100MHz LO frequency is used. A P1dB simulation is performed with a 100.2MHz RF signal and 100MHz LO signal. As shown in Fig. 8, the input referred IIP3 was 13dBm and P1dB was -19dBm. Due to the proposed Gm stage, the mixer shows good linearity. Fig. 9 shows the layout of the circuits. The summarized performance of the I/Q mixer along with a comparison with previous mixers is shown in table I. Compared to previous works, this mixer achieves high IIP3 and low 1/f noise with significantly low power consumption.

V. Conclusion

In this paper, a current driven passive mixer with a 25% duty cycle LO is reported. By adopting g_m" cancellation in the Gm stage and a 25% duty cycle LO in the switching stage, the proposed mixer achieves good linearity and significantly low 1/f noise with extremely low power consumption. Simulated in 65nm CMOS technology, the proposed mixer shows 23dB gain, 9.2dB DSB-NF, under 10kHz 1/f noise corner frequency, and 13dBm IIP3, respectively, while consuming 960uW from a 1.2V supply.

TABLE I. PERFORMANCE COMPARISON OF MIXERS

Parameter	[3]	[4]	[10]	This work
Technology	0.13um	0.18um	0.18um	65nm
Supply Voltage (V)	1.2	1.8	2	1.2
Voltage Gain (dB)	0.5	7.5	25	23
NF (dB)	11	7.6	9.5	9.2
Input P1dB (dBm)	-1.5	N/A	-12	-19
IIP3 (dBm)	10.5	-5	7	13
1/f nosie corner (kHz)	10	1000	N/A	<10
Bias current (mA)	2	4.5	5(I+Q)	0.8(I+Q)

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