A 520 pJ/pulse IR-UWB Radar for Short Range Object Detection

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***Abstract* — This paper presents a low power, low complexity IR-UWB radar transceiver for short range object detection. The transceiver provides robustness against false alarms without increasing power consumption, chip size, or complexity. The receiver (RX) and the transmitter (TX) dissipate only 50 pJ/pulse and 470 pJ/pulse under a 1.2V supply, respectively. The measured TX pulse spectrum, -58 dBm maximum power, complies with the FCC spectral mask and shows 1 GHz bandwidth with 4 GHz center frequency. The measured sensitivity of the RX is -45 dBm, and the RX is fully functional to detect an object in the range of 0.45 ~ 1.2 m. The die size of the IR-UWB transceiver implemented in a 0.13 um CMOS process is 2.1 mm^2.**

***Index Terms* — Radar detection, low noise amplifier, correlator, pulse generation, and interference suppression.**

I. INTRODUCTION

Recently, interest in impulse radar systems has significantly increased due to their low power consumption for applications such as short-range radio communication, ranging systems, and object detection [1-4]. Impulse radar systems using the unlicensed 3.1 ~ 10.6 GHz frequency range, as designated by the Federal Communications Commission (FCC), can be applied in various fields [5]. The FCC limits the radiated power level less than -41.3 dBm/MHz as the noise level for existing standards. There are two demodulation schemes for UWB pulse-based systems, coherent and non-coherent. Although coherent receivers are robust to false detection, the architecture is complex due to the correlation operation. In contrast, non-coherent receivers are simpler, but less robust to false detection. Since the major technical requirements for low data-rate or energy detection systems are low cost, low complexity, and low power design, and thus such systems often adopt the non-coherent demodulation scheme [2-4]. This paper reports design of a robust (to false detection) low-power non-coherent transceiver with a simple architecture.

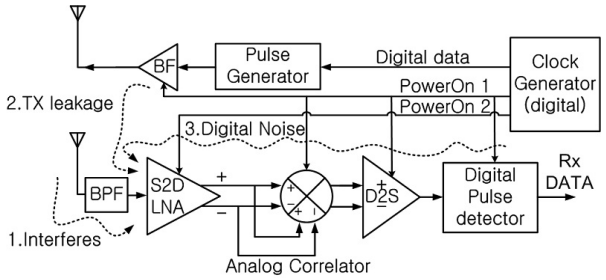

Fig. 1. Proposed low-power low-complexity transceiver

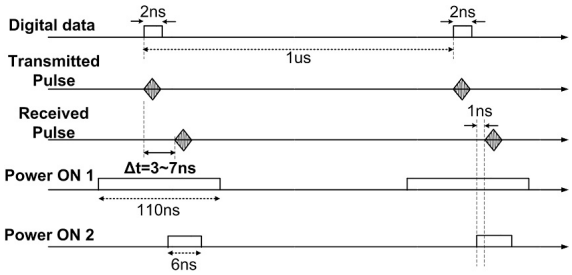

Fig. 2. Timing diagram of the proposed transceiver

II. TRANSCEIVER ARCHITECTURE

The requirement of the proposed object detection system to detect an object located in the short range of 0.45 ~ 1.2 m from the antenna. Any objects closer than the minimum distance or farther than the maximum range should be recognized as erroneous detection. Fig. 1 shows the proposed self-mixing low-power transceiver architecture. A pulse generator and a buffer form a transmitter, and the clock generator provides digital data and power on/off signals for the power saving scheme. Because the longest detection distance is only 1.2 m, the required TX output power is low, -11 dBm, and the required sensitivity of the RX is moderate, -45 dBm under 34 dB channel loss and 15 dB antenna gain. To meet the important requirements of the proposed system, i.e., low power, low cost, and low circuit complexity, a self-mixing receiver architecture is adopted to eliminate the PLL/VCO part. Fig. 2 shows a timing diagram of the transceiver. The pulse generator is triggered by a 2ns

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digital pulse with 1 MHz PRF (Pulse Repetition Frequency), which is generated by the clock generator. The pulse generator transmits a 4 GHz carrier signal with 2 ns duration, and the transmitted pulse is reflected back to the receiver with time delay (t = 3 ~ 7 ns) by an object in the detection range of interest. To prevent erroneous detections, the receiver is turned on only when the reflected pulse from an object exists in the designated range (which is 0.45 ~ 1.2 m). Therefore, power ON 2 signal in Fig. 2, rising at t = 2 ns and falling down at t = 8 ns, is applied to receiver. Therefore, the turn on/off time duration should be under 1 ns for the receiver. However, the correlator cannot be turned on/off rapidly because the block consumes tiny current. Rather, LNA is turned on/off by power ON 2 signal. In addition, the power on/off function prevents the TX leakage to the receiver, which would cause a serious problem for the detection. To save power, the TX buffer and the RX correlator, which are slow turned-on/off blocks, are controlled by power ON 1 signal, which has a larger pulse width than power ON 2 signal. For short range detection, a 2 ns triangular-enveloped pulse transmitted has 1 GHz bandwidth [6], but the bandwidth of the LNA is 400 MHz to ensure effective rejection of interference. In addition, the RX chain is fully differential, so as to reduce digital/supply/ground noise, which can cause false detections. As mentioned earlier, the non-coherent self-mixing approach is susceptible to false detections when noise exists at the input of the receiver. The following schemes are adopted for the proposed transceiver to reduce interference and noise, while maintaining low power and simple architecture.

1) Interferers – Strong interferes, 2.4 GHz ISM and 5 GHz 802.11a bands, are located near the proposed radar system of 4 GHz band. The off-chip BPF and the LNA of the receiver reduce the interference level below the receiver sensitivity level.

2) TX leakage –TX leakage can lead to continuous erroneous detection and possibly system failure. The radar transceiver adopts two separate antennas instead of a switch to reduce the TX leakage. In addition, the receiver provides time filtering, which is explained in the following section.

3) Digital/Supply/Ground noises – The radar system can suffer from digital noise from the clock generator and the digital pulse detection block. The LNA in the receiver adopts the single-ended to differential (S2D) converter architecture, so that differential signal processing can be performed after the LNA.

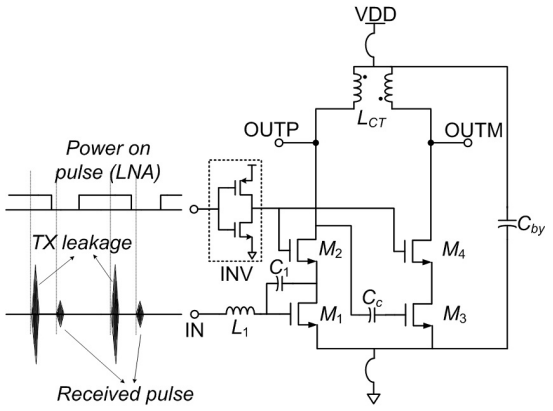


Fig. 3. The proposed fast on/off S2D LNA

III. CIRCUIT DESIGN

A. LNA design

One of the most important design requirements for the proposed radar system are low power and low cost. However, a fully differential signal for the entire receiver chain is essential to improve immunity from supply/ground and digital noise (at the cost of higher circuit complexity) and thereby prevent false detections. An off-chip or on-chip transformer could be used at the front of the receiver, but increases the cost and the foam factor. The S2D conversion can be a suitable solution for the LNA, which has little impact to the power consumption and the chip size. As illustrated in Fig. 3, the proposed fast on/off S2D LNA consists of two cascode amplifiers sharing an LC tank load. The on-chip bypass capacitor, C_{by}, removes ground and supply bonding wire effects and avoids uncertainty in the input impedance and an unexpected resonance with parasitic capacitances. The input matching network, L_1 and C_1, results in input impedance of 50 . The shunt-shunt feedback capacitor, C_1, is small in order to ensure the real value of the input impedance [7], and thus the LNA, without a source degeneration inductor, sacrifices some gain loss for the benefit of a smaller area. The gate inductor, L_1, cancels out the imaginary part of the input impedance. A high frequency gain is achieved by resonating the output node parasitic capacitor with the center-tapped inductor, L_{CT}. The voltage signals of the two LNA outputs are differential due to the symmetric of L_{CT}. Therefore, the proposed LNA implements the high frequency BPF and S2D functions with little increase in power consumption nor die area. The 400 MHz BPF gain of the LNA mitigates unwanted interferences to reduce false detections. As mentioned before, the LNA should be

rapidly turned on after the TX signal is emitted and before the RX signal arrives, so that the receiver does not generate any output due to the TX leakage. After the power ON 2 pulse rises, the LNA needs to be turned on within 1 ns. To turn the LNA on rapidly without degrading LNA performance, two conditions should be met: (1) Neither large resistors nor capacitors are placed at the control node, and (2) No additional switches on the signal path. The suitable nodes to meet the requirements are the gates of the cascode transistors, M_2 and M_4. These nodes are always connected to a low impedance, because the inverter, *INV*, acts as a switch to link the ground or supply.

B. Correlator and pulse detector design

Fig. 4 shows the correlator and the pulse detector. The analog correlator converts a RF pulse into an analog base band pulse, and the differential to single-ended amplifier removes the common-mode noise. Then, the single-ended analog base band signal is converted to a narrow digital pulse by comparators. The digital circuit expands the narrow pulse into a wide digital pulse. Since the polarity of the resultant signal can be in either the positive or negative direction depending on the distance of the transmission link, two comparators are used to detect the positive and negative pulses. To protect against false alarms in case the LNA fails to suppress the noise sufficiently, time filtering is implemented doubly. The filtering is controlled by CLK_{Steady}. Pulses at nodes c_1 and c_2 pass to nodes d_1 and d_2, respectively, if they are generated under CLK_{Steady} = high. Fig. 5 (a) shows the correlator circuit of given in reference [8]. To act as a multiplier, M_1~M_4 must be in the linear mode, while M_5~M_8 must be in the saturation mode. Due to the use of the resistive load, the circuit biasing should be designed carefully to achieve the condition. Moreover, the resistive load necessitates a higher voltage supply for the circuit. As the proposed correlator, therefore, only the active part in the reference circuit is adopted and stacked vertically, as shown in Fig. 5 (b). The advantage of the approach is 50 % of less power consumption and simple biasing. Moreover, the high output impedances of M_1, M_3, M_6 and M_8, which are in saturation mode, and the parasitic capacitances of those MOS integrate the resulting current into voltage, which is easier to detect and amplify

$$v_O = K_I \int (I_{O1} - I_{O2})dt = K_V \int (v_x \cdot v_y)dt \qquad (1)$$

C. Transmitter and clock generator design

The proposed low-power transmitter follows the approach reported in [6] with a buffer for the output matching. The pulse generator [6] is directly controlled by a digital pulse with 2 ns pulse width. The main advantage of the pulse generator is low power, because the circuit consumes power only during 2 ns for each 1 us period. Furthermore, the circuit generates a triangular-enveloped pulse, which achieves more than 20 dB of side lobe rejection without an additional filter. The clock generator provides three kinds of clocks: digital data, power ON 1, and power ON 2, as shown in Fig. 2. A 16 MHz crystal reference clock is applied externally, and digital circuits generate several clocks using inverter delays.

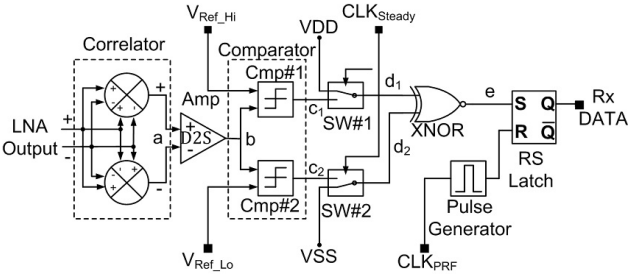
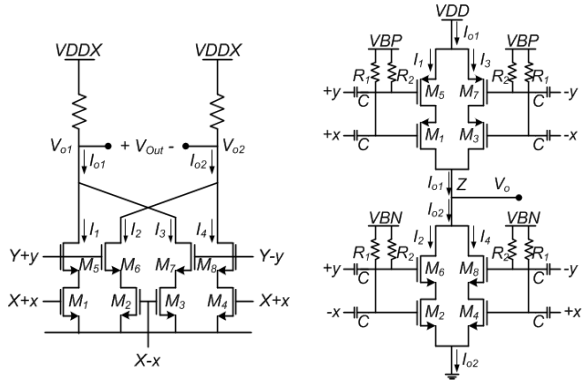


Fig. 4. The analog correlator and pulse detection block



(a) (b)

Fig. 5. (a) Reference circuit [8] (b) Current reuse single-output multiplier as a correlator

IV. MEASUREMENT RESULTS

The proposed low-power transceiver is implemented in a 0.13 um CMOS process. The power spectrum density (PSD) of transmitter pulse, which is less than the FCC limit of -42 dBm/Hz, is shown in Fig. 6. The measured power consumption of the pulse generator is 70 pJ/pulse with 1 MHz PRF, and the buffer consumes the most power for the system, 400 pJ/pulse. The power dissipation of the LNA is 30 pJ/pulse excluding the bias current consumption, owing to short turn on time (= 6 ns).

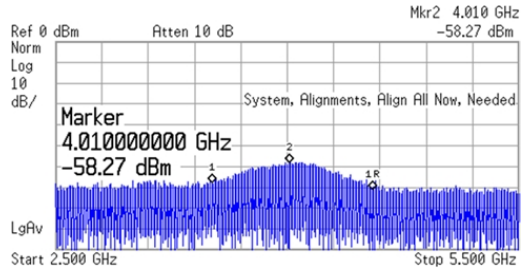
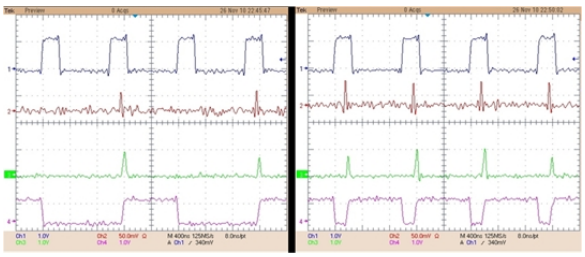


Fig. 6. Measured PSD of 1 GHz BW TX pulse



(a) (b)

Fig. 7. The final receiver measured pulse. The PRF of the power ON 2 pulse in Fig. 2 is (a) 500 KHz, and (b) 1 MHz

Moreover, the proposed current reuse correlator and the pulse generator including a few digital gates dissipate small power, only 20 pJ/pulse. Fig. 7 shows receiver measurement results. The top waveform is the on-time of the RX (port CLK_{PRF}) with PRF = 1 MHz. The second one is the received signal after the LNA under the PRF of power ON 2 pulse is 500 KHz for Fig. 7 (a), and 1 MHz for Fig. 7 (b). The third one shows a monopole narrow digitalized pulse after comparator, node 'e' in Fig. 4, and the last one indicates the final RX_DATA. The comparison between Figs. 7 (a) and (b) indicates no false alarms provide time filtering for the LNA and the pulse detector is working. Short "0" in Fig. 7 (b) is due to a reset at the rising edge of the RX PRF pulse (the top waveform). Fig. 8 shows a micrograph of the fabricated chip with the die area of 2.1 mm^2.

V. Conclusion

The proposed IR-UWB system realizes low cost, low complexity, and low power design, while robust to false alarms. The low cost and simple transceiver is achieved through adoption of (i) a self-mixing receiver that provides robustness against false alarms and (ii) a transmitter which consists of a pulse generator and a buffer. The proposed self-mixing type receiver is composed of a S2D LNA (that can be turned on/off within 1 ns), a current reused correlator, and a pulse detector. The power dissipation of the core LNA is only 30 pJ/pulse, owing to short turn on time of only 6 ns.

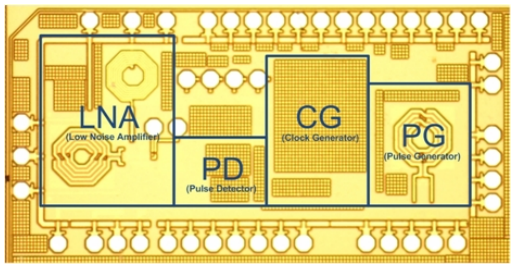


Fig. 8. Microphotograph of the fabricated chip with die size of 2.1 mm^2

The correlator and the pulse detector (including a few logic gates) together consume 20 pJ/pulse. The pulse generator consumes only 70 pJ/pulse and outputs a 1 GHz bandwidth transmitted pulse, while satisfying the FCC spectrum mask. The die size of the IR-UWB transceiver in a 0.13 um CMOS process is 2.1 mm^2, and its total power consumption is 520 pJ/pulse under a 1.2 V supply.

Acknowledgement

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