A 1.5V, 140μA CMOS Ultra-Low Power Common-Gate LNA

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***Abstract* — This paper presents design guidelines for ultra-low power Low Noise Amplifier (LNA) design by comparing input matching, gain, and noise figure (NF) characteristics of common-source (CS) and common-gate (CG) topologies. A current-reused ultra-low power 2.2 GHz CG LNA is proposed and implemented based on 0.18 um CMOS technology. Measurement results show 13.9 dB power gain, 5.14 dB NF, and -9.3 dBm IIP3, respectively, while dissipating 140 uA from a 1.5 V supply, which shows best figure of merit (FOM) among all published ultra-low power LNAs.**

***Index Terms* — CMOS, RF, Low Noise Amplifier (LNA), Ultra-low power, CG, CS**

I. Introduction

Lately, wireless sensor network (WSN) has been deployed rapidly for various military and civilian applications. Communication between sensor nodes in a sensor network is accomplished through wireless transceivers which operate by battery. With respect to sensor nodes sustaining longer life time with limited battery capacity, the implementation of ultra-low power RFICs is an important technical issue, since most of the transceiver powers are dissipated by the RF front-end. As a key block in the RF front-end, the LNA design involves demanding challenges to satisfy the low noise figure, reasonable gain and high linearity while dissipating as little power as possible.

Typical LNAs adopt CS or cascode topologies with inductive degeneration while dissipating power in a range of a few milli-ampere, considering input matching, noise figure, and linearity [1]. The CG topology has not been widely applied due to poor noise and gain performances [2], [3]. However, CG is known to be able to provide better noise performance than that of the CS topology as operating frequencies approach to the cut-off frequency [4]. With ultra-low power RF LNA design, where, the transistors tend to operate close to the subthreshold region, the operating frequency can also approach the cut-off frequency. This work proposes new design guidelines for ultra-low power LNA design by comparing the input matching, gain, and noise figure of CS and CG topologies.

In this paper, in Section II, in order to illustrate the potential of CS and CG amplifiers for ultra-low power LNA design, analysis and comparison of the two topologies are presented in terms of input matching, gain and noise figure. Based on this, in Section III, a current-reused ultra-low power CG LNA topology is proposed and implemented in 0.18 um CMOS technology. Section IV provides measurement results and Section V concludes.

II. Topology Analysis And Comparison

In general, the CS or the cascode topology is widely implemented LNA topology in terms of gain and noise figure. However, in contraction with common understanding, under near weak inversion, sub-milli-ampere operation, or at frequencies where the operating frequency is no longer substantially lower than the cut-off frequency of the MOSFET, the CG topology achieves better noise performance. In order to fully exploit both CS and CG amplifiers for low power design, analysis and comparison between CS and CG are presented in this section in terms of input matching, gain, and noise.

A. Input Matching Aspect

Fig. 1 shows the equivalent small-signal circuit of CS and CG stages looking from the input. The CS topology is a serial RLC tank while the CG topology is a parallel RLC tank. The Q-factor of the tank can be derived as follows:

$$Q_{CS} = \frac{1}{\omega R_{in} C_{gs}} = \frac{1}{\omega R_s C_{gs}} \quad (1)$$

$$Q_{CG} = \omega \frac{1}{g_m} C_{gs} = \omega R_s C_{gs} \quad (2)$$

where ω is the operating frequency, R_{in} is the input impedance real term, C_{gs} is the gate to source capacitance, R_s is the source impedance, and g_m is the device transconductance, respectively.

From the above equations, the working frequency ω is specified by application and R_s is determined by the transmission line impedance; thus the only parameter that remains free to engineer is the C_{gs} value. Two methods can be employed to adjust C_{gs}: (i) changing the transistor size and (ii) shunting an extra capacitor between gate and source, and then adjusting the equivalent C_{gs} value.

Substitute typical values into (1) and (2). With an operating frequency of 2 GHz, R_s 50, and C_{gs} 50 fF, $Q_{L\text{-}CS}$

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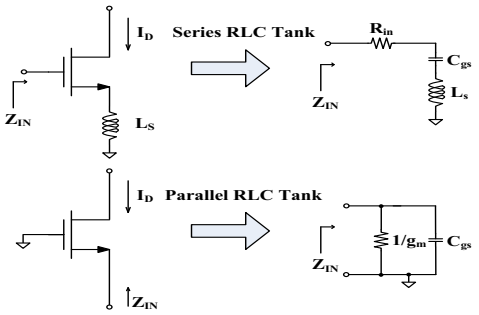

Fig. 1. Equivalent small-signal circuit of CS and CG amplifiers.

is 32 while $Q_{L\text{-}CG}$ is only $3.1\text{x}10^{-2}$. The large value of $Q_{L\text{-}CS}$ reflects the narrowband input matching characteristic of the CS topology while the small value of $Q_{L\text{-}CG}$ reflects the broadband input matching characteristic of the CG topology.

B. Gain Aspect

In order to evaluate the gain, the effective transconductance (G_m) value is taken as a criterion. The following equations of G_m are derived assuming the input matching condition is achieved.

$$G_{m-CS} = \frac{i_d}{V_S} = \frac{\omega_T}{\omega} \cdot \frac{1}{2R_S} \tag{3}$$

$$G_{m-CG} = \frac{i_d}{V_S} = \frac{1}{2R_S} \tag{4}$$

$$\omega_T \propto \frac{V_{GS}}{L^2} \tag{5}$$

Where i_d is the drain current of the input transistor and V_S is the input source voltage. From (3) and (4), $G_{m\text{-}CG}$ is lower than $G_{m\text{-}CS}$ by a factor of (ω_T/ω). However, in the low power domain, this (ω_T/ω) ratio is no longer large, and thus the gain difference between CG and CS is reduced in the low power regime. Equation (5) shows the relationship of ω_T for a long channel CMOS device. Even with submicron transistors, (5) still holds since transistors are biased in low power condition where short channel effect does not appear.

Equation (3) indicates that the only way to enhance the gain of the CS amplifier is through ω_T. Therefore, high gate biasing V_{GS} is preferred since the smallest channel length is always chosen by convention. With a fixed current budget, which is the case for most designs, higher gate biasing is interpreted as smaller transistor size. From a gain aspect, the CS amplifier requires smaller transistor size for higher gain. However, smaller transistor size enhances achievable gain while imposing a higher requirement on the Q-factor of the input matching network. This gain versus input matching trade-off is inherent with CS LNA design. With a normal power budget, this trade-off can be balanced by sacrificing either the gain or input matching. However, with a low power budget, it is difficult to balance this trade-off, since neither the gain nor the input matching network has sufficient margin for sacrifice, thus leading to complicated low power CS LNA design. As for the CG counterpart, the gain and input matching present less of a trade-off, even in the ultra-low power domain. Therefore, low power CG LNA design is more effective than low power CS LNA design.

C. Noise Figure Aspect

A simplified noise model that includes channel thermal noise and gate induced noise is adopted for the noise analysis [2].

A CS topology with source inductive degeneration has become very popular in low noise amplifier design as it provides the lowest achievable noise figure (NF) and achieves noise and power matching simultaneously [2] [3]. Meanwhile, for the CG topology, the noise boundary of $1+\gamma/\alpha$ is too high compared with that of the CS counterpart. However, in the low power regime, the CG topology may yield comparable, if not better, noise performance to that of the CS topology.

In the low power region, the minimum achievable noise figure NF_{min} of the CS LNA increases rapidly while that of the CG LNA remains almost constant. Referring to published papers [2] [5], the noise factor (F) of the CS and CG LNAs are as follows:

$$F_{\min-CS} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1-|c|^2)} \tag{6}$$

$$F_{\min-CG} \approx 1 + \frac{\gamma}{\alpha} \tag{7}$$

where γ is the coefficient of channel thermal noise, δ is the coefficient of gate induced noise, c is the correlation coefficient between channel thermal noise and gate induced noise, and α is the ratio between device g_m and zero-bias drain conductance g_{d0}, respectively.

Equation (6) shows that the minimum noise factor F_{min} of CS is a linear function of the (ω/ω_T) ratio and (7) indicates that F_{min} of CG is a much weaker function of (ω/ω_T) ratio. Published results [4] [5] have proven that as the working frequency ω approaches the cut-off frequency ω_T, i.e., the (ω/ω_T) ratio increases, the CG topology can provide better noise performance than the CS. The same principle can be applied to low power LNA design. In the low power domain, where gate biasing is not high, the cut-off frequency is inherently low. Therefore, the noise superiority of the CS LNA over CG LNA no longer holds in low power design.

D. Summary

From the foregoing topology analysis and comparison, it seen that the CG provides a broader and less sensitive

input matching network than the CS does while the gain of CG is lower than that of CS. CG also achieves better noise performance than CS does. Thus, in the ultra-low power domain, the CG topology is applicable for noise limited design while the CS topology is suitable for noise-relaxed high gain application.

III. Circuit Design

Fig. 2 shows the proposed ultra-low power current-reused common-gate LNA design and a buffer is added for measurement. This topology adopts current-reusing which is realized by four diode-connected common-gate units in one current branch, leading to an ultra-low power design.

Four advantages arise from this topology. First, no bias circuit is needed. Four transistors (M_0-M_3) are diode-connected from DC wise, saving the biasing circuit. In addition, instead of a resistor divider, a capacitor divider (C_1 and C_2) is adopted, leading to no current consumption.

Second, low supply voltage is available. The threshold voltage of the MOS transistors is reduced by using forward body biasing. In order to accommodate four stacks of transistors in a 1.5 V supply in 0.18 um technology, a forward body biasing technique is used, wherein the body terminal of each transistor is not connected to the corresponding source terminal but to lower (PMOS) or to higher (NMOS) voltage levels. The body of the bottom PMOS transistor M_0 is connected to ground and that of the top NMOS transistor M_3 to VDD. The body terminals of transistors M_1 and M_2 are connected to half of VDD.

Third, no inductor or current source is required for input matching, reducing both chip size and noise. In the conventional CG LNA design, either a large size inductor or a current source is needed at the input as an AC choke, which consumes a considerable amount of chip size and degrades noise performance. However, in the proposed current-reused CG LNA, where the input signal is only injected to the input terminals, no AC choke is required, thus resolving the problems brought about by the AC choke. With proper selection of transistor size, the input is self-matched to R_S; no other matching network is needed.

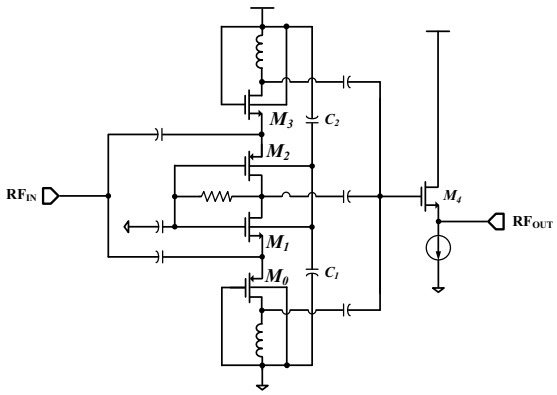

Fig. 2. Proposed current-reused common-gate LNA.

Last, ultra-low power design can be realized. From small-signal perspective, the proposed LNA is a parallel combination of four CG units. Therefore, the total g_m value is four times higher. The circuit draws only 140 uA current from a 1.5 V supply.

IV. Measurement Results

The proposed ultra-low power current-reused CG LNA is implemented in 0.18μm CMOS technology. Fig. 3 shows a die photograph of the chip, which is about 1x1.5 mm^2. The current and IIP3 of the proposed current-reused CG LNA is measured according to the supply voltages. Fig. 4 shows the current consumption and IIP3 of the proposed LNA at various supply voltages ranging from 1.5 to 1.8 V. The proposed LNA only draws 140 uA current and -9.3 dBm IIP3 from a 1.5 V supply. Fig. 5 and Fig. 6 present the measured S-parameter of the proposed LNA. From Fig. 5, S11 is less than -10 dB in a frequency range from 1 to 3 GHz. Fig. 6 shows a peak gain of 13.9 dB at a 1.5 V supply. Fig. 7 shows the measured NF of the proposed LNA. NF at 2.2 GHz is about 5.14 dB from a 1.5 V supply.

In Table I, the performance of the proposed LNA is compared to that of previously reported LNAs. From Table I, in the ultra-low power domain the gain superiority of CS over CG is no longer significant and the CG topology can provide a lower noise figure. Considering the better isolation and broadband input

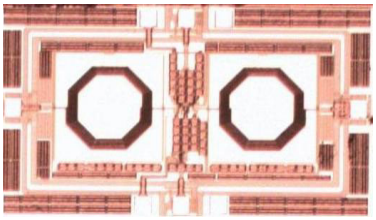

Fig. 3. Chip photograph.

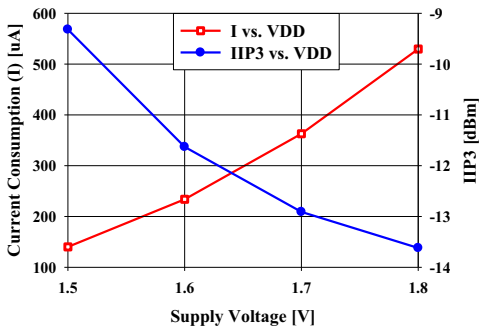

Fig. 4. Measured I and IIP3 versus supply voltages.

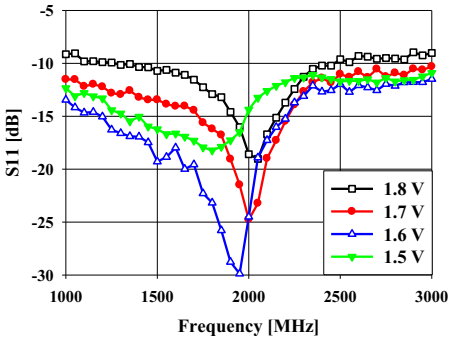

Fig. 5. Measured S11.

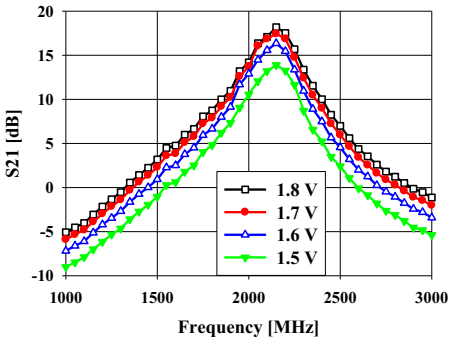

Fig. 6. Measured S21.

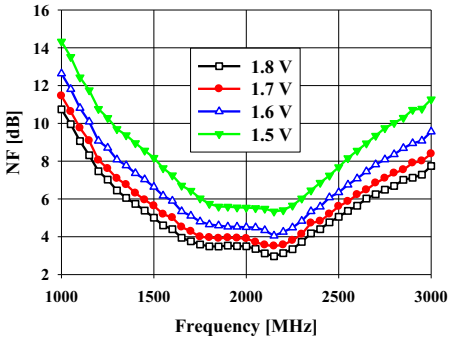

Fig. 7. Measured NF.

TABLE I
SUMMARY OF PERFORMANCE OF ULTRA-LOW POWER LNA

	This Work				[7]	[8]	[9]
Supply [V]	1.8	1.7	1.6	1.5	0.6	0.4	1.2
Power [uW]	954	612	374	210	156	1030	720
Freq. [GHz]	2.2	2.2	2.2	2.2	3	5.1	0.1~0.9
Gain [dB]	18.2	17.4	16.4	13.9	4.5	10.3	13
NF [dB]	2.97	3.41	4.05	5.14	6.3	5.3	4
IIP3 [dBm]	-13.6	-12.9	-11.6	-9.3	-10.5	-12	-10.2
Tech [um]	0.18				0.13	0.13	0.13
Topology	CG				CS	CS	CG
FOM	0.83	1.15	1.74	2.68	0.88	0.43	0.35

* $FOM = \frac{Gain[abs] \cdot IIP3[mW] \cdot F[GHz]}{(NF-1)[abs] \cdot PD[uW]}$ [6]

matching property provided by the CG topology, it appears to be a better choice for ultra-low power LNA design. The proposed LNA shows the best FOM [6] when compared with the previously reported low power LNAs.

V. CONCLUSION

Two well-known LNA topologies, the CS and CG topologies have been analyzed and compared in terms of input matching, gain, and noise. In the ultra-low power domain, the CG topology provides better input matching and noise performances than the CS topology with similar gain performance. This paper presents an ultra-low power CG LNA design for WSN application. By adopting current-reused self biasing and forward body biasing techniques, the ultra-low power LNA design can be achieved. The measurement results show 1 to 3 GHz wide input matching, a 13.9 dB peak gain, 5.14 dB NF and -9.8 dBm IIP3 while consuming 140 uA from a 1.5 V supply, which shows best FOM among all published ultra-low power LNAs.

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