A Wide-band CMOS Low Noise Amplifier for LTE Application

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Abstract— **In this work, a wide band LNA for implementation in Long Term Evolution (LTE) systems is presented. A common gate amplifier with active noise cancellation is adopted to provide wide band input matching and a low noise figure (NF). To mitigate parastics and obtain improved noise performance, an inner-cascode inductor is added. The inter-cascode inductor also allows for bandwidth extension without significant peaking in the frequency response with voltage gain 17.3dB. The proposed LNA is designed in 0.18 um CMOS technology. From post-layout simulations, the design consumes 9.5 mA from a 1.8 V supply and operates in the frequency range of 0.7-2.7 GHz. The simulations also show S_{11}<-10, a 2dB NF, and an IIP3 of approximately 5 dBm.**

Keywords - CMOS receiver, wideband, low noise, transimpedance, mobile communication

1 Introduction

Long Term Evolution (LTE) is the next standard mobile communication technology. LTE is specified by the 3GPP syndicate and is the integration of the existing cellular infrastructures for 2G and 3Gstandards. It achieves full connectivity with previous standards. LTE utilizes a frequency range of 0.7 – 2.7GHz to support frequency division duplexing (FDD), time-division duplexing (TDD), and a wide range of system bandwidths.

Receiver design is one of the most challenging aspects in the implementation of LTE networks. The LNA is the first block of the receiver and has to cover the entire LTE band. In addition, it must provide high linearity, low noise figure (NF), and a reasonably flat gain for the entire bandwidth. Furthermore, the maximum power consumption for a given application often limits the NF and linearity of an LNA. Wide band input matching further complicates the design. Most known methods for providing wide band input matching employ the common gate (CG) topology [1]. However, a CG amplifier suffers from poor noise performance because of limitations on g_m, typically resulting in a NF below 3dB [2]. The capacitive cross coupling (CCC) technique can be used to alleviate this issue [3]. However, the noise contribution of the input stage often remains unacceptably high. In addition, the CCC scheme modifies the input impedance, changing it from $1/g_m$ to $1/(2g_m)$. As a result, the transconductance must be reduced to maintain input matching, thereby degrading the minimum achievable NF.

This paper presents a wideband, CCC LNA that employs active noise cancellation as well as inter-cascode inductors to achieve input matching while providing a low NF. The added inductors also extend the bandwidth of the LNA by resonating out parasitic capacitances.

The result of the paper is organized as follows. Section 2 briefly reviews recent works in wideband, LNA design. The proposed design is presented in Section 3 with simulation results given in Section 4. Conclusions are discussed in Section 5.

2 Review of existing wide band LNA techniques

The CG configuration is often employed to achieve wideband input matching. Fig.1 shows CG LNA that utilizes series peaking for bandwidth extension. The input impedance of the CG LNA is g_m^{-1}. The noise sources in Fig.1 are the channel noise of M_1 [4] and the thermal noise of the output resistor R_D. The resulting noise contributions lead to noise figure in excess of 3.6dB. To reduce the NF, active noise cancelling techniques are often utilized. A traditional noise canceling structure is shown in Fig.2 [5]. Note that the input impedance is unaltered and equal to g_m^{-1}. The channel noise of M_1 induces voltage with opposite polarity at its drain and source. M_2 and M_3 convert the drain and source voltages to currents, which sum at the output. As a result, the channel noise is greatly attenuated with appropriate choice of R_{D1} and device size. However, the added components lead to high power consumption and poor linearity compared to the simple, CG structure. While distortion cancellation schemes can be implemented to improve linearity [6], both power consumption and circuit complexity increase.

3 Proposed circuit

Fig. 2 shows the schematic of the proposed design. The PMOS devices, M_5 and M_6 increase the transconductance, g_m of the CG stage by sourcing additional bias current to M_1 and M_2. Noise cancellation is also achieved by AC coupling the input signal to the gates of M_3 and M_4 [7]. Since the NF reduces with increases in g_m and added noise cancellation, the proposed design exploits two techniques for improving noise performance. However, the increased transconductance of the input stage modifies the input resistance of the LNA. The added transistor also introduce parasitic capacitances, which

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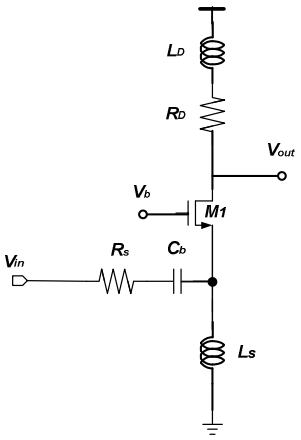
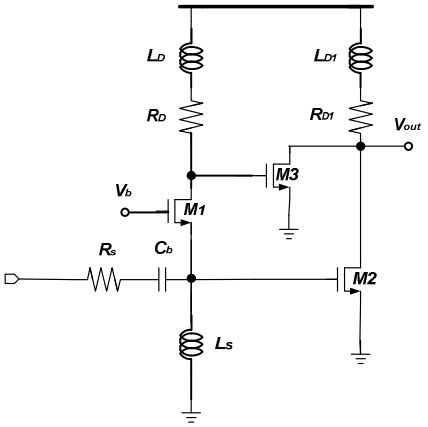


(a)



(b)

Fig. 1. (a) Common gate LNA, (b) conventional noise cancellation technique [4] [5]

have deleterious effects on the frequency response of the design. To alleviate these issues, inter-cascode inductors, L_{int} are included as depicted in Fig. 2. The influence of these inductors on the input impedance is discussed next.

The input impedance of the proposed LNA is given by:

$$Z_{in} = \frac{1}{g_{m1,2}}\left[1 + \frac{Z_{eq}}{r_{ds1,2}}\right] \quad (1)$$

where $g_{m1,2}$ is the transconductance and $r_{ds1,2}$ is the incremental resistance of M_1 and M_2, and Z_{eq} is the equivalent impedance seen at the a higher transconductance than the CG configuration, $g_{m1,2}$ can be expressed as:

$$g_{m1,2} = x g_m \quad (2)$$

where x is greater than unity and g_m denotes the required trasconductance for matching in the typical CG configuration. i.e.: $R_{inMatch} = \frac{1}{g_m}$. (1) can now be written as:

$$Z_{in} = \frac{R_{inMatch}}{x}\left[1 + \frac{Z_{eq}}{r_{ds1,2}}\right] \quad (3)$$

From (3), matching is now accomplished when $1 + \frac{Z_{eq}}{r_{ds1,2}} = x$. The inter-cascode inductor and the parasitic capacitances of $M_{1,2}$ and $M_{5,6}$ form an L-match that, at resonance, transforms the low, source resistance of the cascade device, $M_{3,4}$ to a much larger resistance. Z_{eq} is then given by:

$$Z_{eq} = \frac{1}{g_{m3,4}}(1 + Q^2) \quad (4)$$

where $g_{m3,4}$ is the trasconductance of the cascode devices, M_3 and M_4, and $Q = \omega L_{int} g_{m3,4}$. The inductance, L_{int} is then appropriately selected such that the resulting Z_{eq} results in $Z_{in} = R_{inMatch}$.

In addition to acquiring better input matching and improving noise performance, simulations show that the added inductors extend the LNA's bandwidth, while exhibiting a flat gain response over a wide band of frequencies. However, further work is required to quantify these results.

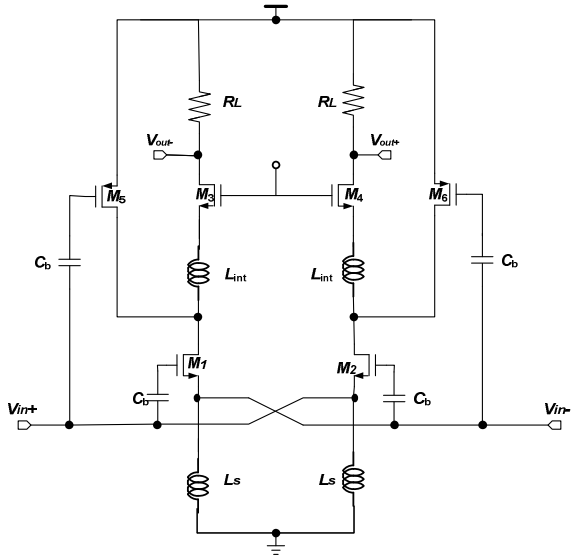


Fig. 2. A Circuit schematic of the proposed LNA.

4 Simulation results

A Wide-band CMOS LNA is simulated with Cadence Spectre RF using a 0.18µm RF-CMOS process design kit (PDK). The design is targeted to achieve low NF and power consumption over a wide 3dB bandwidth (0.7 to 2.7GHz).

Fig. 3 shows the simulated voltage gain and reflection coefficient, S_{11}, of the proposed LNA. The gain response is flat and remains at approximately 17.3 dB from 0.5 to 3.5 GHz. The proposed LNA achieves S_{11} < -10dB over the 0.4~3.6GHz bandwidth, thereby validating input matching.

As discussed in the previous section, $g_{m1,2}$ is x times larger than the transconductance of a typical, CG LNA. In the simulated design, x is approximately 3. Fig. 4 shows the simulated IIP3 and NF of the design. Due to the increased transconductance, the simulated NF is approximately 2dB, as shown in Fig.4. Fig. 4 also shows that the IIP3 lies within the range of +5.2~+8.84dBm.

Table 1 compares the performance of the proposed LNA and the design published in [1] [2] [7]. The proposed design shows substantial improvements in both NF and linearity.

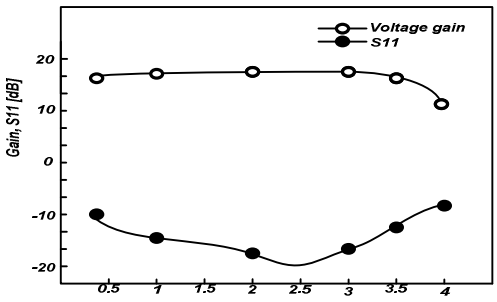


Fig. 3. Simulated Voltage gain and S11 of LNAs

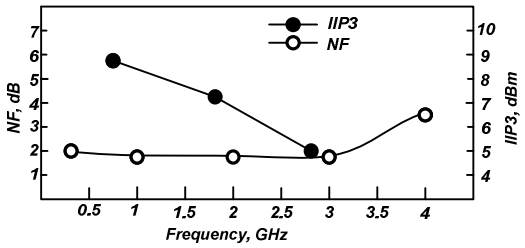


Fig. 4. Simulated IIP3 and NF of LNAs

Table 1. Performance comparison of proposed LNA with [4]

LNA	Technology CMOS(um)	BW (GHz)	A_v (dB)	NF (dB)	IIP3 (dBm)	V_{DD} (V)	Power mW
[1]	0.18	0.4~10	18.4	4.4~6.5	-6	1.8	12
[2]	0.18	2~6.5	17	2.5~2.7	3.4~5.4	1.8	4.6
[7]	0.09	0.5~3	20.1	2.32~2.87	-4.5~-1	1	5.5
This work	0.18	0.7~2.7	17.3	1.9~2	5.2~8.84	1.8	17

5 Conclusion

The proposed LNA is capable of working in various next generation standards like LTE/GSM, WiMAX and IEEE 802.11 family. It is also suitable for single chip, next generation radio solutions with low cost and low power consumption. The LNA, which operates from 0.7 to 2.7 GHz, is designed in 0.18µm CMOS technology. Inter-cascade inductors are used to achieve input matching and bandwidth extension without degrading performance in terms of noise figure. The simulated NF is approximately 2dB and S_{11}< -10. The voltage gain is about 17.3dB while the IIP3 is +5.2~+8.84dBm. The simulated current consumption is 9.5mA from a 1.8V supply.

Acknowledgment

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