A Low Power Discrete-Time Receiver for Triple-Band FM/T-DMB/DAB System-on-Chip

Hoai-Nam Nguyen[1], Seung-Hwan Jung[2], Byung-Hun Min[3], Young-Jae Lee[3],
Sang-Gug Lee[1], Yun-Seong Eo[2], and Huyn-Kyu Yu[3]
[1]Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea
[2]Kwangwoon University (KWU), Seoul, Korea
[3]Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea

***Abstract*— This paper presents a low power discrete-time receiver supporting three broadcast services FM, T-DMB and DAB. To meet the requirement of sensitivity, three LNAs are implemented to cover each band. The proposed mixer core is terminated by a common-gate current buffer to improve linearity and merged with a switched-capacitor sampled filter in current mode for low power and low complexity. The filter performs the second-order low-pass filtering with anti-aliasing ratio up to 70 dB at 1.6 MHz bandwidth. The chip is fabricated in a 90 nm CMOS technology and dissipates 11 mA current from 1.2 V supply. The receiver shows 48 dB maximum gain, 60 dB gain control range, 2.7 dB noise figure, and -22/0 dBm IIP3 in LNA high/low gain mode.**

I. INTRODUCTION

In recent years, multimedia broadcasting standards such as DVB-H, ISDB-T, T-DMB, DAB and FM are widely used. To support various applications, the multi-standard multi-band RF tuners are developed considering power, cost and size efficiencies with zero-/low-IF architectures [1, 2]. Mobile TV system-on-chip (SoC) approach further increases the level of integration and functionality by integrating the RF tuner, ADC, baseband demodulator into a single chip [3, 4]. The multi-standard multi-band TV SoC design reported in [4] achieves a significant reduction in chip area and power consumption by doing baseband processing tasks which include channel selection, image rejection filtering and DC offset cancellation in digital domain.

An earlier demonstration of radio SoC is introduced based on discrete-time analog signal processing [5]. In [5], the RF input signal is down converted to baseband by a RF charge sampler at carrier frequency sampling rate. The following decimation filter performs channel selection by discrete-time (DT) IIR/FIR filtering and down-converts the sampling rate to a feasible speed for low power ADC designs. Compared to the continuous-time (CT) signal processing, the DT counterpart has advantages with technology scaling and SoC integration in the robustness to process, voltage and temperature variations.

Although RF sampling receivers reported in [5, 6] simplify analog building blocks, they increase the complexity of DT baseband processing and digital front-end (DFE) due to the frequency-dependence of filtering characteristic when they are applied in multi-band multi-standard contexts. Those receivers require dedicated variable decimation rate FIR filter in pre-ADC signal conditioning [6] and re-sampling process in DFE [5]. In order to tolerate this disadvantage, DT receivers based on baseband charge samplers are presented with LO-independent sampling frequencies [7, 8]. However, those DT receivers still have high complexity in analog designs that demands implementation efforts when CMOS technology is scaled down to improve digital processing performances.

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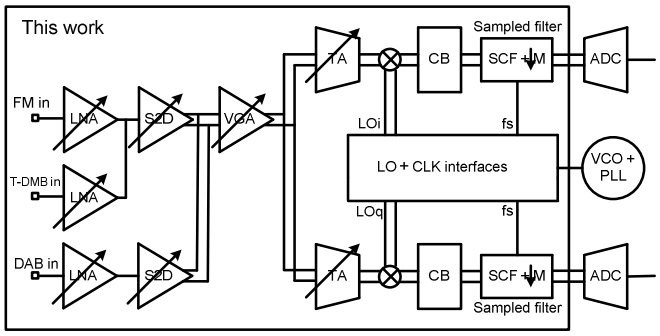

Figure 1. Block diagram of the triple band discrete-time receiver.

This paper proposes a triple-band DT receiver based on merging of the mixer and baseband switched-capacitor filter in current mode for FM/T-DMB/DAB applications. Direct conversion architecture is adopted for T-DMB and DAB standards, while low-IF architecture is chosen for FM reception to avoid the effects of flicker noise and DC offset.

II. ARCHITECTURE AND CIRCUIT DESIGNS

The proposed discrete-time receiver architecture is shown in Figure 1. The receiver consists of a triple band RF front-end (LNA+S2D+VGA), current commutating passive mixers, current buffers (CB), and baseband switched-capacitor filters (SCF) with an LO+Clock interface. RF input signal is amplified by the variable gain RF front-end and down-converted by the quadrature mixer with output current buffer. Then, baseband/IF current is sampled and lowpass filtered by the SCF with built-in anti-aliasing and high linearity characteristics before analog-to-digital conversion.

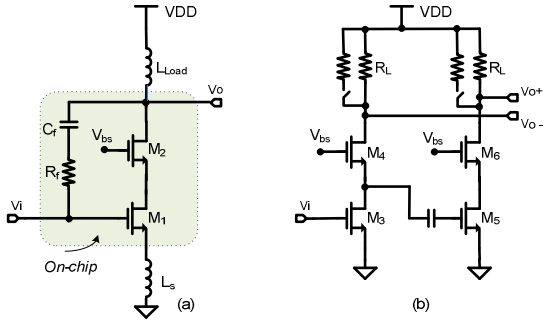

Figure 2. Simplified schematic of LNA (a) and S2D (b).

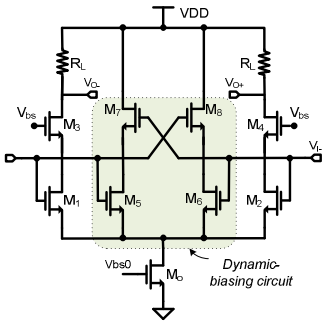

Figure 3. Dynamic biasing RF VGA cell.

A. *Triple-Band RF Front-End*

The RF front-end consists of three LNAs designed to optimize sensitivity performances and suppress out-of-band and harmonic mixing interferences for each operating band. Single-to-differential (S2D) conversion is performed after the LNAs to protect the following stages from common-mode and supply noises. Figure 2 shows the simplified schematic of the LNAs and S2Ds. The LNAs adopt the inductive source degeneration and resistive feedback topology to achieve sub-2dB NF in wide frequency band [9]; the S2Ds circuit use CG-CS topology for a low noise figure.

Since the mobile broadcasting standards define various test patterns of interferences besides wide input power ranges, the receiver requires a gain control to prevent the circuits from saturation and distortion. Therefore, the LNAs are designed with 21 and 0 dB of high gain and low gain, respectively, by adopting bypass switches [10]. The S2Ds have two gain modes of 10 and 7 dB for the overall RF gain step of 3 dB.

A high/low band reconfigurable RF variable gain amplifier (VGA) in combination with gain control of LNAs and S2Ds provide wide dynamic ranges for the receiver and relax linearity requirement of flowing stages. The capacitive divider-based VGA architecture similar to that in [10] is adopted for good noise performance. The VGA is designed for the gain range of -18 to 0 dB with 6 dB step by 2-bit control. Since the LNAs and S2Ds provide high gain for low NF, the VGA is also considered in term of linearity. The dynamic biasing linearization technique presented in [11] is adopted for RF VGA cell with cascoded loading, as shown in Figure 3; therefore the linearity of the VGA is improved with slight sacrifices of bandwidth and noise figure.

B. *Mixer and Switched-Capacior Filter*

Mixers in zero-/low-IF architectures must satisfy stringent requirements of flicker noise and linearity. Among various reported mixers, the current commutating passive mixer is one of the most preferred solutions for those performances [1-4].

To improve the linearity of mixer, a well-known method is adopting an opamp-based transimpedance amplifier (TIA) with low input impedance at the output of switching quad [1-4]. However, the small output impedance of the TIA shows that the mixer output behavior is voltage mode not current mode, which is required to drive a built-in anti-aliasing charge-domain SCF. In order to use the SCF, a baseband transconductance amplifier (TA) is needed, which leads to additional power consumption and chip area to the design.

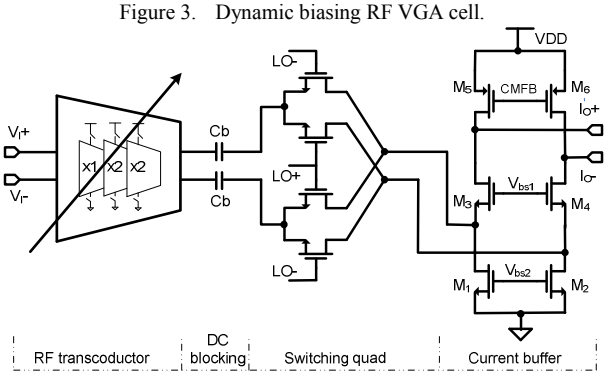

Figure 4. Proposed mixer with current buffer.

For the purpose of low input impedance, the common gate (CG) TIA can be utilized with biasing and loading resistors [8]. This solution has advantages of compact implementation and eliminating the common-mode feedback circuitry; however it requires a high voltage supply due to the large voltage headroom dropped on resistors to obtain a high conversion gain to archive low noise performance. In addition, this CG amplifier shows a moderate output impedance or current driving capability; therefore if merged with the SCF, the circuit shows limited performances in conversion gain, noise, linearity and anti-aliasing rejection since the current mode operation is no longer guaranteed.

Figure 4 shows the proposed mixer to address the afore-mentioned issues. As can be seen from Figure 4, the mixer consists of an RF transconductor, a switching quad with DC blocking capacitors and a current buffer. In order to reduce flicker noise of the mixer, the transistors in the current buffer is sized with large enough channel length. The channel width of the CG transistors is also increased to achieve low input impedance with minimum current consumption. The output impedance of the CG current buffer is the parallel combination of the boosted output resistance of the NMOS CG amplifier and the intrinsic resistance of the PMOS current source load. Therefore, the proposed mixer core obtains a high output impedance to maximize the driving current. Moreover, the increase in channel length reduces the channel length modulation effect that benefits the high output impedance of the CG current buffer. The simulation shows that, with 380 µA current in each CG branch from 1.2 V supply and 1.5 µm channel length transistors, the CG buffer output impedance is 16 kΩ that equivalents to a 2x8-kΩ resistive load implementation with a drop voltage of 3V. This means that the proposed mixer is suitable to low voltage design.

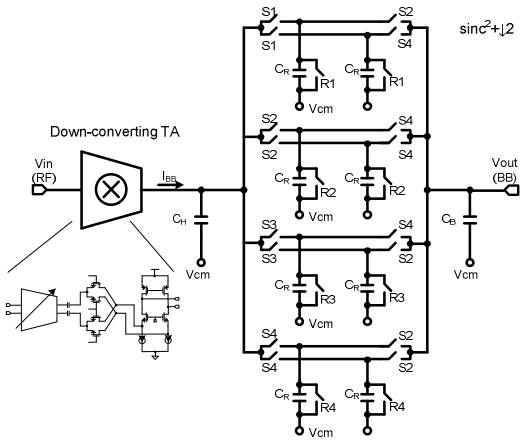

Figure 5. Charge-domain switched-capacitor filter (SCF).

The mixer with the high output impedance CG current buffer can be consider as a down-converting TA, with which the radio frequency input voltage is down-converted to the baseband current. The output current of the CG buffer directly drivers the SCF, thereby no additional baseband TA is required, which saves the chip area and power consumption.

In order to extend the dynamic range of the receiver, a 3-bit programmable RF transconductor is implemented. Based on self-bias inverter with dynamic biasing linearization presented in [11], the transconductor offers low power, low noise and high linearity to the mixer. A transconductance gain ratio of 1:2:2 can provide gain factors of 1, 2, and 4 for the 12 dB gain range with 6 dB step in typical usage. The highest gain with the factor of 5 is set for L-band to compensate the overall gain reduced at the interface between the RF VGA and transconductor to maintain the noise performance.

Figure 5 shows the single ended half-circuit of the charge-domain switched-capacitor decimation filter. The down-converted current I_{BB} is integrated into four pairs of rotating capacitors (C_R) connected to a history capacitor (C_H) building a first-order CT FIR filter (*sinc*-shape for anti-aliasing rejection) and a first order DT IIR (low-pass filter for channel selection), simultaneously. The successive samples on rotating capacitors share their charge together with a non-reset buffer capacitor (C_B) to form a DT FIR filter and another first-order DT IIR low-pass filter. The FIR coefficient of 1:2:1 provides the $sinc^2$ filtering response with the decimation rate of 2 [7].

The baseband discrete-time signal can be processed further by cascading filters and equalizers. However, based on the system calculation, the filter shown in Figure 5 satisfies required standards, which saves power and chip size. The SCF uses 3 control bits for rotating capacitors to set 3dB cut-off frequencies to be around 850 kHz for T-DMB/DAB band and 420 kHz for FM band, respectively, under the sampling frequency fs changing condition. In the design, fs is the same as f_{LO} for FM and T-DMB bands and $f_{LO}/8$ for DAB L-band.

III. Measurement Results

The proposed receiver is fabricated in a 90-nm CMOS process. The receiver, shown in Figure 6, occupies an area of 1x2mm2 including pads. The chip is wire-bonded to PCB for testing purposes.

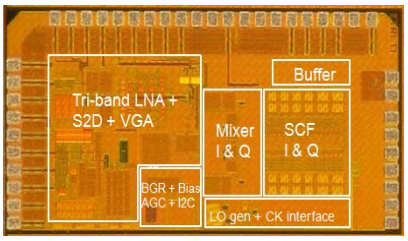

Figure 6. Chip photograph of triple band DT receiver.

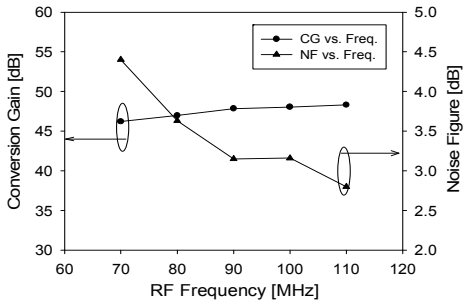

Figure 7. VHF-II (FM) band Gain and NF vs. Frequency.

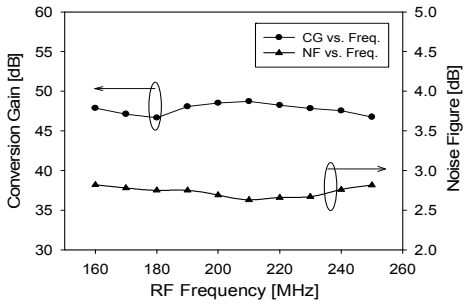

Figure 8. VHF-III (T-DMB) band Gain and NF vs. Frequency.

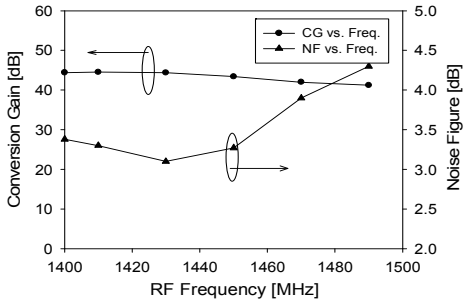

Figure 9. L- band (DAB) Gain and NF vs. Frequency.

Figures from 7 to 9 present the measured maximum voltage conversion gain and minimum NF for the three frequency bands. The conversion gains for FM/T-DMB and DAB bands are 48 and 42 dB, respectively. The shared low-band inductor load is optimized for VHF-III band of T-DMB, thus the gain is fairly flat for this band keeping the NF less than 2.8 dB. For the FM band, the LNA gain reduced at low frequencies, which causes the system NF to increase up to 4.5 dB at 70 MHz. The same effect occurs at high frequencies of L-band (DAB) but the NF still satisfy the requirement of 5 dB.

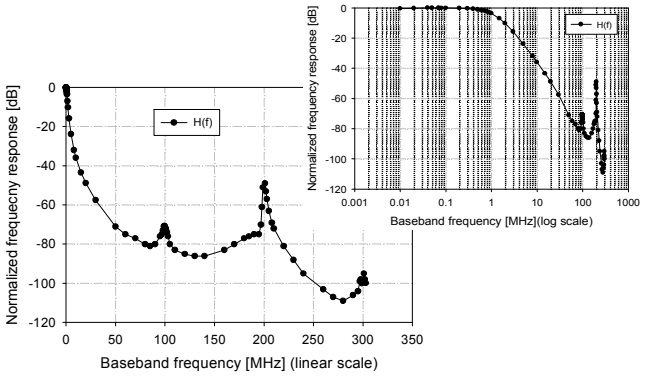

Figure 10. Baseband frequency response at f_{LO} of 200 MHz (T-DMB).

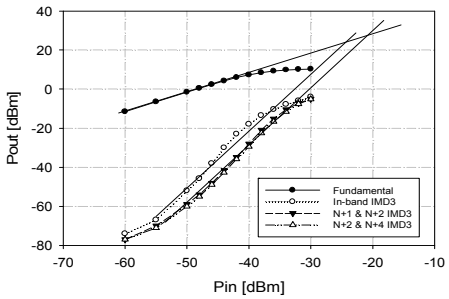

Figure 11. IIP3 test at highest gain mode at f_{LO} of 200 MHz (T-DMB).

Figure 10 shows the baseband frequency response of the down-converted signal at f_{LO} of 200 MHz of T-DMB system in linear and log scale of frequency. The CT and anti-aliasing rejection (AAR) are 50 dB at 200 MHz and AAR is 70 dB at 100 MHz, respectively.

Figure 11 illustrates the linearity performance of the receiver tested at f_{LO} of 200 MHz. At highest gain setting (48 dB), the in-band IIP3 is about -25 dBm and the out-of-band IIP3 is -22 dBm with -40 dBm interference power at N+2 and N+4 channels. The out-of-band IIP3 increases to -20 dBm in L-band because of gain drop. The OIP3 is 25±2 dBm for most frequencies.

In Table I, the measured results are summarized with those of state-of-the-art low power mobile TV receivers [4], [12]. The NF and IIP3 performances of the proposed receiver are comparable to those of [4] in FM and T-DMB bands and better NF in DAB L-band. The power consumption in this work is a half of that of the dedicated conventional design [12] and comparable to that of the analog simplified design [4], which is reported including PLL.

IV. CONCLUSION

A triple-band discrete-time receiver for FM, T-DMB and DAB applications is presented. The chip satisfies noise and linearity requirements with low power consumption. Based on merging a current commutating passive mixer with a charge domain discrete-time filter, the receiver architecture shows low power and low complexity which suitable for mobile TV applications in nano-scale CMOS technology.

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TABLE I. PERFORMANCE SUMMARY

Parameter	**Unit**	**FM**			**T-DMB**			**DAB**		
Frequency	MHz	70 - 110			170 - 250			1450 - 1490		
RF conversion gain	dB	**48**	66[a]	46.6[sim]	**48**	68[a]	44	**42**	67[a]	35.3[sim]
NF (average)	dB	**3.4**	3	1.3[sim]	**2.7**	2.8	1.5	**3.8**	7	2.7[sim]
CT/DT FIR AAR	dBc	**47/72**	-	-	**50/70**	-	-	**48/70**	-	-
IIP3 HG/LNA LG	dBm	**-22/0**	-18/-	-29/1.7	**-22/0**	-21/-	-34/0	**-20/1**	-18/-	-16/0.6
Current/Supply	mA/V	**10.6/1.2**	20[b]/1.2	18/1.2	**10.3/1.2**	20[b]/1.2	19/1.2	**11.2/1.2**	20[b]/1.2	27/1.2
CMOS technology	nm	**90**	65	130	**90**	65	130	**90**	65	130
Reference		**This work**	**[4]**	**[12]**	**This work**	**[4]**	**[12]**	**This work**	**[4]**	**[12]**

[a] including baseband PGA / [b] including PLL