26.4 An Interference-Aware 5.8GHz Wake-Up Radio for ETCS

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Wake-up radios have been a popular transceiver architecture in recent years for battery-powered applications such as wireless body area networks (WBANs) [1], wireless sensor networks (WSNs) [2,3], and even electronic toll collection systems (ETCS) [4]. The most important consideration in implementing a wake-up receiver (WuRX) is low power dissipation while maximizing sensitivity. Because of this requirement of very low power, WuRX are usually designed by a simple RF envelope detector (RFED) consisting of Schottky diodes [1,3] or MOSFETs in the weak inversion region [2] without active filtering or amplification of the input signal. Therefore, the performance of the RFED itself is critical for attaining good sensitivity of the WuRX. Moreover, the poor filtering of the input signal renders the WuRX vulnerable to interferers from nearby terminals with high transmit power such as mobile phones and WiFi devices, and this can result in false wake-ups [1]. Although the RFED has very low power, a false wake-up will increase the power consumption of the wake-up radio as it will enable the power-hungry main transceiver.

An RF SAW filter can be used in front of the RFED to reduce false wake-ups [2], but it has wider bandwidth in the GHz range and is not sufficient to reject interferers. Furthermore, its insertion loss degrades sensitivity. A narrowband BPF also can be used to remove interference after the RFED [3]. However, it is usually implemented by a passive R-C filter due to the requirement of low power, and also has poor selectivity [1,2]. To overcome these challenges of WuRX, a low-power, high-gain RFED and a low-power delay-based BPF (DBPF) that has a narrow and sharp frequency response that is sufficient to reject interferers are newly proposed in this paper. The IC reported here is a fully integrated wake-up radio for ETCS compliant with the GB/T 20851-2007 Chinese dedicated short-range communication (DSRC) standard [4].

Figure 26.4.1 shows the entire block diagram of the transceiver. The WuRX consists of an RFED, a comparator with hysteresis acting as a 1b ADC, and a DBPF. The RX path is similar to that of the WuRX except for the implementation of a front-end low-noise amplifier (LNA) to increase the sensitivity, and the input ports of the WuRX and RX are shared to allow a single antenna. An external 1:N balun transformer is used to maximize the gain of the RFED at a given current consumption. A switching PA-based polar transmitter that was reported in our previous work [6] is adopted, optimizing the performance for the Chinese ETCS. A fractional-N PLL and an ASK baseband processor which consists of a modulation index control (MIC), a 3rd-order Gaussian pulse-shaping filter (PSF), and a programmable-gain amplifier (PGA) are included. The downlink signal of the Chinese ETCS consists of a wake-up pattern including 15 to 17 cycles of 14kHz square waves and a normal frame encoded by the 256kb/s FM0 method. The WuRX should provide an interrupt signal to the modem part in response to the wake-up pattern to enable the Rx to receive the normal frame. If there are AM interferers such as *fcarrier2* and *fcarrier3*, as shown in Fig. 26.4.1, the resulting baseband envelope signals *fmod2* and *fmod3* converted by the RFED will be removed by the DBPF. Therefore, the DBPF reduces the possibility of false wake-ups significantly.

The circuit schematic of the RFED is shown in Fig. 26.4.2. A pseudo-differential amplitude detector [5] is used for the RFED. To increase the RFED gain, a 1:N external balun transformer, X1, is used, and the input transistors M1 and M2 are cross-coupled through the coupling capacitors C2 and C3. C1 is used to match the impedance between the transformer and the IC input. The load consists of R3 and C4 to remove high frequency components. M3 and C5 stabilize the DC operating point, and the diode-connected M4 is used to increase the dynamic range of the RFED. From these configurations, the proposed RFED shows an approximately $4N^2$-fold increase in gain compare to a simple pseudo-differential circuit. The detected envelope signal is fed to the dynamic referenced comparator by R4 and C6 to generate digital bit streams. The noise signals from the RFED and the comparator itself are limited by the hysteresis voltage, V_{HYST}.

Figure 26.4.3 shows the DBPF block diagram, where the DBPF consists of an LPF and an HPF. The HPF consists of a counter and periodic counter-reset (PCR) circuit synchronized to the incoming clock. PCR charges capacitor C1 at the rising edge of *clkin* through M1, and discharges at the falling edge of *clkin* with a time constant of R1C1. Therefore, low frequency signals in comparison with the time constant of the PCR circuit will be removed by the initializing operation of the counter. The LPF is based on three state machines, which have four unique logic states, s1, s2, s3, and s4, respectively, defined by the incoming clock (*clkin*) and its delayed one (*clkdly*). The cut-off frequency is $1/(2td)$, and *td* is the time delay of the N-stage delay cell. A conventional edge detector, DFFs, and logic gates are used to construct the whole state machine. The output of the state machine gates the *clkin* to the output, and an 8-stage delay cell is used in this design to reject frequency components higher than the cut-off frequency.

The frequency response of each state machine is shown in Fig. 26.4.4. The first state machine uses a *td*-delayed clock, *clkdly*, and has a periodic frequency response with a period of $1/td$, as shown in Fig. 26.4.4-(a). To remove the periodic frequency response, a half-delayed clock, *clkdly2*, and a quarter-delayed clock, *clkdly4*, are used. The delay cell is bandwidth limited, and it also acts as an LPF to remove signals higher than $4/td$. Although the second and third state machines also have periodic frequency of $2/td$ and $4/td$ respectively, the composite frequency response is nearly the same as that of an ideal LPF, as shown in Fig. 26.4.4-(d). Figure 24.4.4-(e) shows the measured frequency response of the WuRX. The WuRX using only passive R-C filters has 3dB bandwidth of about 50kHz. However, it cannot reject interferers sufficiently due to its gradual frequency response. On the other hand, the WuRX with the DBPF has a narrow and abrupt frequency characteristic with bandwidth of about 28kHz. The proposed DBPF has narrow bandwidth and rejects the out-of-band signal completely. Therefore, it can reduce the false wake-up operation more effectively. In addition to good filtering performance, it also has very low standby current consumption, because the DBPF consists of standard logic gates and passive devices. The DBPF dissipates only the static leakage currents of the logic gates when there is no wake-up signal in the air.

The measurement results of the IC are shown in Fig. 26.4.5. The sensitivity of the WuRX is about -45dBm based on 40% to 60% duty, and the dynamic range is about 45dB. The RX sensitivity is about -60dBm and the dynamic range is about 60dB. The limiting transistor M4 in Fig. 26.4.2 increases the dynamic range of both WuRX and RX dramatically. The peak power of the ASK modulated output is about +5dBm, and the ACPR is about -53dBc.

Figure 26.4.6 summarizes the measured results. As there is no prior published work to date, the performance requirements [4] of the standard document are used to compare the total performance of the IC. The operating frequency is 5.8GHz, and the operating current of WuRX, RX, and TX are 15uA, 19mA, and 40mA respectively. A micrograph of the transceiver IC that is implemented in a 1P6M 0.13μm RF CMOS process is shown in Fig. 26.4.7, and the chip size is 1.70x1.65mm^2. The measured performance indicates that this transceiver IC meets all the requirement of the standard sufficiently, and is suitable for the Chinese ETCS.

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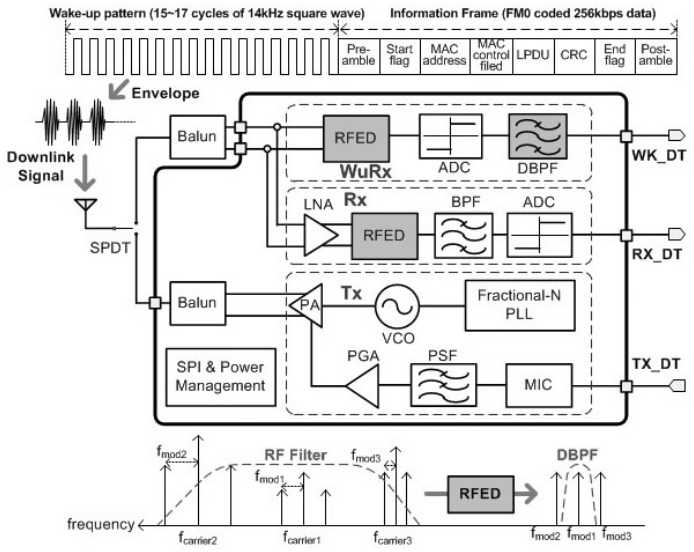

Figure 26.4.1: Transceiver block diagram.

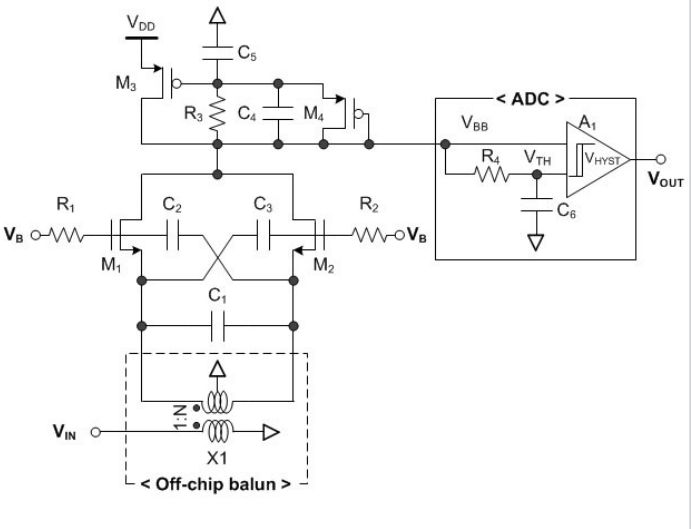

Figure 26.4.2: Circuit schematic of the RF envelope detector.

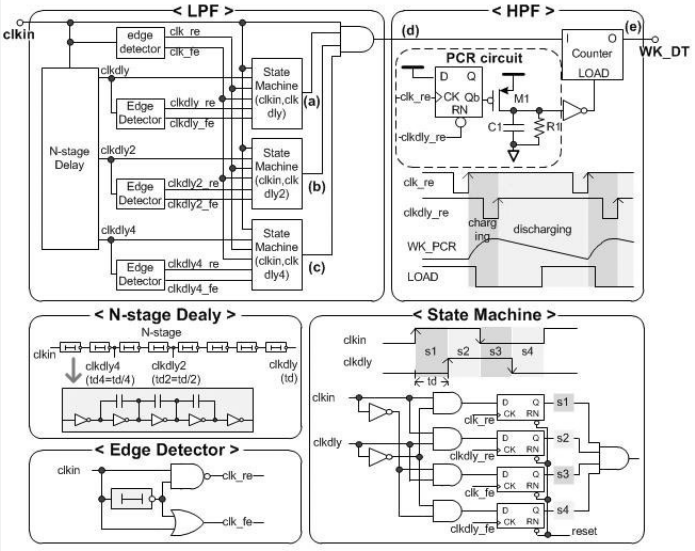

Figure 26.4.3: Block diagram of the delay-based BPF (DBPF).

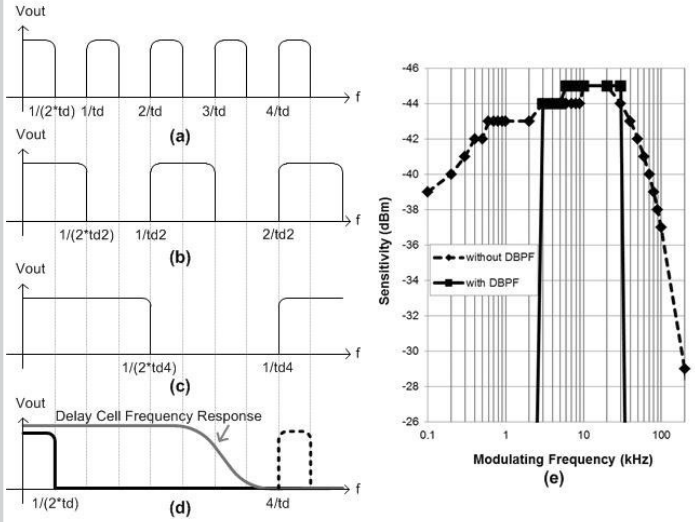

Figure 26.4.4: Frequency response of the DBPF.

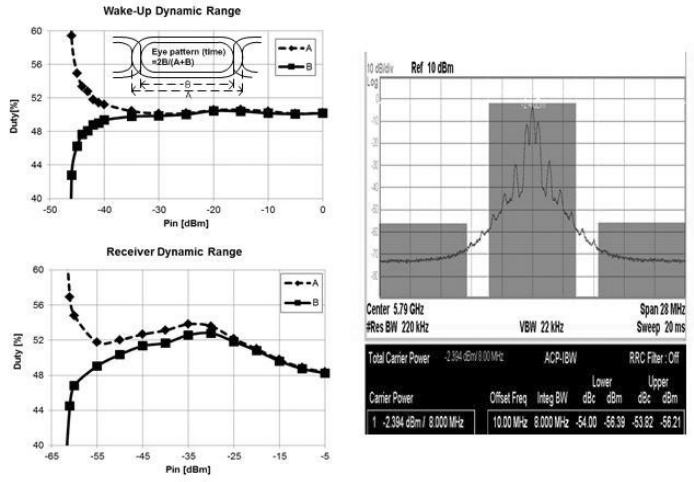

Figure 26.4.5: WuRX and RX dynamic range and TX ACPR.

Parameter		Requirement [3]	This Work
Technology		-	0.13um CMOS
Supply Voltage		-	3.0~3.6V
Operating Frequency		5.8GHz	5.8GHz
WuRx	Wake-Up frequency	14kHz	14kHz
	Sensitivity (MI=0.85)	≤ -40dBm	-45dBm
	Current consumption	-	15uA
Rx	Data rate	256kbps	256kbps
	Sensitivity (MI=0.85)	≤ -50dBm	-61dBm
	Current consumption	-	19mA
Tx	Output power	≤ +10dBm	+5dBm
	Modulation index	0.5~0.9	0.5~0.9
	Data rate	512kbps	512kbps
	Occupied BW (99% power)	≤ 5MHz	3MHz
	ACPR	≤ -30dBc	-53dBc
	Spurious emission	≤ -30dBm	-51dBm
	Current consumption	-	40mA

Figure 26.4.6: Complete transceiver performance summary.

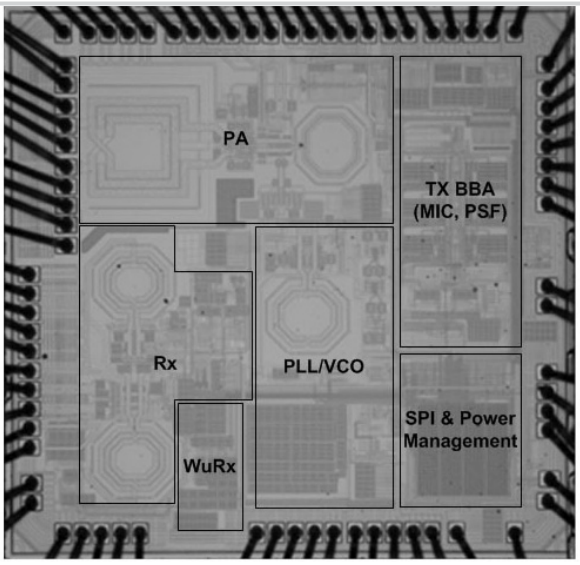

Figure 26.4.7: Chip micrograph (1,700µm x1,650µm).

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