A CMOS Highly Linear Low-Noise Amplifier for Digital TV Applications

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***Abstract*—This paper presents a highly linear low-noise amplifier (LNA) for Digital TV applications. By including a second-order nonlinear cancelling transistor to the noise cancelling circuit, the proposed LNA achieves high IIP_3 which is immune to the offset frequency of two tone signals. The proposed LNA is implemented as a differential architecture in 0.13 μm CMOS technology, and measurements show +17.8 dBm, 12.4 dB and 1.6 dB of IIP_3, gain and NF, respectively, while drawing 18.45 mA from 1.2 V.**

***Index Terms*—Wide-band, Nonlinear cancellation, low-noise amplifier (LNA), noise cancelling, resistive shunt feedback**

I. Introduction

THE digital TV (D-TV) market has recently experienced substantial growth due to the transition from analog to digital television broadcasting system. There has been much efforts to fully integrate the D-TV tuners into a single chip, which covers the entire TV band of both terrestrial and cable modes. However, the stringent specifications of the D-TV standard present numerous design challenges that must be resolved. Especially, the low-noise amplifier has many challenging performance requirements such as wide-band input matching, low NF and high linearity. Wide-band input matching can be rather easily achieved by adopting common-gate input stage, resistive shunt feedback, active shunt feedback, etc. However, most of these techniques has high NF problem. The simultaneous noise and input matching technique [1] is a narrow band solution and not effective in wide-band LNA design. In wide-band LNA design, noise cancellation techniques are widely adopted [2].

Besides NF, linearity is also an important parameter in wide-band LNA design by the fact that the LNA has to handle numerous signals at the same time, which will interfere with each other by the nonlinearities. Amplifier nonlinearities can be expressed in terms of the input second and third-order intercept points (IIP_2 and IIP_3). The even-order nonlinearity (IIP_2) can generally neglected in a narrow band LNA systems because the intermodulation products are located out of band. Furthermore, IIP_2 can be increased by adopting a differential architecture. In contrast, the intermodulation products that determine the IIP_3 often fall within the desired frequency band. To solve this issue, cancelling the third-order nonlinear component of the amplifying transistor(s) [3-5] has been proposed. This solution is very effective solution to improve IIP_3 of narrow band LNAs [3-5]. With wide-band amplifier as a solution, however, cancelling only the third-order nonlinear component is not sufficient to achieve high IIP_3, especially, when it is combined with noise cancelling technique as well. In order to acquire high IIP_3, all the third-order inter-modulated distortion (IMD3) components from various elements of the circuit must be identified so that they can be eliminated.

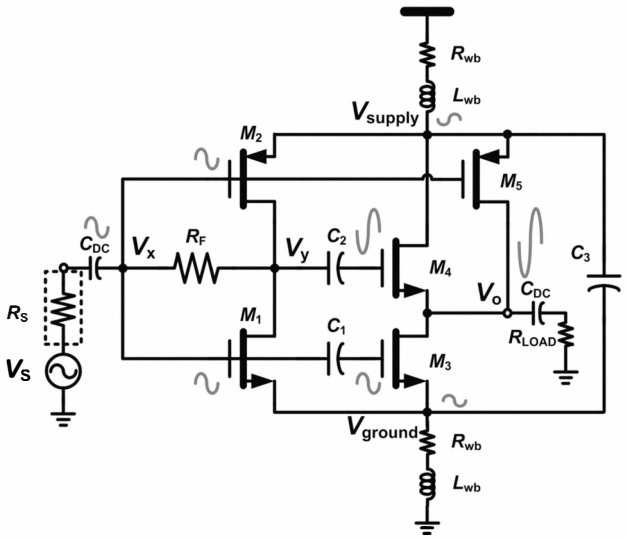

Fig. 1. The half circuit of the proposed LNA.

This works reports a wide-band LNA topology that achieves low NF and high IIP_3 by adopting simultaneous noise and IMD3 cancelling technique based on a detailed analysis of the circuit behavior.

II. Proposed LNA Utilizing Noise and Nonlinear Cancellation Mechanism

The proposed LNA is designed as a differential amplifier and the complete half circuit schematic is shown in Fig. 1. In Fig. 1, the first stage adopts a complementary resistive shunt feedback (CRSF) amplifier to increase the transconductance, achieve input matching, facilitate reduced power consumption, and attain wide-band operation [2]. An additional benefit of the CSRF architecture is self-biasing since the feedback resistor sets the bias point of M_1 and M_2. The second stage, composed of M_3, M_4, and M_5, provides noise and nonlinear component cancellation function. Similar to the design in [2], M_3 and M_4 effectively cancel the thermal noise generated by M_1 and M_2. The two additional components in the second stage, M_5

and C_3, are added to further improve the linearity of the LNA without degrading the NF. In Fig. 1, R_{wb} and L_{wb} models the wire-bond.

In designing the CSRF amplifier, the ratio of R_F and R_S should be maximized to achieve a high gain, thereby minimizing the noise contributions of subsequent stages. Consequently, the ratio of the transconductances of M_3 and M_4 (g_{m3}/g_{m4}) must also be high to satisfy the noise cancelling condition [2]. However, this leads to an increase in the size ratio of $(W/L)_{M3}/(W/L)_{M4}$, which leads to the decrease in the DC bias voltage at the output node. As a result, M_3 moves close to the triode region operation, degrading the linearity of M_3. To avoid this situation, the PMOS transistor M_5 is added as a bleeding current source to increase the output DC voltage. Thus, the linearity of the LNA can be improved. Furthermore, in Fig. 1, the gate of M_5 is connected to the input of the LNA, which effectively makes M_5 in parallel connection with M_3. Therefore, the required g_m value of M_3 can be reduced, meaning that the size ratio of M_3 with respect to M_4 ($(W/L)_{M3}/(W/L)_{M4}$) can be reduced, which additionally contribute to increase the output DC voltage. With M_5, the modified noise cancelling condition is given by

$$\frac{R_F + R_S}{R_S} = \frac{(g_{m3} + g_{m5})}{g_{m4}} \tag{1}$$

which should be satisfied to minimize the NF of the LNA. From the noise cancelling condition, the third-order nonlinear components of M_1, M_2, M_3, M_4 and M_5 are also partially cancelled at the output node. For the more complete cancellation, the more accurate analysis of the proposed LNA is required.

By adopting Volterra analysis is adopted, the fundamental and the third-order nonlinear components at the output of the proposed LNA are given by

$$\begin{aligned} C_1(s_1) = &\left(-\left(g_{m3} + g_{m5}\right) A_1(s_1) + g_{m4} B_1(s_1)\right) \\ &\times \left(r_{o3} || r_{o4} || r_{o5} || Z_l(s)\right) \end{aligned} \tag{2}$$

and

$$\begin{aligned} &C_3(s_1, s_2, s_3) = \\ &\left(-\left(g_{m3} + g_{m5}\right) A_3(s_1, s_2, s_2) + g_{m4} B_3(s_1, s_2, s_3)\right. \\ &-\frac{1}{2}\left(g'_{m3} - g'_{m5}\right) A_1(s_1)\overline{A_2(s_2, s_3)} - \frac{g'_{m4}}{2} B_1(s_1)\overline{B_2(s_2, s_3)} \\ &-\frac{1}{6}\left(g''_{m3} + g''_{m5}\right) A_1(s_1) A_1(s_2) A_1(s_3) \\ &\left.+\frac{g''_{m4}}{6} B_1(s_1) B_1(s_2) B_1(s_3)\right) \\ &\times \left(r_{o3} || r_{o4} || r_{o5} || Z_l(s_1 + s_2 + s_3)\right) \end{aligned} \tag{3}$$

where $K_1(s_1)$, $K_2(s_1, s_2)$ and $K_3(s_1, s_2, s_3)$ denote Volterra kernels (coefficients) at V_x, V_y and V_o for K=A, B and C, respectively. To increase IIP_3, the value of $C_3(s_1, s_2, s_3)$ is minimizing while maintaining $C_1(s_1)$. The first and second terms in (3) are cancelled by the noise cancelling condition of (1). Also, the fifth and sixth terms are cancelled by the same condition with a small amount of error [7]. Adding PMOS, the opposite polarity term of g'_{m5} is added the second-order nonlinear components in (3). In Fig. 1, a blocking capacitor

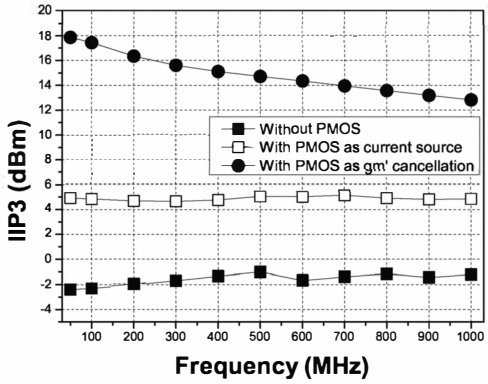

Fig. 2. The simulated IIP_3 without M_5, with M_5 as current source and g'_{m3} cancellation.

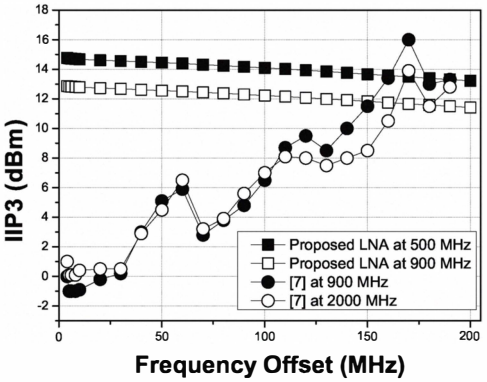

Fig. 3. The IIP_3 comparisons with [7] over frequency offset.

(C_1) is inserted at the gate of M_3 to allow independent control of the bias current of M_3 and M_5. Therefore, by the appropriate biasing of M_3 and M_5, the third and fourth terms of (3) can be eliminated. As a result, all terms in (3) can be removed by the adoption of M_5 and C_1.

Fig. 2 shows the simulated IIP_3 of the LNA for different roles of M_5. In Fig. 1, the ratio of $(R_F + R_S)$ and (R_S) is set to 7:1 while the transconductances of M_3, M_4 and M_5 are determined to satisfy (1). For the frequency offset of 6 MHz, in Fig. 2, the simulated IIP_3 is -2 dBm without M_5 and 5 dBm when M_5 is used as a current source, respectively. When M_5 is employed for the third and fourth terms cancellation as well, the IIP_3 increases to around 17 dBm at low frequencies. At high frequencies, IIP_3 decreases caused by the parasitic capacitors, which are neglected in the analysis for simplicity. The simulation results shown in Fig. 2 demonstrate the improvement in IIP_3 by cancelling the nonlinear components at the output, which are achieved by the adoption of M_5 and C_1.

The proposed LNA offers an additional advantage over previously reported noise cancelling designs [7]. Typically, the

NMOS and PMOS transistors that facilitate the cancellation of second-order (g'_m) nonlinear components must be capacitively coupled so that independent biasing can be achieved [7]. However, the required capacitance becomes inhibitively large to cover the low offset frequencies of the two tones, like the case implemented in the D-TV applications. In contrast, the proposed LNA requires no coupling capacitor at the output node, thereby maintaining excellent IIP_3 performance at an arbitrarily low offset frequencies. For verification, simulations are performed at 500 and 1000 MHz, and the offset frequency is varied from 1 to 200 MHz in each case as shown in Fig. 3. In Fig. 3, the IIP_3 of the proposed LNA remains at around 14 and 12 dBm for 500 MHz and 1000 MHz, respectively, as the offset frequency is varied, while the LNA reported at [7] show more than 15 dB reduction. The small reduction in IIP_3 of the proposed design at higher frequencies is caused by the asymmetry of the second-order nonlinear components at the output node caused by the gain mismatch at high $(\omega_1 + \omega_2)$ and low $(\omega_1 - \omega_2)$ frequencies due to the parasitic capacitors.

Generally, wire bondings can have a significant impact on the performance of RFICs. Therefore, the bond-wire parasitic should be considered. In Fig. 1, as a compromise between accuracy and simplicity, the wire-bonds are modelled with a series resistor and an inductor. While there are numerous wire bonding connections, their effects can be neglected depending on the location and frequency. In Fig. 1, the wire bonding effects of only the supply and ground nodes are considered. In Fig. 1, LNA performance can be improved by adopting separate bond pads for M_1/M_3 and $M_2/M_4/M_5$, respectively. However, the number of available pads on the IC often precludes this option. Compare to the narrow band designs, wide-band LNAs tend to draw substantially higher amounts of current for the matching and low NF, such that the voltage across the bond wire can be considerable, which leads to the NF, gain and linearity degradation.

The proposed LNA is a pseudo differential architecture, therefore, the second-order harmonics of the input signal are incurred at the supply and ground nodes. Additionally, the second- and third-order nonlinear components appear at the output node caused by the wire-bond parasitics since transconductance is a function of V_{gs}. To decrease the linearity degradation, the bond-wire parasitics should be minimized. In Fig. 1, the issue of bond-wire parasitics resolved by adopting the MOS capacitor C_3. Fig. 4 shows the IIP_3 of the LNA for three cases: with wire-bonding, without wire-bonding, and wire-bonding with an MOS capacitor C_3. As can be seen in Fig. 4, the bond wire effect can be removed substantially by the adoption of C_3 with less than the 2dB of IIP_3 degradation.

III. Implementation and Measurement Results

The proposed LNA designed for the frequency band of 50 to 900 MHz is fabricated in a 0.13 μm CMOS technology. The microphotograph of the fabricated chip is shown in Fig. 5 with chip size of 0.88 $\times$ 0.62 mm^2. The chip is directly wire bonded on a PCB for measurements.

Fig. 6 shows the measured S-parameters and NF. The input and output are well matched over the entire target frequency.

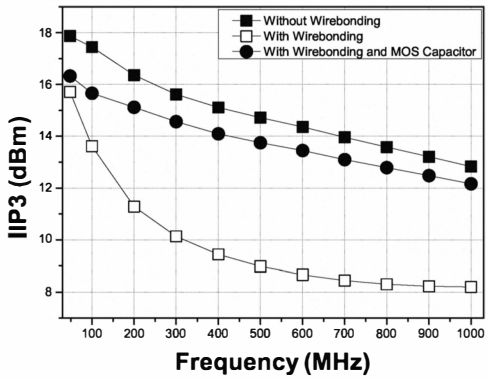

Fig. 4. The simulated IIP_3 values over wire-bonding and bypass capacitor.

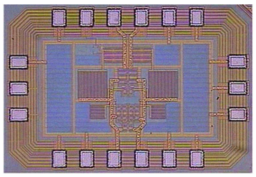

Fig. 5. Chip micro photograph.

S11 and S22 remain below -8 dB for frequencies over the entire frequency band of measurement. S21 starts to drop at frequencies exceeding 2 GHz due to the parasitic capacitances of the chip and PCB. The maximum S21 is 12.4 dB and the 3-dB bandwidth is approximately 2.3 GHz. The measured NF of the proposed LNA is under 2 dB over the target frequency ranges of 50 to 900 MHz and shows good agreement with simulation results. However, discrepancies are observed at low and high frequencies. At low frequencies, MOSFET flicker noise as well as incomplete noise cancellation caused by the high impedance of the on-chip DC blocking capacitor degrade

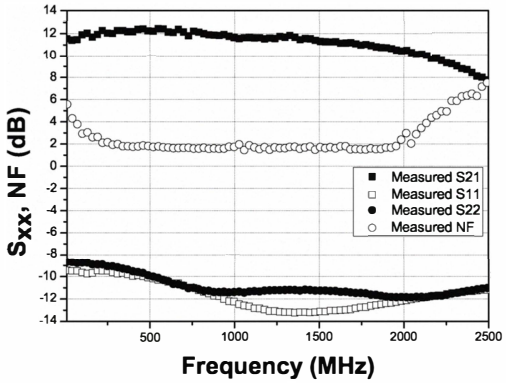

Fig. 6. The measured S-parameters and NF.

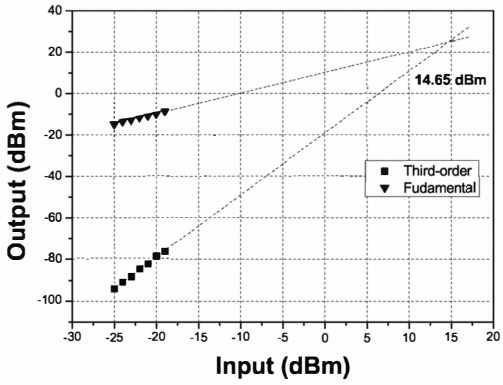

Fig. 7. The measured IIP_3 at 500 MHz.

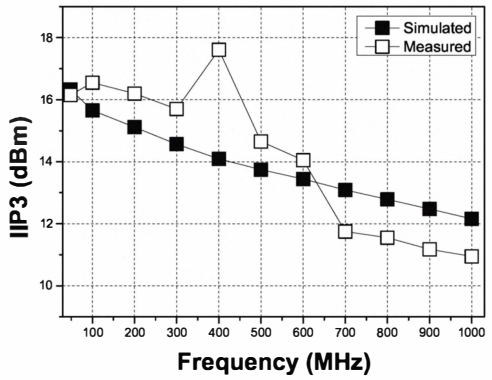

Fig. 8. The simulated and measured IIP3 over the frequency

the NF. At frequencies exceeding 2 GHz, the NF increases due to gain degradation caused by the parasitic capacitances of the chip and PCB.

Fig. 7 shows the measured IIP_3 at 500 MHz. For the IIP_3 measurement, two tones of 497 and 503 MHz are applied to the input of the LNA, yielding an IIP_3 of 14.65 dBm. Fig. 8 shows the simulated and measured IIP_3 of the LNA over the operating frequency range of 50 to 1000 MHz. IIP_3 is measured with two tones of 6 MHz offset. In Fig. 8, overall, the measurement results are in good agreement with simulation. The measured IIP_3 exceeds 10 dBm below 1 GHz, which is comparable to the performances achieved in the narrow band LNAs that utilize linearity improvement techniques [3-4]. Measurement results confirm the effect of adopting M_5 and C_3.

The proposed LNA draws 18.45 mA from a 1.2 V supply. Table. I summarizes the measured performances and compares with state-of-the-art LNAs. The proposed LNA shows the highest IIP_3 value measured with narrow two tone frequency offsets.

TABLE I
PERFORMANCE COMPARISON WITH RECENTLY PUBLISHED WORKS

	Tech. (nm)	Bandwidth (MHz)	S_{11} (dB)	Gain (dB)	NF (dB)	IIP_3 (dBm)	Supply Voltage (V)	Power (mW)	Freq. Offset (MHz)
This	**130**	**4-2200**	**<-8**	**12.4**	**1.6**	**+17.8**	**1.2**	**18.45**	**6**
[2]	250	2-1600	<-8	13.7	2.5	0	2.5	35	4
[6]	130	2100	<-10	5.2	3.0	+10.5	1.2	12.6	7
[7]	130	0.8-2.1	<-15	14.5	2.6	+16	1.5	17.4	170
[8]	130	400-5000	<-10	19	3	+1	1.8	11.7	
[9]	180	470-860	<-10	10	5.7	+10	1.8	5.2	7

IV. CONCLUSION

This paper presents a highly linear, inductor-less wide-band LNA for D-TV applications. A CRSF amplifier with noise cancelling circuits is adopted for wide-band input matching and low NF. In order to increase IIP_3, a PMOS transistor is added to the design to cancel the remained second-order nonlinear components at the output as well as to prevent triode mode operation of a transistor in the noise cancellation path. In addition, the impacts of wire-bonding on wide-band amplifier are also considered and a bypassing MOS capacitor is adopted to alleviate the performance degradation. The measured results verify that the proposed LNA achieves a high IIP_3 of over 10 dBm over the frequency band of 50 to 1000 MHz. The linearity achieved by the proposed architecture is comparable to that of narrow band LNAs, making it very attractive for wide-band applications.

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