A Quantization Noise Cancelling Fractional-N type $\Delta\Sigma$ Frequency Synthesizer using SAR-based DAC Gain Calibration

Seungjin Kim, In-Young Lee, Joo-Myoung Kim, and Sang-Gug Lee

Dept. of Electrical Engineering, KAIST, Daejeon, 305-701, Korea

***Abstract*—A high-speed and low-power adaptable period SAR-based DAC gain calibration is presented for DSM quantization noise suppression, which completes within 10μs while dissipating 0.2mW. The proposed calibration scheme is applied to the fractional-N type frequency synthesizer which adopts an 8-bit noise-cancelling DAC. The frequency synthesizer has a range of 48 to 900 MHz, consumes 11mA from 1.2-V supply and occupies 1.5 $\times$ 1.4 mm^2 in 0.13μm CMOS process. The measurement shows more than 30-dB quantization noise suppression at a 877-MHz oscillation frequency which results in the phase noise of -100.7dBc/Hz and -134.5dBc/Hz at 100-kHz and 1.25-MHz offset frequencies respectively.**

I. Introduction

Fractional-N type frequency synthesizer has gained much interest for their high flexibility for channel allocation and superior in-band noise performance by employing high reference frequency. However, the fractional-N type architecture suffers from out-of-band phase noise arising from the quantization noise of the $\Delta\Sigma$ modulator (DSM).

Much effort has been reported associated with the cancellation technique of the quantization noise. In particular, the noise-cancelling DAC technique [1]-[4] is considered the most suitable solution to alleviate the quantization noise issue in wideband frequency synthesizer due to its high quantization noise rejection ratio (QNRR)[1]-[4]. The quantization noise rejection in [1]-[4] depends on the precise timing and gain matching between the noise-cancelling DAC and the synthesizer core. However, the wide variation of design parameters, up to synthesizer operating condition, such as frequency dividing ratio and charge pump current restricts precise timing and gain matching along with PVT variation.

Moreover, in [1],[2], the gain of DAC is set as a fixed constant in the design phase such that a small design variation easily disturbs the frequency synthesizer to operate in the least quantization error region. Although, as an alternative solution, the least-mean-square(LMS) algorithm-based gain trimming technique has been reported in [3], [4], its narrow bandwidth of LMS loop and analog implementation of correlation comparing blocks leave high power consumption and slow settling time issues to be solved.

This paper presents a quantization-noise cancelling fractional-N type frequency synthesizer using a high-speed and low-power successive approximation register(SAR)-based DAC gain calibration which adopts an adaptable period scheme and XOR-based correlation comparator.

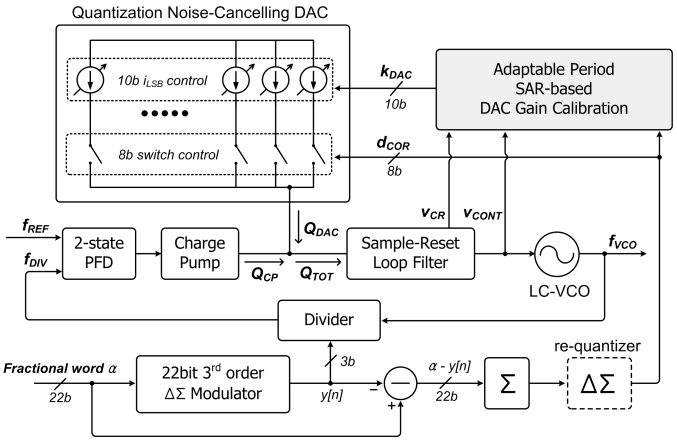


Fig. 1. The block diagram of the proposed frequency synthesizer

II. Architecture and Operational Principle

Fig. 1 shows the block diagram of the proposed frequency synthesizer. As shown in Fig. 1, the synthesizer core adopts Type-I architecture which consists of a two-state phase/frequency detector(PFD), single-polarity charge pump(CP) along with a discrete-time sample-reset loop filter(LF). Type-I architecture guarantees an always-negative phase error($\Phi_{REF} < \Phi_{DIV}$) at the input of the PFD and thus allows CP and DAC to adopt single-polarity scheme, which alleviates up/down current mismatch[2].

While a 22-bit 3rd-order single loop DSM is used for fractional-N function, the subtractor and accumulator generate an error correction code, d_{COR}, for DSM quantization noise cancellation. During the DAC gain calibration, the re-quantizer is set to be turned off such that the 22-bit error correction code is truncated to 8-bit code, and then is turned on after the DAC gain calibration is completed. An 8-bit quantization noise-cancelling DAC converts d_{COR} to error correction charge, Q_{DAC}, with a proper gain, k_{DAC}, and thus cancels DSM quantization noise in CP charge, Q_{CP}. The sample-reset LF converts the noise-cancelled total charge, Q_{TOT}, into the coarse voltage, v_{CR} as well as the filtered VCO-control

978-1-4673-1556-2/12/$31.00@2012 IEEE

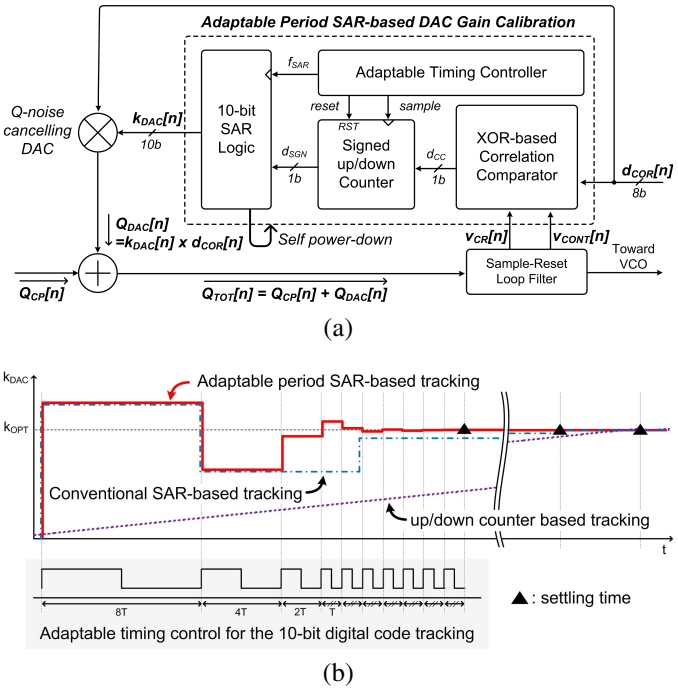


Fig. 2. (a) The block diagram of the proposed SAR-based DAC gain calibration and (b) timing waveform for the adaptable timing control.

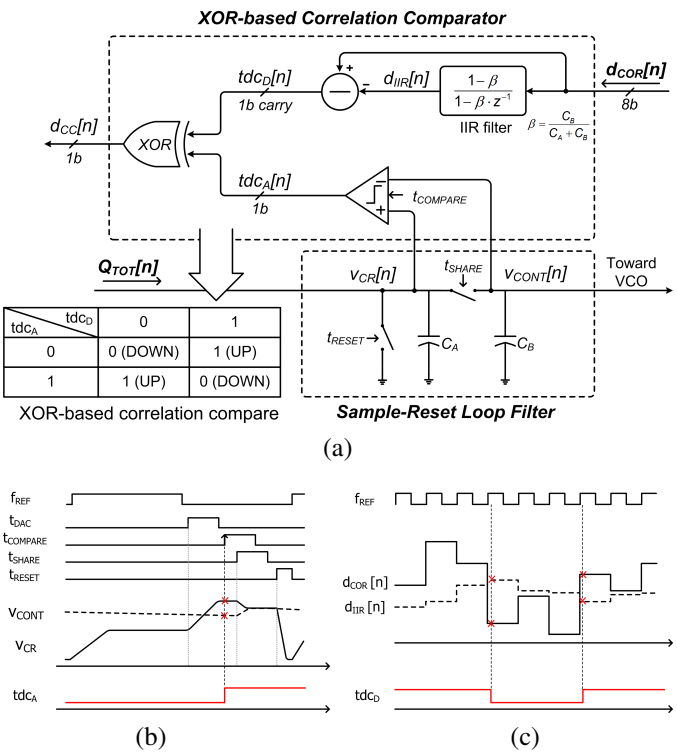


Fig. 3. (a)Block diagram of the proposed XOR-based correlation comparator and timing diagram of (b)analog 1-bit tendency code with sample-reset loop filter and (c) digital 1-bit tendency code.

voltage, v_{CONT}.

An adaptable period SAR-based gain calibration is proposed for DAC gain, k_{DAC}, calibration in which an adaptable timing controller further reduces the settling time of SAR-based binary gain-code tracking schemes.

A. Adaptable Period SAR-based DAC Gain Calibration

As shown in Fig. 2, the proposed SAR-based DAC gain calibration consists of an XOR-based correlation comparator, a signed up/down counter, an adaptable timing controller, 10-bit SAR logic, and self-power-down circuit. The XOR-based correlation comparator persistently yields 1-bit correlation code, d_{CC} which represents the correlation between up/downward tendency of $d_{COR}[n]$ and that of $Q_{TOT}[n]$. The signed up/down counter takes 1-bit correlation code, d_{CC}, and generates 1-bit up/down decision code, d_{SGN}, after the bias voltage of the quantization noise-cancelling DAC is settled enough. Then, the 10-bit SAR logic performs binary gain-code tracking using d_{SGN} and finally sends out 10-bit DAC gain code, k_{DAC}. Although the SAR-based binary gain-code tracking inherently has faster settling time than that of prior works[3],[4], the proposed architecture further reduces its settling time by adaptable-period allotment for each bit of gain-code tracking.

As shown in Fig. 2(b), the adaptable-period SAR-based tracking chases an optimal gain, k_{OPT}, with binary-length periods thus settling faster while the conventional SAR-based and the up/down counter based tracking schemes are chasing k_{OPT} with equi-length periods.

B. XOR-based Correlation Comparator and Self Power-Down

The discrete-time sample-reset LF in type-I architecture allows noise-cancelled total charge, $Q_{TOT}[n]$, to be simplified into 1-bit up/downward tendency code by comparing v_{CR} and v_{CONT} because v_{CONT} represents IIR-filtering value of v_{CR}. For the sake of the simple tendency code, the proposed correlation comparator can operate based on XOR gate and thus reduces the design complexity and power consumption at the same time. In addition, the DAC gain calibration loop adopts the self-power-down circuit to further reduce the power consumption by turning itself off after gain calibration is finished.

III. Circuit Implementation

A. XOR-based Correlation Comparator

As shown in Fig. 3(a), the XOR-based correlation comparator consists of a clocked comparator, an IIR filter, a subtractor, and an XOR gate. The clocked comparator along with the sample-reset LF generate 1-bit tendency code, $tdc_A[n]$ from the coarse voltage, $v_{CR}[n]$ and VCO control voltage, $v_{CONT}[n]$. Since, as is well known, sample-reset LF has an infinite-impulse response(IIR) filter characteristic, the coarse voltage, $v_{CR}[n]$ and VCO control voltage, $v_{CONT}[n]$ represents $Q_{TOT}[n]$ and the average from $Q_{TOT}[n-\infty]$ to $Q_{TOT}[n-1]$. Thus, the clocked comparator output, $tdc_A[n]$, can be regarded as the up/downward tendency of $Q_{TOT}[n]$.

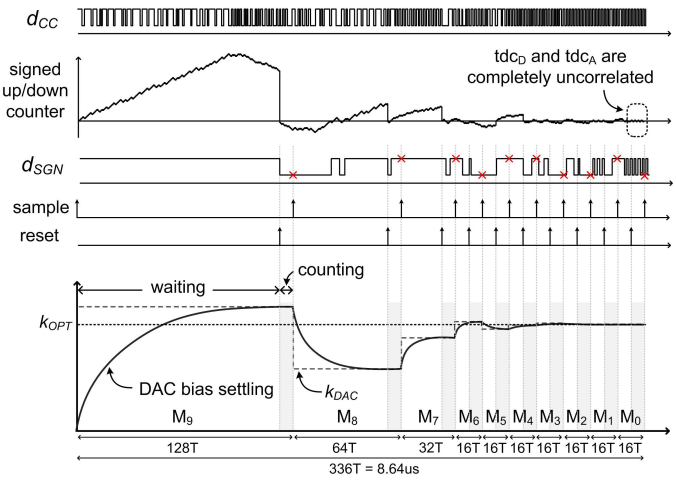


Fig. 4. The timing diagram for the proposed SAR-based DAC gain-code tracking.

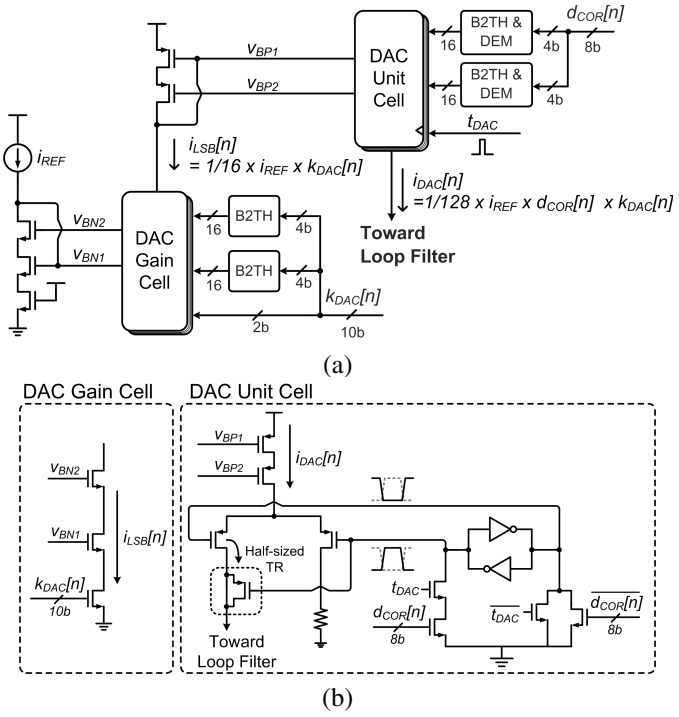


Fig. 5. The block diagram of (a) the noise-cancelling DAC and (b) the schematic of DAC gain cell and DAC unit cell.

For equivalent comparison, a digital IIR filter with a coefficient β and a digital subtractor are implemented for 1-bit tendency code generation, where $\beta = C_B/(C_A + C_B)$. In the same manner, digital error-correction code, $d_{COR}[n]$, is converted into the average value, $d_{IIR}[n]$ through the digital IIR filter while the subtractor sends out the carry bit by comparing $d_{COR}[n]$ with $d_{IIR}[n-1]$. The carry bit of the subtractor is the 1-bit tendency code, $tdc_D[n]$.

The table in Fig. 3(a), shows the correlation comparing code, $d_{CC}[n]$, and the corresponding order to adjust the DAC gain code, $k_{DAC}[n]$. If $tdc_D[n]$ and $tdc_A[n]$ are equal, we can judge that the $d_{COR}[n]$ and $Q_{TOT}[n]$ have positive correlation, therefore the correlation comparator issues an order to decrease the DAC gain, k_{DAC}, to minimize the correlation between $d_{COR}[n]$ and $Q_{TOT}[n]$. Otherwise, correlation comparator issues an order to increase the DAC gain, k_{DAC}.

B. 10-bit SAR-based DAC Gain-Code Tracking

Fig. 4 shows the timing diagram for the proposed SAR-based DAC gain-code tracking. For the binary code settling operation, the SAR-based DAC gain-code tracking scheme requires a decision bit to determine whether the next half-bit is increased or decreased. As shown in Fig. 4, a signed up/down counter is utilized to generate the 1-bit up/down decision code, d_{SGN}, by accumulating the 1-bit correlation code, d_{CC}. In order to prevent an erroneous operation due to incomplete DAC bias settling, the 1-bit up/down decision code, d_{SGN}, in the *counting* period (from *reset* to *sample* phase) where the DAC bias is stabilized enough, is utilized to assign the next half-bit.

Furthermore, a non-uniform period allocation is used to reduce the DAC gain calibration time. As shown in Fig. 4, the first three MSBs are set to have a wider period(128T, 64T, and 32T) than the others(16T) by considering the abrupt changes in DAC bias voltage. The total required DAC gain-code tracking time for the 10-bit SAR-based binary searching is only 8.64μs(336 period) using 38.88MHz reference clock.

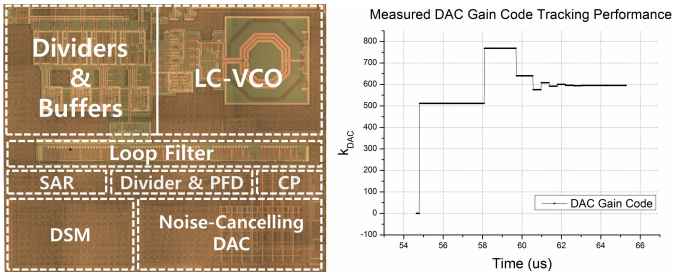
In addition, after the DAC gain-code tracking is finished, the DAC gain calibration block is designed to hold its calibrated digital codes using D-flipflops and turn itself off by cutting the operating clock until the next change in operation to prevent additional power consumption.

C. 8-bit Noise-Cancelling DAC

Fig. 5 shows the block diagram of the noise-cancelling DAC and the schematic of its subsidiary blocks. As shown in Fig. 5(a), the 10-bit $k_{DAC}[n]$ code from the DAC gain calibration block is utilized to set the unit current, $i_{LSB}[n] = i_{REF} \cdot {}^1\!/_{16} \cdot k_{DAC}[n]$. By multiplying the unit current, $i_{LSB}[n]$, to the 8-bit digital error-correction code, $d_{COR}[n]$, the total DAC current $i_{DAC}[n]$ can be given by

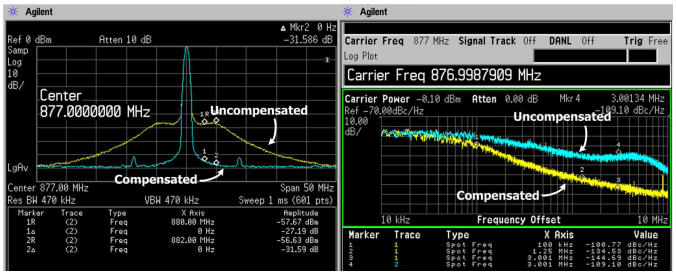
$$\begin{aligned} i_{DAC}[n] &= i_{LSB} \cdot {}^1\!/_8 \cdot d_{COR}[n] \\ &= {}^1\!/_{128} \cdot i_{REF} \cdot k_{DAC}[n] \cdot d_{COR}[n] \end{aligned} \quad (1)$$

where 128 is the relative width of the current mirroring circuitry of the DAC gain cell and DAC unit cell in Fig. 5. As shown in Fig. 5(a), a 4-bit binary to thermometer decoder(B2TH) and dynamic element matching(DEM) block are adopted to improve the monotonousness and reduce the mismatches between the individual DAC unit cell, respectively. Fig. 5(b) shows the DAC gain cell has a cascode architecture with an nMOS switch to adjust the current, $i_{LSB}[n]$. The DAC unit cell adopts a pMOS cascode with a differential switch along with a half-sized dummy to absorb the charge injection from the switching operation and an inverter latch to improve the differential characteristic of switching signal.



(a) (b)

Fig. 6. (a)The micrograph of the fabricated chip and (b)measured DAC gain settling time.



(a) (b)

Fig. 7. Measured (a)frequency spectrum and (b) phase noise at 877MHz output frequency.

IV. Experimental Results

The frequency synthesizer has a range of 48M to 900-MHz, consumes 11mA from 1.2V supply, and occupies 1.5 $\times$ 1.4 mm^2 in 0.13μm CMOS, including LC-VCO and wideband dividers. Fig. 6 shows the micrograph of the fabricated chip and the measured DAC gain settling time. Fig. 6(b) shows that the settling time of the proposed SAR-based DAC gain calibration is 8.64μs while dissipating 0.2mW only during the k_{DAC} settling region. Fig. 7(a), the frequency spectrum at 877MHz of output frequency of the proposed synthesizer shows more than 30dB of QNRR at 3MHz offset frequency. Fig. 7(b) shows the phase noise of -100.7 dBc/Hz and -134.5 dBc/Hz at 100-kHz and 1.25-MHz offset frequencies, respectively.

V. Conclusion

In this paper, a high-speed and low-power adaptable period SAR-based DAC gain calibration is proposed for DSM quantization noise suppression, which completes within 10μs while dissipating 0.2mW. The proposed calibration scheme is applied to the fractional-N type frequency synthesizer with an 8-bit noise-cancelling DAC. The proposed frequency synthesizer shows more than 30-dB quantization noise suppression at 877-MHz oscillation frequency, resulting in the phase noise of -100.7dBc/Hz and -134.5dBc/Hz at 100-kHz and 1.25-MHz offset frequencies respectively while dissipating 11mA from 1.2-V supply.

TABLE I
Performance Summary and Comparison

	[3]	[4]	This work
Frequency	1.6-2.0GHz	2.4-2.5GHz	48-900MHz
Area [mm^2]	2	4.8	2.1
In-band PN	-98 dBc/Hz	-101 dBc/Hz	-100 dBc/Hz
Out-band PN	-123 dBc/Hz (3MHz)	-124 dBc/Hz (3MHz)	-144.7 dBc/Hz (3MHz)
Power [mW]	25	38	13.2
Cal. Power[mW]	9	1.4	0.2 (Only for settling)
Cal. Settling	1s	35μs	8.64μs
QNRR	30dB	33dB	35dB
Technology	0.18μm	0.18μm	0.13μm

Acknowledgment

This work was supported by a National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (Grant No. 2010-0018899)

References

[1] S. E. Meninger and M. H. Perrott, "A 1MHz Bandwidth 3.6GHz 0.18μm CMOS Fractional-N Synthesizer Utilizing a Hybrid PFD/DAC Structure for Reduced Broadband Phase Noise", *IEEE J. Solid-State Circuits* , vol.41, no.4, pp.966-980, Apr. 2006.

[2] H. Hedayati, W. Khalil and B.Bakkaloglu, "A 1MHz Bandwidth, 6GHz 0.18μm CMOS type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications", *IEEE J. Solid-State Circuits*, vol.44, no.12, pp.3244-3252, Dec. 2009.

[3] M. Gupta and B.-S Song, "A 1.8-GHz spur-cancelled fractional-N frequency synthesizer with LMS-based DAC gain calibration", *IEEE J. Solid-State Circuits*, vol.41, no.12, pp.2842-2851, Dec. 2006.

[4] A. Swaminathan, K. Wang, and I. Galton, "A wide-bandwidth 2.4GHz ISM-band fractional-N PLL with adaptive phase-noise cancellation," *IEEE J. Solid-State Circuits*, vol.42, no.12, pp.2639-2650, Dec. 2007.