Non-Load-Balance-Dependent High Efficiency Single-Inductor Multiple-Output (SIMO) DC-DC Converters

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***Abstract*—A single-inductor multiple-output (SIMO) DC-DC converter providing buck and boost outputs with a new control topology is presented. In the proposed switching sequence, which does not require any special blocks, energy delivery is always accomplished by flowing energy through an inductor, which leads to high conversion efficiency regardless of the balance between the buck and boost output loads. Implemented in 0.35-μm CMOS, the proposed SIMO DC-DC converter achieves high conversion efficiency regardless of the load balance between the outputs. The measured maximum efficiency reaches 82 $\%$ under heavy loads.**

I. Introduction

Along with the growth of the battery-powered portable device market, the development of efficient power management integrated circuits (PMIC) is currently a popular and active research area. A DC-DC converter, which is an essential block in PMIC, provides a regulated output voltage from linearly discharging battery voltage in portable devices. In many portable device systems which require multiple regulated output voltages from only one battery supply, including multiple DC-DC converters can be a viable means of generating different output voltage levels. However, this approach leads to an increase in cost and area requirements due to the use of multiple off-chip inductors, which is not suitable for portable devices. To circumvent this issue, the single-inductor multiple-output (SIMO) DC-DC converter has been proposed. It literally requires only one inductor to regulate multiple output voltages. Various works [1]-[4] have focused on SIMO DC-DC converters that adopt a single energizing cycle per switching period, leading to performance levels with greater accuracy characterized by smaller output voltage ripples and faster control loops [5]. Several works [1]-[3] have proposed control topologies, each with their own advantages. However, their applications are limited by lack of flexibility as regards buck and boost implementations. One study [4] presented a SIMO DC-DC converter that provides both buck and boost outputs simultaneously with a reduced number of power switches. To overcome a stability problem that arises during unbalanced output loads, a hysteresis mode was proposed [4]. However, implementing the hysteresis mode not only requires special blocks such as a power comparator and a delta-voltage generator circuit, but it also degrades the power conversion efficiency because the current flows not through the inductor but through the resistive freewheeling switch as the the buck output is charged. Thus, this paper proposes a new control topology. A switching sequence is presented to generate multiple buck and boost outputs without special blocks while achieving high conversion efficiency.

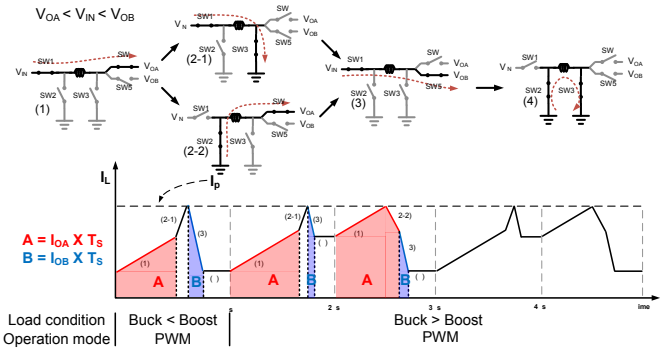

Fig. 1. Control sequence of a proposed SIMO DC-DC converter

This paper is organized as follows. Section II introduces the newly proposed control topology. Then, the implementation details of a DC-DC converter that adopts the newly proposed control sequence are shown in Section III and the measurement results are given in Section IV. The conclusions are made in Section V.

II. Principle of the Proposed Control Topology

A new control sequence is proposed, as shown in Fig. 1, to resolve the problems in the hysteresis mode [4]. The operation of a SIMO DC-DC converter with one buck and one boost output, adopting the proposed control sequence, can be described as follows. During phase-(1), switches SW1 and SW4 are turned on to charge the buck output. The inductor current I_L then ramps up at a rate of $(V_{IN} - V_{OA})/L$. The next phase is then determined between phase-(2-1) and phase-(2-2) depending on output load condition. When the buck output finishes being charged to a desired voltage level before the inductor current reaches a peak-current I_p, which can be controlled by previously reported techniques, phase-(2-1) is selected. Switches SW1 and SW3 are then turned on to energize the inductor during phase-(2-1), which makes I_L increase with a slope of V_{IN}/L until I_L reaches I_p. On the other hand, phase-(2-2) is chosen if more energy is required to regulate the buck output when I_L reaches I_p. During phase-(2-2), Switches SW2 and SW4 are turned on to deliver more charge to the buck output while I_L ramps down at a rate of $-V_{OA}/L$. After phase-(2-1) or phase-(2-2)

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TABLE I
CONTROL SEQUENCES DEPENDING ON LOAD CONDITIONS

Load conditions	Control sequences
Buck $<$ Boost	$1 \rightarrow$ 2-1 $\rightarrow 3 \rightarrow 4$
Buck $>$ Boost	$1 \rightarrow$ 2-1 $\rightarrow 3 \rightarrow 4 \rightarrow 1 \rightarrow$ 2-2 $\rightarrow 3 \rightarrow 4$

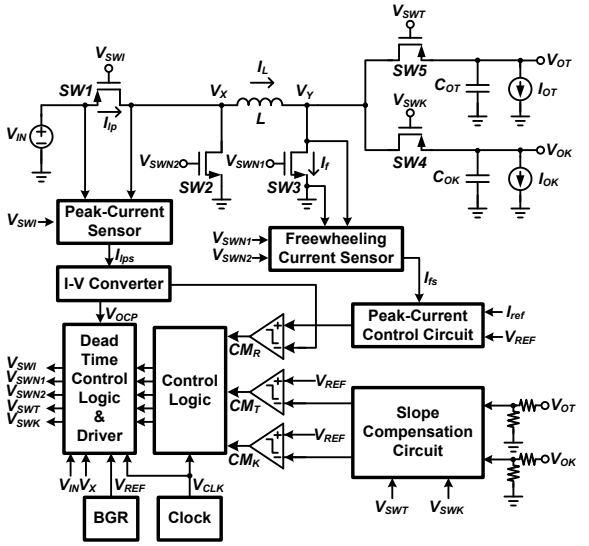


Fig. 2. Block diagram of the proposed SIMO DC-DC converter with non-load-balance-dependent high efficiency

is finished, phase-(3) begins and then I_L ramps down at a rate of $(V_{IN} - V_{OB})/L$ with switches SW1 and SW5 turned on. As soon as the boost output reaches thee desired voltage, phase-(3) becomes phase-(4) which is a freewheeling period. In phase-(4), switches SW2 and SW3 are turned on to hold I_L constant. Upon the end of the switching period, the routine returns to phase-(1). In summary, according to output load condition, two types of control sequences are used to regulate the buck and the boost outputs, as shown in Table I. Note that, high conversion efficiency can be achieved because energy delivery is always accomplished by flowing energy through the inductor. Moreover, the decision process between phase-(2-1) and phase-(2-2) can be implemented digitally without any special blocks.

III. IMPLEMENTATION DETAILS

The block diagram of the proposed SIMO DC-DC converter with non-load-balance-dependent high efficiency is illustrated in Fig. 2. The proposed control sequence, which was explained in Section II, can be implemented by a control logic block. The required control signals (CM_R, CM_T, and CM_K) are generated from other sub-blocks. A peak-current I_p, which is one of the factors that determines the duty cycle for each phase, can be controlled by adopting a freewheeling current feedback control scheme [2]. The output voltages are regulated directly by comparators in the freewheeling current feedback control scheme. A single compensation is sufficient for a freewheeling feedback loop. The principle of the freewheeling current feedback control scheme is to control the peak current by comparing the average of the freewheeling current with

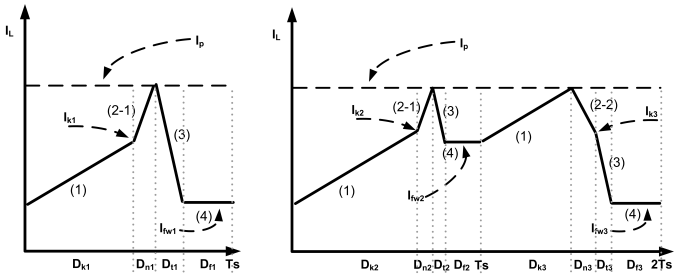


Fig. 3. Inductor current waveforms for (a) case-I (Buck $<$ Boost) and (b) case-II (Buck $>$ Boost)

a reference current. Even though the basic concept of the freewheeling current feedback control is used, the DC and AC characteristics of the proposed SIMO DC-DC converter are different from [2] because the control sequences are dissimilar. There are two cases for the DC and AC characteristics according to the load condition. Each case is analyzed in the next parts.

A. Case-I : Buck $<$ Boost

When the power of boost output is larger than that of buck output, the current waveform is shown in Fig. 3(a). The duty cycle of each phase is given by

$$d_{k1} = \frac{f_s}{m_K} \cdot (i_{k1} - i_{fw1}) \quad (1)$$

$$d_{n1} = \frac{f_s}{m_{N1}} \cdot (i_p - i_{k1}) \quad (2)$$

$$d_{t1} = \frac{f_s}{m_T} \cdot (i_p - i_{fw1}) \quad (3)$$

$$d_{f1} = 1 - d_{k1} - d_{n1} - d_{t1}, \quad (4)$$

where m_K, m_{N1}, and m_T are $(V_{IN} - V_{OA})/L$, V_{IN}/L, and $-(V_{IN} - V_{OB})/L$, respectively. The average of the freewheeling current, which should be regulated to I_{ref}, is given by

$$\langle i_{f1} \rangle_T = d_{f1} \cdot i_{fw1}. \quad (5)$$

The averaged supplied currents to the buck and boost outputs are given by

$$\langle i_{ok} \rangle_T = \frac{1}{2} \cdot (i_{k1} + i_{fw1}) \cdot d_{k1} \quad (6)$$

$$\langle i_{ot} \rangle_T = \frac{1}{2} \cdot (i_p + i_{fw1}) \cdot d_{t1}. \quad (7)$$

From the above equations (1)-(7), the quiescent operating point is determined. At the operating point, the small signal gain $G_1(s)$ from $\hat{i}_p$ to $\hat{i}_{f1}$ can be calculated by constructing perturbation variable matrices.

B. Case-II : Buck $>$ Boost

When the power of boost output is smaller than that of buck output, the current waveform is shown in Fig. 3(b). The duty cycle of each phase is given by

$$d_{k2} = \frac{f_s}{m_K} \cdot (i_{k2} - i_{fw3}) \quad (8)$$

$$d_{n2} = \frac{f_s}{m_{N1}} \cdot (i_p - i_{k2}) \quad (9)$$

$$d_{t2} = \frac{f_s}{m_T} \cdot (i_p - i_{fw2}) \quad (10)$$

$$d_{f2} = 1 - d_{k2} - d_{n2} - d_{t2} \quad (11)$$

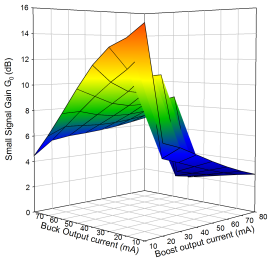


Fig. 4. Small signal gain G_0 versus load currents I_{ok} and I_{ot}

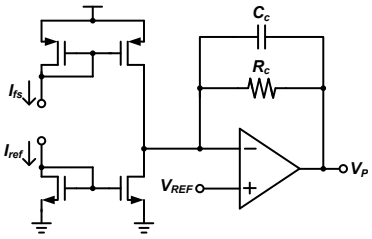


Fig. 5. Peak-current control circuit

$$d_{k3} = \frac{f_s}{m_K} \cdot (i_p - i_{fw2}) \quad (12)$$

$$d_{n3} = \frac{f_s}{m_{N2}} \cdot (i_p - i_{k3}) \quad (13)$$

$$d_{t3} = \frac{f_s}{m_T} \cdot (i_{k3} - i_{fw3}) \quad (14)$$

$$d_{f3} = 1 - d_{k3} - d_{n3} - d_{t3}, \quad (15)$$

where m_{N2} is V_{OA}/L. The averaged freewheeling current, which should be equal to I_{ref}, is given by

$$\langle i_{f2} \rangle_T = \frac{1}{2} \cdot (d_{f2} \cdot i_{fw2} + d_{f3} \cdot i_{fw3}). \quad (16)$$

The averaged supplied currents to the buck and boost outputs are given by

$$\langle i_{ok} \rangle_T = \frac{1}{2} \cdot (i_{k2} + i_{fw3}) \cdot d_{k2} \quad (17)$$

$$= \frac{1}{2} \cdot \{(i_p + i_{fw2}) \cdot d_{k3} + (i_p + i_{k3}) \cdot d_{n3}\} \quad (18)$$

$$\langle i_{ot} \rangle_T = \frac{1}{2} \cdot (i_p + i_{fw2}) \cdot d_{t2} \quad (19)$$

$$= \frac{1}{2} \cdot (i_{k3} + i_{fw3}) \cdot d_{t3}. \quad (20)$$

The above equations (9)-(21) determine the quiescent operating point. At the operating point, the small signal gain $G_2(s)$ from $\hat{i}_p$ to $\hat{i}_{f2}$ can be obtained by using perturbation variable matrices. Fig. 4 shows the calculated gain G_0 versus buck and boost load currents where G_0 can be $G_{1,0}$ or $G_{2,0}$ according to the load condition. The design parameters are chosen as $L = 10$ μH, $V_{IN} = 3.7$ V, $V_{OK} = 1.8$ V, $V_{OT} = 5$ V, $f_s = 1$ MHz, and $I_{ref} = 30$ mA. The gain G_0 is considered to compensate for the freewheeling feedback loop in a peak-current control circuit.

C. Peak-Current Control Circuit

The peak-current control circuit, which is an integrator with one pole, is shown in Fig. 5. The value of I_{ref} is chosen for the freewheeling periods (D_{f1}, D_{f2} and D_{f3}) to be larger than 0.1 for accurate operation because a freewheeling current sensor takes time to transition from an off-state to an on-state. Adequate freewheeling periods also guarantee good cross-regulation performance. I_{lps} (=I_{lp}/N_1) and I_{fs} (=I_f/N_2) are the scaled-down current from the peak-current sensor and the freewheeling current sensor, respectively. The loop gain of the freewheeling feedback loop is given by

$$T(s) = \frac{N_1}{N_2 \cdot R_P} \cdot G(s) \cdot A(s) = \frac{1}{R_P} \cdot \frac{G_0 \cdot R_c}{1 + sR_c \cdot C_c}, \quad (21)$$

where $N_1 = N_2 = N$ and R_P is the value of the resistor in the I-V converter (I-V conversion ratio). Generally, the unity gain frequency of a feedback loop, which should be sufficiently lower than the Nyquist rate, is set at one tenth of the switching frequency. Because the effective frequency of the inductor current waveform for case-II is one half of the switching frequency f_s, the unity gain frequency ($f_u = G_0/(2\pi \cdot R_P \cdot C_c)$) of the freewheeling feedback loop is designed to be about $f_s/20$.

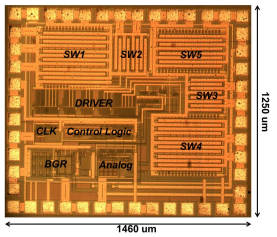
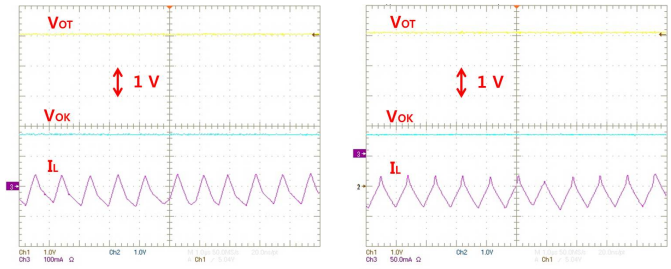


Fig. 6. Micrograph of the proposed SIMO DC-DC converter



(a) (b)

Fig. 7. Inductor current waveforms for (a) case-I (I_{OK}=10 mA and I_{OT}=80 mA) and (b) case-II (I_{OK}=80 mA and I_{OT}=10 mA)

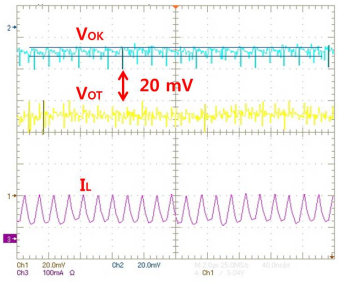
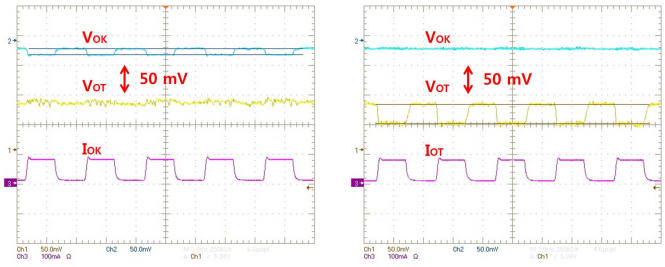


Fig. 8. Maximum output ripples for I_{OK}=80 mA and I_{OT}=80 mA



(a) (b)

Fig. 9. Load transient response for (a) I_{OK} changes of 10 mA to 80 mA under I_{OT}=10 mA and (a) I_{OT} changes of 10 mA to 80 mA under I_{OK}=10 mA

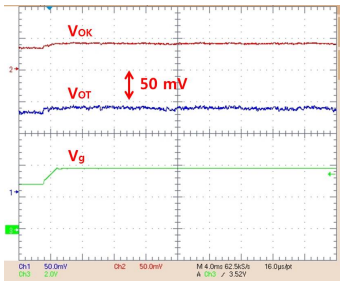


Fig. 10. Line transient response for line variations of 3 V to 4 V with I_{OK}=40 mA and I_{OT}=40 mA

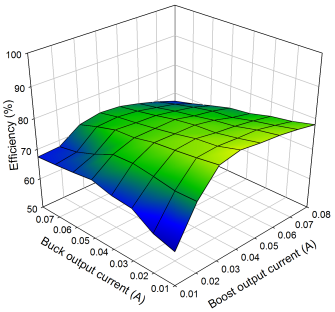


Fig. 11. Conversion efficiency of the proposed SIMO DC-DC converter

IV. Measurement Results

The proposed SIMO DC-DC converter is implemented in a 0.35-μm CMOS technology. The chosen design parameters were as follower: $C_{OK} = C_{OT} = 22$ μF, $L = 10$ μH, $V_{IN} = 3.7$ V, $V_{OK} = 1.8$ V, $V_{OT} = 5$ V, and $f_s = 1$ MHz. Fig. 7 shows the measured inductor current waveforms. The operation mode changes according to the output load condition. Fig. 8 shows the maximum output ripples for the maximum output load currents. The maximum output ripples of the buck and boost outputs are 5.6 mV and 4.8 mV, respectively. Because the operation of the proposed scheme is even stable for the small value of ESR, output voltage ripples can be minimized. Fig. 9 shows the load transient response when pulse loads of 10 mA to 80 mA are applied. The load regulations of the buck and boost outputs for the load current variations are 10 mV and 32 mV, respectively. Fig. 10 shows the line transient response for step line changes between 3 V and 4 V. The line regulations of the buck and boost outputs for the line variations are 7 mV and 7 mV, respectively. The power conversion efficiency of the proposed SIMO DC-DC converter is shown in Fig. 11. It is verified that high conversion efficiency is achieved regardless of the output load condition. There is no conversion efficiency drop according to mode change at the load balance boundary. The proposed scheme achieves the maximum conversion efficiency of 82 % under heavy load conditions. Table II summarizes the key performances of the proposed SIMO DC-DC converter.

TABLE II
Performance Summary

Process	0.35-μm CMOS	
Chip area	1460 μm x 1250 μm	
Input voltage	3.7 V (3 - 4 V)	
Switching frequency	1 MHz	
Inductor	10 μH (400 mΩ DCR)	
Output capacitor	22 μF (10 mΩ ESR)	
Converter type	Buck (V_{OK})	Boost (V_{OT})
Output voltage	1.8 V	5 V
Maximum load current	80 mA	80 mA
Output ripples	5.6 mV	4.8 mV
Load regulation	0.142 mV/mA	0.457 mV/mA
Line regulation	7 mV/V	7 mV/V

V. Conclusion

In this paper, a single-inductor multiple-output (SIMO) DC-DC converter capable of regulating buck and boost outputs with non-load-balance-dependent high efficiency is proposed and implemented. By adopting the newly proposed control sequence, input energy can be delivered to the outputs through a lossless inductor continually without a current accumulation problem. Thus, the proposed SIMO DC-DC converter can achieve high efficiency unrelated to the load condition. Implemented in a 0.35-μm CMOS technology, the measurement results of the proposed SIMO DC-DC converter show even a conversion efficiency of 82% under heavy load conditions.

Acknowledgment

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