A 0.5V, 2.41GHz, 196.3dBc/Hz FoM Differential Colpitts VCO with an Output Voltage Swing Exceeding Supply and Ground Potential Requiring No Additional Inductor

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***Abstract* — A low-voltage differential Colpitts VCO that achieves an output voltage swing above the supply voltage and below the ground potential to improve the phase noise while requiring no additional inductor for a small chip area is proposed. Implemented in a 65nm CMOS process, the proposed VCO achieves the phase noise of -131.05dBc/Hz at an offset of 1MHz from an oscillation frequency of 2.41GHz and a FoM of 196.3dBc/Hz while dissipating 1.74mW from a 0.5V supply.**

***Index Terms* — Oscillators, voltage-controlled oscillator (VCO), phase noise.**

I. Introduction

As CMOS technologies continue to be scaled down to reduce cost, increase speed, and achieve higher levels of integration, small and low-voltage voltage-controlled oscillators (VCOs) are highly demanded. However, the low-supply voltage severely limits the output voltage swing and therefore the output power of the VCO, thereby degrading the phase noise. To overcome the limitation of the low-supply voltage, the tail current sources of typical VCOs (both cross-coupled and Colpitts) have been replaced with inductors in [1-3]; this opens up an opportunity to increase the output voltage swing of the VCO above the supply voltage and below the ground potential, which leads to higher output power and lower phase noise [1-3]. Furthermore, capacitive feedback and forward-body-bias (FBB) techniques have been shown to be effective in improving the output voltage swing and phase noise, as well as the frequency tuning range [2].

Fig. 1 shows the schematics of the low-voltage VCOs reported in earlier work [1-3], where large output voltage swings and lower phase noise are achieved by adopting a voltage swing enhancement technique, that is, above the supply voltage and below the ground potential. The key issue with the designs shown in Fig. 1 is that each VCO requires an additional inductor, L_S, in addition to the LC-tank inductor L_{Tank}. The added inductor translates to an increased chip area and a higher cost, as the inductor occupies a large area on the chip and the inductor sizes are not scaled with technology. In order to resolve the trade-off between the phase noise and chip area at a low voltage, this paper proposes a VCO topology that requires no additional inductor while still achieving an output voltage swing above the supply voltage and below the ground potential.

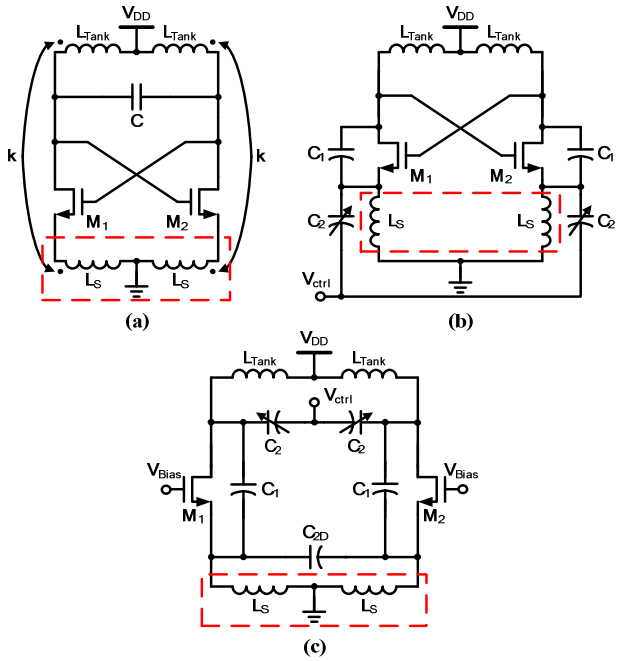

Fig. 1. Conventional low-voltage VCOs: (a) transformer feedback VCO [1], (b) cross-coupled Colpitts VCO [2], (c) enhanced swing differential Colpitts VCO [3]

II. Proposed Low Voltage VCO

Fig. 2 shows the circuit schematic and the waveforms of voltage swing (V_{out+}, V_{out-}, V_{s3}, and V_{s4}) of the proposed VCO. In Fig. 2(a), in order to accommodate a low supply voltage, the proposed VCO does not utilize current source transistors. The LC-tank of the proposed VCO is coupled to the gate nodes of M_3 and M_4 and forms a differential Colpitts oscillator with capacitive divider $C_1(=C_1')$ and C_2 $(=C_2')$. The cross-coupled transistors M_1 and M_2 provide negative resistance to compensate the loss of the tank and help the oscillator start-up. The differential output voltage

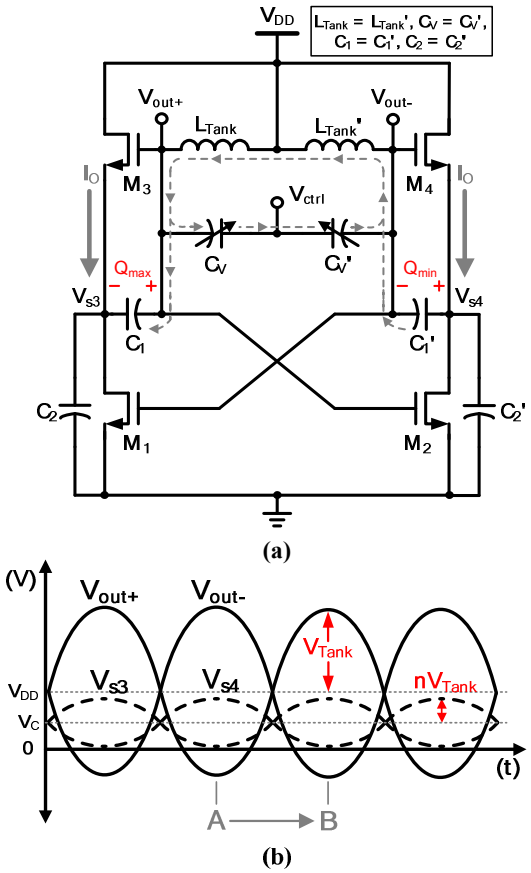

Fig. 2. Proposed VCO: (a) schematic and (b) waveforms of V_{out+}, V_{out-}, V_{s3}, and V_{s4}

swings at the nodes V_{out+} and V_{out-} and the voltage swings at node V_{s3} and V_{s4} are determined by the capacitive division of C_1 and C_2. In order to demonstrate the enhancement of the output voltage swing, the steady-state operation of the proposed VCO is explained over the period of point from A to B, as depicted in Fig. 2(b). While V_{out+} changes from the minimum peak to the maximum peak voltage, the current of L_{Tank} charges C_V and C_1 until the charge stored in C_1 reaches up to Q_{max}:

$$\begin{aligned} Q_{\max} &= C_1 \cdot (V_{out+} - V_{s3}) \\ &= C_1 \cdot (V_{DD} + V_{Tank} - V_C - nV_{Tank}) \end{aligned} \quad (1)$$

where V_{Tank} is the amplitude of the output voltage swing, V_C is the bias voltage of V_{s3} and V_{s4} during the steady-state oscillation, and $n=C_1/(C_1+C_2)$. In the meantime, V_{out-} changes from the maximum to the minimum and the charge stored in C_V' and C_1' flows through L_{Tank}'. Thus, at point B, the charge stored in C_1' becomes Q_{min}:

$$\begin{aligned} Q_{\min} &= C_1' \cdot (V_{out-} - V_{s4}) \\ &= C_1' \cdot (V_{DD} - V_{Tank} - V_C + nV_{Tank}). \end{aligned} \quad (2)$$

This cyclostationary operation continues during the oscillation. As the minimum voltage of V_{s3} and V_{s4} is limited to the ground potential by the switching operation of M_1 and M_2 during the oscillation period, Q_{min} can be redefined as

$$Q_{\min} = C_1' \cdot (V_{DD} - V_{Tank}) \quad (3)$$

at the minimum voltage of V_{out-}. If V_{Tank} becomes larger than V_{DD}, Q_{min} reverses its polarity, which can be caused by the continued discharging operation of C_1' through L_{tank}' without being limited by the ground potential. Eventually, voltage across C_1' reverses its polarity and V_{out-} can swing below the ground potential.

As V_{Tank} in the proposed VCO is required to be larger than V_{DD} in order to swing below the ground potential, V_{Tank} is needed to be analyzed quantitatively. The maximum current flowing through M_3 and M_4, I_O, can be approximated by the maximum drain current with the transistor operating in the triode region

$$\begin{aligned} I_o \approx \mu_n C_{ox} \frac{W}{L} \cdot \{ &(V_{DD} + V_{Tank} - V_C - nV_{Tank} - V_t)(V_{DD} - V_C - nV_{Tank}) \\ &- \frac{1}{2}(V_{DD} - V_C - nV_{Tank})^2 \} \end{aligned} \quad (4)$$

where V_t is the threshold voltage of the MOSFET. By adopting the derivation process for V_{Tank} of the Colpitts oscillator introduced in [4, 5], the maximum voltage swing across the LC-tank of the proposed VCO can be given by

$$V_{Tank} \approx n \cdot I_o \cdot R_p \quad (5)$$

where R_p represents the parallel resistance of the tank. Substituting (4) into (5), and solving for V_{Tank}, it can be shown that

$$V_{Tank} \approx \frac{1}{2} \cdot (V_{DD} - V_C) \cdot \frac{C_1 + C_2}{C_1} \quad (6)$$

assuming

$$n(1-n) > \frac{L}{\mu_n C_{ox} W \cdot R_P}. \quad (7)$$

From (6), V_{Tank} can be determined by the selection of the C_2/C_1 ratio as V_{DD} is fixed and V_C is determined by the voltage swing amplitude, nV_{Tank}, of V_{s3} and V_{s4}. For a sufficiently large value of C_2/C_1, V_{Tank} can be larger than V_{DD} and the output voltage swing can go below the ground potential. For example, in the case of V_{DD}=0.5V, C_2/C_1=5, and V_C=0.25V, from (6), V_{Tank} is 0.75V, which is larger value than V_{DD} of 0.5V. Thus, V_{out+} and V_{out-} can swing from -0.25V to 1.25V.

Fig. 3 shows the simulated output voltage waveforms of the proposed VCO for two states of the C_2/C_1 ratio (C_2/C_1=1 and 5). For the C_2/C_1 ratio of 1, the simulated value of V_C is 0.15V and V_{Tank} is about 0.365V, which is smaller than the supply voltage of 0.5V. Thus, the output voltages still swing above the ground potential. For the C_2/C_1 ratio of 5, on the other hand, the simulated value of V_C is 0.25V and the output amplitude V_{Tank} becomes about

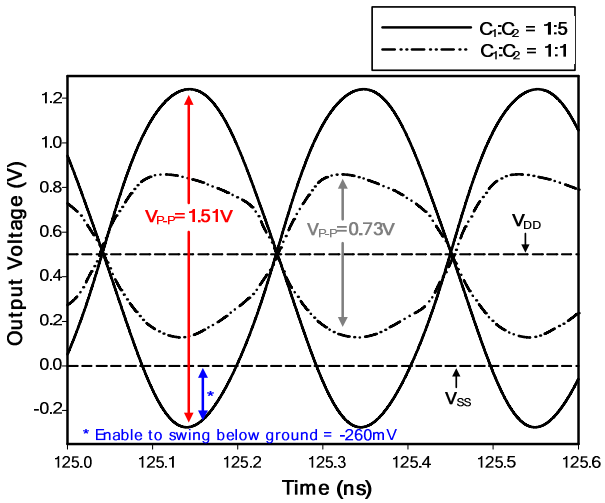

Fig. 3. The simulated output voltage waveforms of the proposed VCO for C_2/C_1 ratios of 1 and 5

0.755V, which is larger than the supply voltage of 0.5V. Eventually, the output voltage can swing below the ground potential. Thus, the proposed VCO is capable of generating an output voltage swing that goes above the supply voltage and below the ground potential without an additional inductor.

Fig. 4 shows the peak-to-peak output voltage amplitude, the phase noise at a 1MHz offset, the power dissipation, and the FoM of the proposed VCO as a function of the C_2/C_1 ratio, simulated at 2.41GHz. In Fig. 4(a), the amplitude of the output voltage increases with an increase in the C_2/C_1 ratio. For the supply voltage of 0.5V, the proposed VCO exhibits voltage swing below the ground potential for $V_{p\text{-}p}$ in excess of 1V, which corresponds to a capacitance ratio of approximately 1.8 (C_2/C_1 = 1.8). As expected, the phase noise is improved with an increase in the C_2/C_1 ratio. However, the capacitance ratio cannot be set arbitrarily high as the required current for the start-up of the oscillator is also proportional to C_2/C_1. Fig. 4(b) shows that the power dissipation of the proposed VCO is increased with an increase in the C_2/C_1 ratio. This constitutes a trade-off between the phase noise and power dissipation [4] that must be considered when selecting the C_2/C_1 ratio in order to achieve the highest FoM as shown in Fig. 4(b), where the FoM peaks at around a C_2/C_1 ratio of 5.

III. Measurement Results

The proposed VCO is implemented in a 65nm CMOS process to operate from a 0.5V supply while dissipating 1.74mW, and the chip occupies 0.17 mm^2 as shown in Fig. 5. A center-tapped inductor of 3.8nH is chosen for the LC-

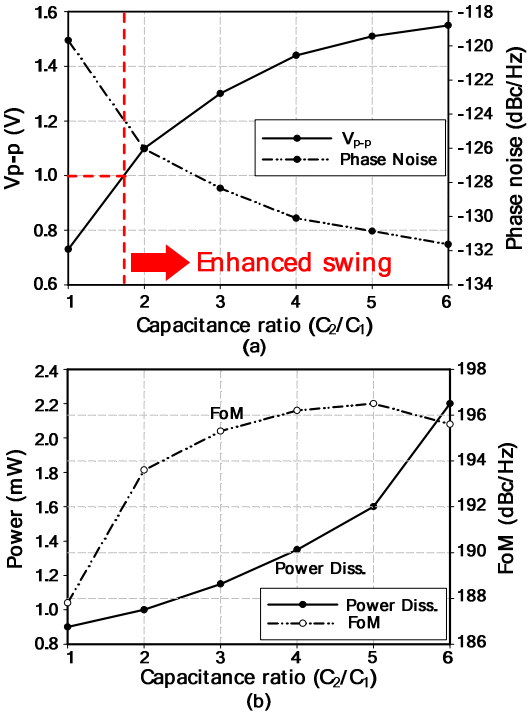

Fig. 4. Simulated VCO performance vs. C_2/C_1 ratio (a) peak-to-peak output voltage swing and phase noise (b) power dissipation and FoM

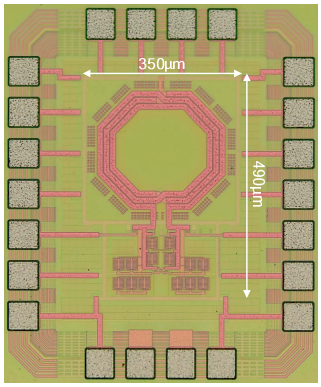

Fig. 5. Chip micrograph of the proposed VCO

tank. The frequency tuning capacitors are implemented with MOS-varactors while MIM-capacitors are selected for C_1 and C_2 with values of C_1=1pF and C_2=5pF, respectively. For the tuning voltage of from 0V to 0.5V, the VCO frequency varies from 2.35GHz to 2.48GHz. The measured phase noise is shown in Fig. 6. For an oscillation frequency of 2.41GHz, the measured phase noise is -131.05dBc/Hz at a 1MHz offset. Table I presents a performance summary in comparison with recent state-of-the-art low-voltage VCOs. In order to provide a fair comparison with other reported works at different center frequencies (f_o) and power consumption (P_{DC}), a FoM, as defined below, is used:

TABLE I
Measured Performance Summary in Comparison with State-Of-The-Art Low Voltage VCOs

	This work	[1] JSSC 05	[2] MTT 07	[3] JSSC 11	[6] MWCL 10
Technology	65nm	180nm	180nm	130nm	130nm
Supply Voltage [V]	0.5	0.5	0.6	0.475	0.3
Frequency [GHz]	2.41	3.8	5.6	4.9	3.579
Tuning Range [GHz]	2.35 – 2.48 (5.4%)	3.65 – 3.76 (3%)	5.4 – 5.85 (8.1%)	4.85 – 4.97 (2.5%)	3.39 – 3.63 (6.8%)
Phase Noise / Δf [dBc/Hz]	-131.05 / 1MHz	-119.0 /1MHz	-118.0 / 1MHz	-136.2 / 3MHz	-116.88 / 3MHz
Power Consumption [mW]	1.74	0.57	3	2.7	0.225
FoM [dBc/Hz]	196.3	193	189	196.2	194.43
Added Inductor (L_S)	**X**	**O**	**O**	**O**	**O**
Oscillator Description	Enhanced Swing	Enhanced Swing	Enhanced Swing	Enhanced Swing	Enhanced Swing

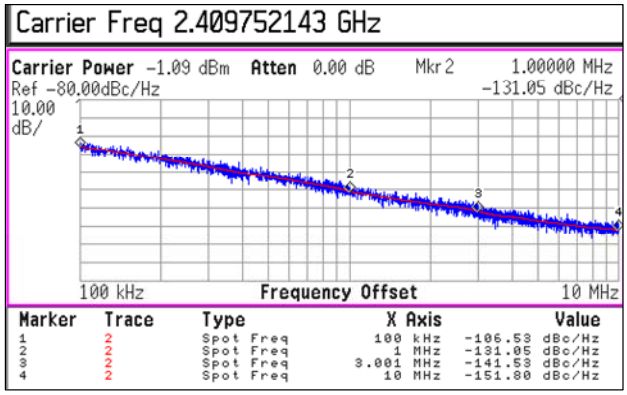

Fig. 6. Measured phase noise of the proposed VCO.

$$FoM = 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{DC}}{1mW}\right) - L\{\Delta f\} \qquad (8)$$

where Δf is the offset frequency and $L\{\Delta f\}$ is the phase noise of the VCO. The proposed VCO achieves a FoM of 196.3dBc/Hz, the best performance reported to date. Nonetheless, it requires no additional inductor, in contrast to other VCOs which adopt voltage swing enhancement techniques [1- 3, 6]. The chip size of the proposed VCO is not directly compared with other VCOs based on voltage-enhancement techniques in Table I, because the size of LC-tank inductor becomes different for different oscillation frequencies and also does the pad size for each technology. However, it is obvious that the proposed design offers an advantage in the chip size as it requires fewer inductors.

IV. Conclusion

We present a low-voltage differential Colpitts VCO for low phase noise and a small chip area. The proposed VCO achieves enhanced output voltage swing above the supply voltage and below the ground potential by the combination of the differential output at the gate nodes of the feedback transistors and the capacitive dividers, without requiring an additional inductor. The VCO is implemented in a 65nm CMOS process to operate from a 0.5V supply while dissipating 1.74mW. For an oscillation frequency of 2.41GHz, the measured phase noise is -131.05dBc/Hz at a 1MHz offset. The FoM of the proposed VCO is 196.3dBc/Hz which is the best performance to date as a low-voltage VCO.

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