A Low Power Low Inaccuracy Linearity-Compensated Temperature Sensor for Attachable Medical Devices

Oh-Yong Jung, Seungjin Kim, Sok-Kyun Han and Sang-Gug Lee
Department of Electrical Engineering
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon, Republic of Korea
Email : {id1232, sj-kim, sskk}@kaist.ac.kr, sglee@ee.kaist.ac.kr

Abstract— In this paper, an accurate, low power CMOS temperature sensor for attachable medical devices (AMDs) is presented. The proposed temperature sensor consists of a high-slope proportional to absolute temperature (PTAT) current and reference voltage generator, a current controlled relaxation oscillator (ICRO), a digital counter, and a reference clock generator. By adopting a temperature conversion linearity compensation technique, simulation results show -0.10℃ ~ +0.13℃ temperature inaccuracy in a range of 20℃ ~ 50℃ with a 100 samples/s sampling rate. The presented sensor dissipates 2uW under 1.2-V supply in a 0.13um CMOS technology.

I. INTRODUCTION

Research in the body sensor network (BSN) area has been intensified as researchers seek the capacity to monitor human body conditions at any time. A BSN is composed of devices called AMDs that combine medical sensors with a wireless communication system. The AMDs sense vital signs in real time and transmit the information to other devices using wireless communication. Depending on the purpose of the sensors, AMDs can be implemented in various ways. Body temperature sensing is one of the most important goals for AMDs, because a great deal of health information can be obtained and many conditions such as fever and hypothermia can be diagnosed by sensing body temperature. However, even a small error in body temperature can cause a serious medical misdiagnosis. Therefore, highly-accurate monitoring devices are required. Furthermore, an AMD should be designed with low power dissipation to meet the long-lasting battery requirement of wireless sensor devices.

Numerous ways to implement the sensor for temperature monitoring have been introduced [1], [2], [3]. Although a voltage monitoring ADC-based architecture has gained much interest for its accuracy-guaranteed characteristic, it suffers from high power dissipation and design complexity. Oscillator-based temperature sensors, that is, sensors that utilize a temperature-dependent frequency characteristic, have been used to monitor the ambient temperature. This type is implemented in a simple and low-power manner, because it utilizes a frequency counter instead of the ADC. However, the inaccuracy is large enough to cause serious errors in AMD applications due to nonlinear temperature-to-frequency conversion.

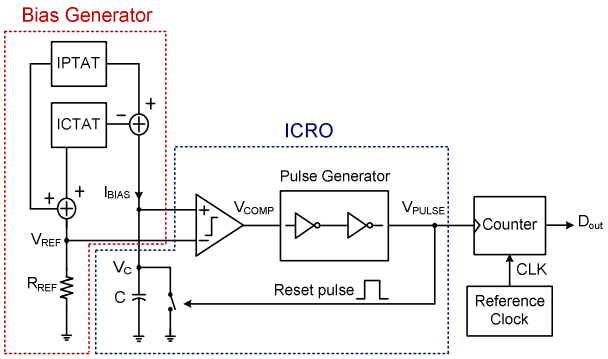

Figure. 1 Block diagram of the temperature sensor architecture.

In this paper, we propose a temperature conversion linearity compensation technique for an oscillator-based temperature sensor, thus achieving low power, high accuracy performance.

II. ARCHITECTURE

Fig. 1 shows the proposed linearity-compensated temperature sensor architecture, which consists of a bias generator, an ICRO, a counter, and a reference clock generator. The bias generator is composed of a PTAT current generator and a complementary to absolute temperature (CTAT) current generator. The summation and subtraction between the PTAT and CTAT current generates a temperature-independent reference voltage and a high-slope, low-offset PTAT current, respectively. The MOSFET devices in the bias generator operate in the subthreshold region for lower power dissipation. The bias current is fed to the current-mode comparator and the integral capacitor to further reduce the power consumption [4]. An ICRO and a counter are devoted to current-to-frequency conversion and frequency-to-digital code conversion. A pulse generator in the ICRO generates a resetting pulse to dump the charge in the integral capacitor with a modulated pulse-width

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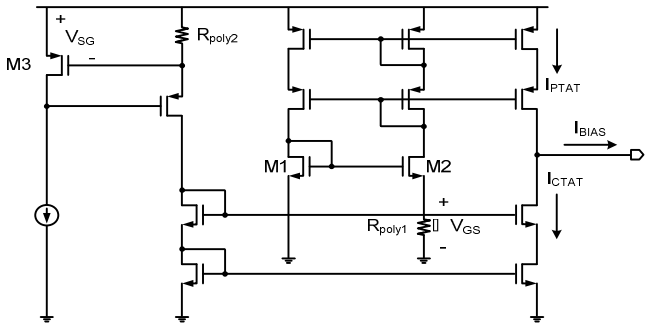

Figure 2. Simplified schematic of the proposed bias current generator.

to implement the linearity compensation technique. There is an additional constant-frequency clock generator to make an internal reference clock. The constant-frequency pulse is used by the counter in order to achieve temperature-independent counting.

III. NONLINEARITY IN TEMPERATURE TO CURRENT CONVERSION

As long as the frequency is an ideal first order function of temperature and the counter has adequate resolution, 2-point calibration will lead to zero-error temperature sensing. However, there are various nonlinear effects that increase inaccuracy. In this section, the nonlinearity effects of the temperature sensing block are described in order to find a linearity improvement method.

The methods of PTAT and CTAT characteristic generation are well-known and have been used in various applications. Generally, a PTAT characteristic is generated by using the devices that execute exponential behavior of the voltage-to-current conversion, such as BJTs and subthreshold MOSFETs. A CTAT characteristic comes from process-dependent parameters such as the threshold voltage and the mobility of MOSFETs. Since the temperature-related characteristics of the PTAT current are easier to handle than those of the CTAT current, the PTAT current is more useful to sense temperature variation.

In the proposed bias generator, a high-slope PTAT-based current is utilized. Fig. 2 shows a schematic of the high-slope PTAT current generator. Specifically, it is used for the ICRO to generate a temperature-controlled frequency. The rapid variation of frequency is advantageous in terms of the resolution. By subtracting the current that has different polarity of the temperature coefficient, the resulting current will have a high-slope conversion characteristic. The summation of the PTAT and CTAT current generates the temperature-independent reference voltage, which is essential to make a standard for comparison of the temperature-dependent variations. Since the subthreshold MOSFET has relatively small area and shows low-power dissipation, it is better for low-cost, low-power applications as compared with the BJT. A low voltage bandgap reference using subthreshold MOSFETs is a good choice in this case [5].

In the subthreshold region, the gate-source voltage difference of M1 and M2 is approximately given by

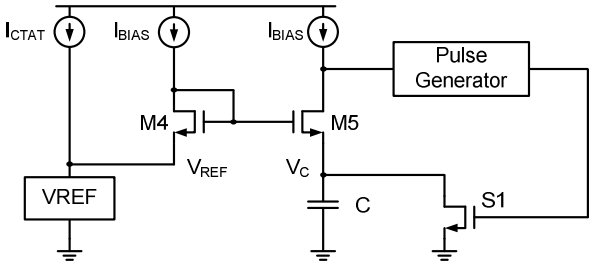

Figure 3. Simplified schematic diagram of the proposed ICRO.

$$\Delta V_{GS} = V_{GS1} - V_{GS2} \approx \frac{nk_B T}{q} \cdot \ln\left(\frac{K_2 I_1}{K_1 I_2}\right) \quad (1)$$

where K is the aspect ratio (=W/L) of the transistor, k_B the Boltzmann constant, n the nonlinear subthreshold slope factor, T the absolute temperature, q the charge and I the drain current of the transistor. If each current of M1 and M2 is the same, ΔV_{GS} has a PTAT characteristic controlled by the device size. Despite the linear conversion characteristic of ΔV_{GS}, various factors can degrade the linearity. For example, the CTAT characteristic of the p-type poly resistance (R_{poly}) can cause nonlinearity of temperature-to-current conversion. Considering this nonlinearity, PTAT current is represented as

$$I_{PTAT} \approx \frac{\Delta V_{GS}(T_0)}{R_{poly1}(T_0)} \cdot \left(1 + (K_P + K_R)\Delta T + (K_P K_R + K_R^2)\Delta T^2 + \cdots\right) \quad (2)$$

where K_P and K_R are positive temperature coefficients of ΔV_{GS} and R_{poly}, ΔT (=T-T_0) the temperature difference between T and the reference temperature (T_0), and $\Delta V_{GS}(T_0)$ the gate-source voltage difference at T_0. As shown in equation (2), second and higher order components of ΔT are generated. The second order component is the most important factor because it causes the dominant nonlinearity in the temperature-to-current conversion. Thus, an increase of the second order coefficient due to the poly resistor degrades the linearity. The CTAT current shows a more linear characteristic because of the cancellation of the temperature coefficients between V_{SG} and the resistor. It can be represented as

$$I_{CTAT} \approx \frac{V_{SG}(T_0)}{R_{poly2}(T_0)} \cdot \left(1 - (K_C - K_R)\Delta T - (K_C K_R - K_R^2)\Delta T^2 + \cdots\right) \quad (3)$$

where K_C is a positive temperature coefficient of V_{SG} and $V_{SG}(T_0)$ the gate-source voltage of M3 at T_0. K_C-K_R takes a positive value. The weighted subtraction of the PTAT and CTAT current provides the high-slope PTAT bias current. Since these currents have opposite polarity of the first and second order coefficients, the subtraction achieves a high-slope but less-linear conversion characteristic. The bias current is given by

$$I_{BIAS} \approx I_{BIAS0} \cdot \left(1 + K_{B1}\Delta T + K_{B2}\Delta T^2 + \cdots\right) \quad (4)$$

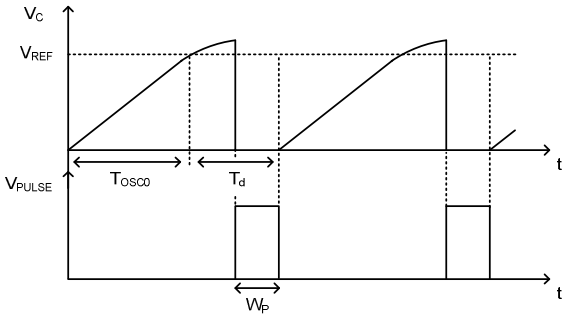

Figure 4. Practical sawtooth waveform including T_d.

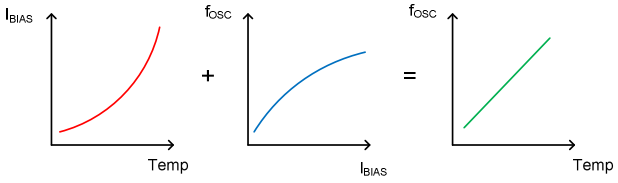

Figure 5. Nonlinearity cancellation process.

where I_{BIAS0} is the bias current at T_0, and K_{B1} and K_{B2} are positive and include K_R, K_C, K_P and other nonlinear factors. Because the temperature variation is only sensed by this bias current, the nonlinearity in I_{BIAS} can cause a serious decrease of accuracy. Therefore, cancellation of the dominant nonlinearity is essential for accurate sensing.

IV. Linearity Compensation

In this paper, a linearity-compensated current controlled relaxation oscillator (ICRO) is proposed. The inherent characteristics of a relaxation oscillator can be utilized to cancel out the nonlinearity from the bias current generator.

Fig. 3 shows the schematic of the ICRO. A current mode comparator is used and it compares the reference voltage (V_{REF}) to the integral capacitor voltage (V_C) that has a current-proportional slope. When V_C exceeds V_{REF}, the drain voltage of M5 shows a rapid increase and becomes the input of the pulse generator, which makes a pulse to discharge the capacitor. This charging and discharging repetition makes a sawtooth voltage waveform at V_C and its oscillation frequency (f_{OSC}) is given by

$$f_{OSC} = \frac{1}{T_{OSC0}} = \frac{I_{BIAS}}{CV_{REF}} \tag{5}$$

where T_{OSC0} is the period of oscillation and C the capacitance of the integral capacitor. f_{OSC} ideally shows a proportional-to-bias current characteristic. However, the ICRO has an unexpected delay (T_d) caused by extra factors such as the small comparator gain and the excess discharging pulse-width (W_P). Fig. 4 shows the practical sawtooth waveform including T_d and the effect of the pulse-width. Considering T_d, the equation of f_{OSC} should be changed to

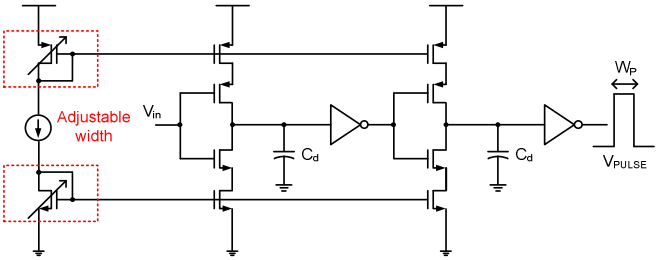

Figure 6. Simplified schematic of the adjustable pulse-width generator.

$$f_{OSC} = \frac{1}{T_{OSC0} + T_d} = \frac{1}{\frac{CV_{REF}}{I_{BIAS}} + T_d} = \frac{1}{CV_{REF}} \cdot \frac{I_{BIAS}}{1 + K_d I_{BIAS}}$$

$$\approx \frac{1}{CV_{REF}} \cdot \left(I_{BIAS} - K_d {I_{BIAS}}^2 + K_d^2 {I_{BIAS}}^3 - \cdots \right) \tag{6}$$

where K_d ($=T_d/CV_{REF}$) is a coefficient representing the nonlinearity of the current-to-frequency conversion. This additional nonlinearity has different polarity of the nonlinearity from the temperature-to-current conversion. Thus, nonlinearity cancellation occurs during the two-step conversion progress. Fig. 5 shows the graph of the cancellation between the temperature-to-current conversion and the current-to-frequency conversion. By summing the I_{BIAS} and f_{OSC} curves together, the nonlinearity of each conversion is easily cancelled out by their complementary curve shape. Using equations (4) and (6), f_{OSC} can be re-calculated as

$$f_{OSC} \approx \frac{I_{BIAS0}}{CV_{REF}} \cdot \left[1 - K_d I_{BIAS0} + K_{B1}(1 - 2K_d I_{BIAS0})\Delta T + K_{B2}\left(1 - \alpha K_d I_{BIAS0}\right)\Delta T^2 + \cdots \right] \tag{7}$$

where α is related with K_{B1} and K_{B2}. The third order and above polynomials of I_{BIAS} are ignored due to their negligible effect on the linearity. The dominant nonlinearity effect also comes from the second order polynomial of ΔT. Therefore, linearity compensation can be achieved by finding the optimum K_d that yields a zero-coefficient of ΔT^2.

One of the most feasible and practical ways to control K_d is to adjust T_d by changing the width of the capacitor reset pulse. Since the pulse-width is proportional to T_d, K_d has a proportional relationship with the pulse-width. In the ICRO, an adjustable pulse-width generator is proposed to control T_d, as presented in Fig. 6. The pulse is made by the sum of the inverter delays, which are controlled by adjusting the biasing current flow to the current starved inverter array. Fig. 7 shows the slope change resulting from the adjustment of T_d. The maximum absolute deviation from the average slope can be regarded as an index of the linearity performance. Because an increase of T_d leads to a negative value of deviation, there is an optimal point that yields zero-deviation. In the proposed temperature sensor, the values of the capacitance, V_{REF}, and I_{BIAS0} are designed as 1pF, 255mV, and 80nA respectively at

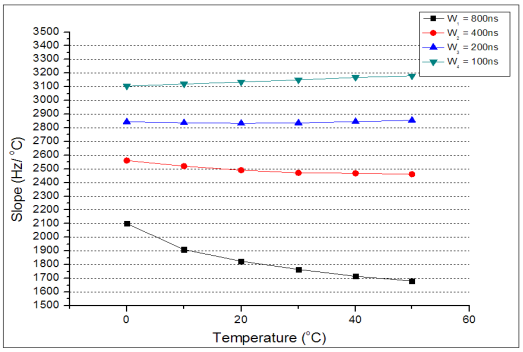

Figure 7. Simulated temperature-to-frequency conversion slope.

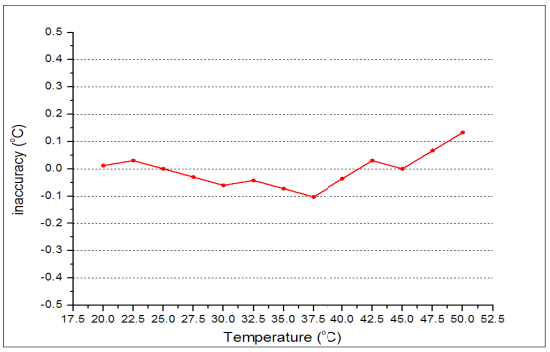

Figure 9. Simulated temperature inaccuracy.

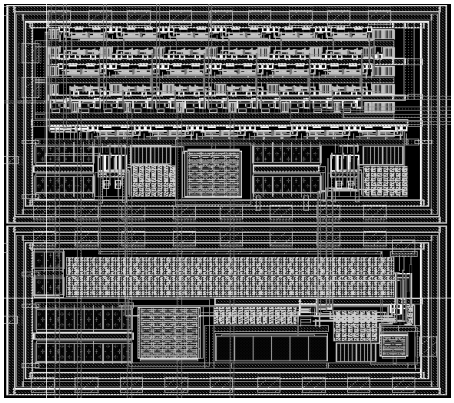

Figure 8. Layout of the temperature sensor.

room temperature. Thus, the simulated optimum value of the pulse-width is about 200ns, and total T_d is about 1us.

The nonlinearity can be suppressed externally, because the external selecting signals can limit the inverter biasing current by controlling the total width of the current mirroring transistors [6].

V. POST-LAYOUT SIMULATION RESULTS

As shown in Fig. 8, the proposed temperature sensor is implemented with an active area of 0.25mm^2 in a 0.13um CMOS process. The measurement range is from 20℃ to 50℃ with 0.048 ℃ /LSB resolution under 1.2-V supply while drawing 2uW at room temperature. After two-point calibration, as shown in Fig. 9, the simulated temperature error ranges from -0.10 ℃ to +0.13 ℃. By the adoption of an internal reference clock, a sampling rate of 100 samples/s is achieved, which is fast enough to measure body temperature. The performance of the temperature sensor along with a comparison with previous works is summarized in table I. The results show that the proposed temperature sensor has provides satisfactory accuracy performance in a low power consumption area of less than 2uW application.

VI. CONCLUSION

In this paper, a low power high accuracy CMOS temperature sensor for AMDs is presented. The proposed temperature sensor adopts an ICRO for low power consumption. Furthermore, a temperature conversion linearity compensation technique is used to alleviate the nonlinear characteristic arising from the temperature-to-frequency conversion. After the linearity compensation, simulation results show -0.10℃ ~ +0.13℃ inaccuracy in a range of 20℃ ~ 50℃ with a 100 samples/s sampling rate. The presented sensor dissipates 2uW under 1.2-V supply in a 0.13um CMOS technology.

TABLE I. PERFORMANCE COMPARISON OF TEMPERATURE SENSORS

Parameter	[1]	[2]	[3]	This work
Technology (um)	0.16	0.18	0.18	0.13
area (mm^2)	0.12	0.004	0.2	0.25
Inaccuracy (℃)	±0.2(3σ)	+1/-0.8	±1	+0.13/-0.10
Resolution (℃ /LSB)	0.015	0.035	0.14	0.048
Temperature range(℃)	-30~125	-10~30	27~47	20~50
Power Dissipation (uW)	7.4	0.11	0.9	2

VII. ACKNOWLEDGEMENT

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