A Low-Power Small-Size Transmitter with Discrete-Time Baseband Filter for LTE in 65 nm CMOS

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***Abstract*— This paper presents the design of a low-power small-size transmitter with discrete-time baseband filter for LTE application operating at 1.8-2 GHz. The transmitter achieves 4.5 dBm output power with more than -46 dBc of LO feedthrough suppression and -38 dBc image rejection ratio. At -0.3 dBm transmitted power of LTE 5 MHz channel, ACLR is measured below -42 dBc for both upper and lower channels with 1.83 and 2.47 % EVM for QPSK and 16-QAM modulation signals, respectively. The prototype chip is fabricated in a 65 nm CMOS technology and dissipates 59 mA current from 1.2 V supply and 13 mA from 2.5 V supply.**

I. INTRODUCTION

In recent years, Long-Term Evolution (LTE) standards have been widely used to provide 4G broadband mobile connectivity [1]. LTE supports both frequency-division duplex (FDD) and time-division duplex (TDD), as well as multiple bands from 700 MHz to 2.7 GHz. In addition, LTE standards support various channel bandwidths from 1.4 to 20 MHz with bandwidth-efficient digital modulation and multiplexing schemes such as QPSK, 16QAM, 64QAM and OFDM that lead to a high PAPR of transmission signals. Therefore, LTE transmitters require high linearity to reduce unwanted emissions of adjacent channels as defined in ACLR specifications. Besides, LTE transmitters are considered low spurious and noise at receiver bands in FDD modes or other band services in co-existed multi radios.

In conventional transmitters [2], [3], the baseband signals after DAC are processed by low-pass filters to suppress out-of-band noise, distortion and spurious. The filters typically implemented in active RC type are bulky and sensitive to process, voltage and temperature variations. To handle wide channel bandwidth, the active RC filters require wide gain-bandwidth product opamps that dissipate high power. Furthermore, the filter designs are challenged by low supply voltages in nanometer CMOS. In addition, the chip size and power consumption of baseband sections are also hard to scale down in CMOS technology.

With current trend toward SoC radios that integrates RF transceivers and digital baseband modems into a single chip, digital-intensive transmitter architectures are strongly desired. Direct digital to RF modulators (DRFM) that combine digital--to-analog conversion with up-conversion functions into a single digital-like block yield the advantages of CMOS scaling flexibility, small chip size and low power consumption [4], [5]. However the DRFMs lack filtering function presenting high noise floor of transmission spectrum. Thus a high bit-resolution modulator is required that leads to high power consumption for high sampling rate and calibration circuits. Although DRFMs with Finite Impulse Response (FIR) filter are used to suppress the quantization noise of the DRFMs, the architectures need parallel modulator paths that increasing chip sizes and power consumptions [6], [7].

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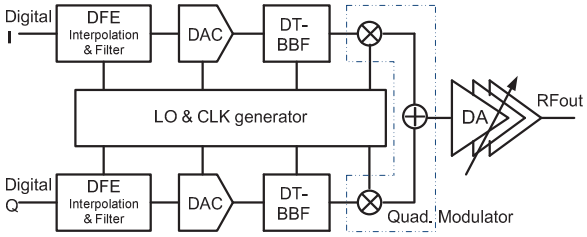

Fig. 1. Proposed transmitter architecture.

This paper presents a low-power small-size transmitter implemented in 65nm CMOS for LTE application. Instead of using high-order continuous-time lowpass filter, a compact 2nd-order Infinite Impulse Response (IIR) discrete-time filter is adopted after the DAC to suppress out-of-band noise, distortion and spurious emissions with the help of a high over sampling ratio. Based on passive switched-capacitor circuitry, the discrete-time baseband filter shows the advantages in high flexibility and less sensitivity to process, voltage and temperature variations, especially in nanometer CMOS technologies for the transmitter design.

II. TRANSMITTER ARCHITECTURE

The block diagram of the proposed transmitter architecture is shown in Fig. 1. The transmitter consists of I/Q digital front-ends (DFE), digital-to-analog converters (DAC), discrete-time baseband filters (DT-BBF), a quadrature direct conversion modulator and an RF programmable gain driver amplifier (DA) with LO and clock generation circuits.

As shown in Fig. 1, input digital baseband signals are processed by I/Q DFEs to re-sample and interpolate the

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original signals into higher sampling rate signals. The digital up-sampling signals are converted to analog signals by 12-bit DACs with high over-sampling ratio to reduce the quantization noise. The DAC sampling rates are selectable between 122.88 or 245.76 MHz for different LTE channel bandwidth modes. The quantization noises and DAC spurious images are suppressed further by the DT-BBFs. In this work, the clock frequency of the BBFs is twice that of DAC sampling rate to reduce aliasing emissions. The analog sampled signals are then up-converted and amplified to RF output signals by the quadrature modulator and driver amplifier.

III. Circuit Designs

This section describes the transmitter implementation details after digital baseband signal processing and digital-to-analog conversion.

A. Discrete-Time Baseband Filter

Fig. 2 shows the single-ended half-circuit schematic and clock diagram of the DT baseband filter. The filter operates in charge-domain (or current) sampling mode for built-in anti-aliasing rejection. In order to avoid non-linearity of I-V and V-I conversions, the I-I converter is applied to receive the DAC current. The output current of the current-steering DAC is divided into lower baseband current for saving power consumption and capacitor sizes of the filter stage.

The I-I converter is implemented with low-voltage cascode current mirror as depicted in Fig. 2. The cascode current mirror will copy the linear DAC output current to the baseband current that drives the discrete-time filter with high accuracy to maintain the linearity of DAC output current. The current mirror dissipates 410 uA static current from 1.2 V supply while the diode-connected cascode load reuses the 5 mA bias current of the DAC for each I/Q channels.

After scaled by the I-I converter, the baseband current is sampled on to the non-reset history capacitor C_H and resettable sampling capacitors C_{S1} and C_{S2} to form the *sinc* built-in anti-aliasing function and the first passive IIR pole. The sampled data on identical sampling capacitors C_{S1} and C_{S2} are then read out alternatively through RD_1 and RD_2 switches with the buffer capacitor C_B to create the second passive IIR pole. After the read-out phase, the rotation sampling capacitors are reset (phase R_1 or R_2 = HIGH) before new samples arrives (phase S_1 or S_2 = HIGH). A two-channel time-interleave sampling structure is used to ensure that the *sinc* nulls of the DT baseband filter would be allocated at every multiples of the sampling clock. The time-interleaved filter also provides double sampling to relax noise folding with low power consumption.

Cut-off frequency of the DT baseband filter is programmed by 4-bit C_H and C_B capacitor banks to configure 1.4 – 20 MHz LTE channel bandwidths. The filter is driven by a non-overlap 4-phase clock pattern shown in Fig. 2. The 4-phase clock is generated by a low power TSPC DFF counter with non-overlap combination logic gates. The simple clock scheme offers compact size and low power to the clock generator design and low noise to the baseband filter.

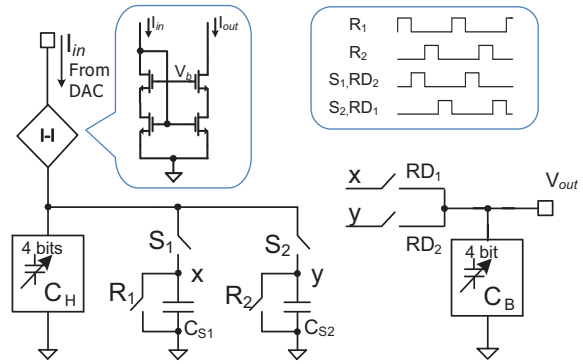

Fig.2. Simplified schematic and clock diagram of the DT baseband filter.

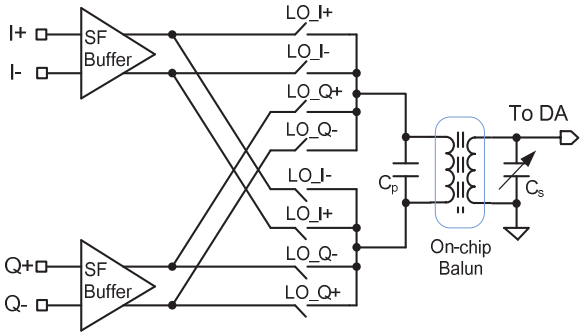

Fig.3. Quadrature modulator using passive voltage mixers.

B. Quadrature Modulator

A traditional current mode Gilbert active mixer suffers from up-converted baseband noise, and high power consumption is needed to make an intrinsically low noise mixer design. In contrast, the passive mixer is an attractive candidate due to its low voltage headroom, low-noise and high-linearity [2]. The simplified schematic of the quadrature modulator using passive up-conversion mixers is shown in Fig. 3. The quadrature modulator includes I/Q source follower (SF) buffers, switching quads and transformer balun load with 25% duty-cycle LO.

Since the passive mixer have low isolation between RF and IF ports and the 2*LO frequency can appear at the I/Q baseband sides that create unwanted harmonic emission, the buffer is needed to reduce interactive-effect between the discrete-time filters and mixing quads. The buffers are implemented with I/Q source followers dissipating 6 mA from 1.2 V supply. The output impedance of the buffers are designed to be 50 Ohm that is low enough to drive the 300-Ohm equivalent load without scarifying linearity while the power consumption is saved.

The RF signal at the passive mixer output is passed to the driver amplifier (DA) through an on-chip 1:1.5 turns-ratio balun. Through this balun, the differential mixer output signal are converted to a single ended signal with about 3 dB voltage gain. A 5-bit MIM capacitor bank has been employed at the secondary side of the transformer to tune the resonated frequency into the range of 1.8-2 GHz. The balun could be

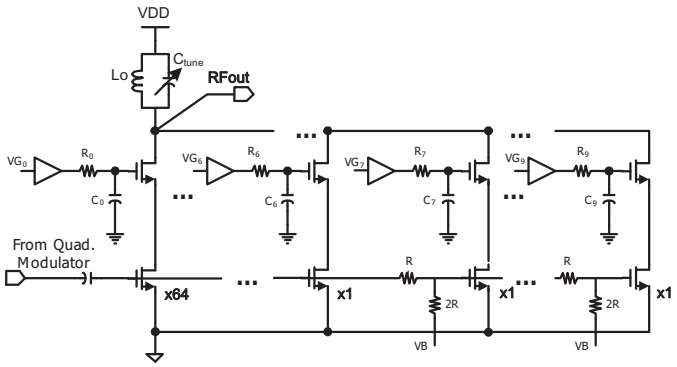

Fig.4. Schematic of the programable gain driver amplifier.

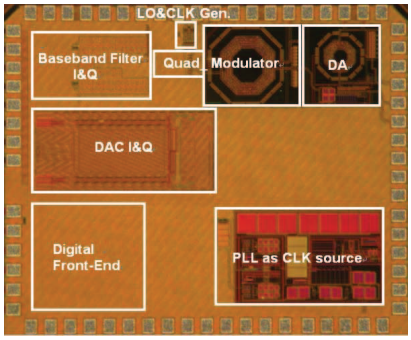

Fig. 5. Chip photograph of the proposed transmitter.

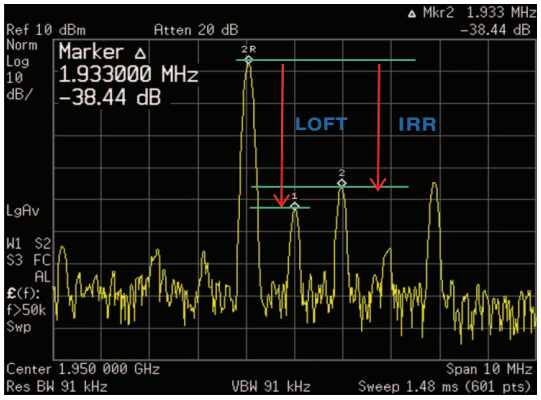

Fig. 6. Measured output spectrum of transmitter for signle tone test.

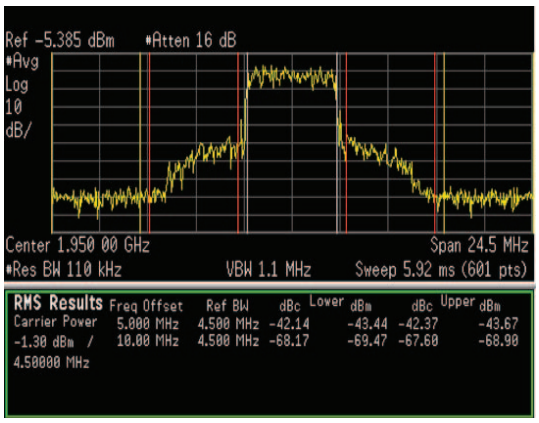

Fig. 7. Measured ACLR with LTE 5 MHz channel bandwidth.

emplaced at the DA output for better supply noise rejection. However, in that case, the differential DA will dissipate high power or the turns-ratio of the balun must be increased to 2:1 for the same power consumption and gain in driving 50 Ohm load. Increasing the turns-ratio of balun leads to large insertion loss in balun and high output swing at the DA output reducing linearity and degrading reliability of cascode transistors in the DA.

C. Driver Amplifier

The last stage of the transmitter chain is the DA. As shown in Fig. 4, the DA core is a single-ended cascode amplifier with tuned output load for low noise and low power. Gain control is achieved by switching the binary-weighted parallel-placed cascode transistors. The DA is designed for the gain range of 60 dB with 6dB steps by a 10-bit gain control scheme. The MSB 7-bit gain is controlled by binary-weighted transconductor cells, while the LSB 3-bit gain is controlled by a R-2R voltage divided ladder with unit transconductor cells.

In Fig. 4, the cascode transistors suffere from large drain voltage swings at high output power modes. If the gate voltage of the cascode transistors is biased at a constant voltage, the drain-gate voltages of cascode transistors could be very large and this may lead to device break down due to hot carrier injection (HCI) effect. In this work, a self-biased cascode amplifier technique is adopted to reduce HCI effect [8]. By using resistors R_0-R_9 and capacitor C_0-C_9, the gate voltages tracks the drain voltages to keep the drain-gate voltages of the cascode transistors not too high [8],[9].

IV. Measurement Results

The proposed transmitter is fabricated in a 65 nm CMOS process. The chip, shown in Fig. 5, occupies an area of 1.6x2 mm^2 including pads where the layout size of the baseband filter is only 0.33x0.51 mm^2. On-chip transformer and inductor are optimized to work in middle LTE bands from 1.8 to 2 GHz. The transmitter chip is packaged in a MLF type in measurements.

Fig. 6 presents the output spectrum of the transmitter at 1.95 GHz carrier frequency with a single tone I/Q digital input of 1 MHz. In this measurement, the amplitude of digital input signal is reduced to avoid output power saturation. The measured output power is +4.5 dBm after de-embedding 1 dB cable loss. The transmitter shows LO feedthrough suppression better than -46 dBc and image rejection ratio -38.4 dBc without calibration. The digital input amplitude is also increased to estimate the saturation point of the transmitter output power. The measured P1dB compression point is 6 dBm at maximum analog and RF gains.

The measured Adjation Channel Leakage Ratio (ACLR) for a 5 MHz LTE signal at 1.95 GHz carrier frequency with 245.76 MHz DAC sampling rate of is shown in Fig. 7. At -0.3 dBm transmitted channel power (1 dB cable loss is de-embedded), the ACLR is below -42 dBc for both upper and lower channels. In wider channel bandwidths, the transmitter

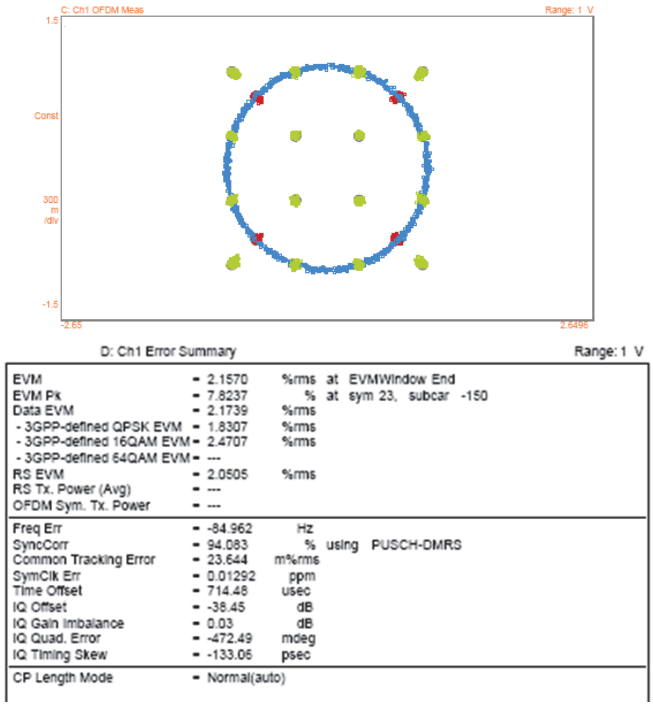

Fig. 8. Measured constellation and EVM for channle bandwidth of 5 MHz.

TABLE 1. PERFORMANCE SUMARY

Parameter	This work	[2]	[7]
Frequency (GHz)	1.8-2	0.7-3.5	1.98
Output power (dBm)	4.5	4.39	6
LO feadthrough (dBc)	-46	-	-54
IRR (dBc)	-38	-	-40
ACLR 5MHz (dBc)	-42 @-0.3 dBm	-40.2 @3.8 dBm	-42 @6dBm
ACLR 20 MHz (dBc)	-43 @-1.9 dBm	-38.4 @1.7 dBm	-
EVM 5MHz Channel	1.83% QPSK 2.49% 16QAM	2%	3%
Noise floor (dBc/Hz)	-154.5	-162.5	-156
Current consumption (mA)/(voltage supply)	59/(1.2 V) 13/(2.5 V)[a]	24/(1.1 V)[b] 40/(2.5 V)[b]	54/(1.5 V) 88/(3.3 V)
Filter topology	2nd-order DT-IIR	2nd-order Active RC	3-tap DT-FIR
Filter 3dB BW (MHz)	0.7 - 10	0.4 – 20	-
Filter size (mm^2) Analog size (mm^2)	0.168 1.08 w/i DAC	0.3[c] 0.98 w/o DAC	0.6[d] 1.3 w/i DAC
Technology	65 nm	40 nm	130 nm

[a] 2.5 V supply used for only DAC [b] DAC not designed
[c] estimated size from layout; [d] estimated size from two auxiliary DRFM paths

shows -41 dBc ACLR at +0.3 dBm output power and -43 dBc ACLR at -1.9 dBm output power for 10 MHz and 20 MHz channel bandwidths, respectively.

Fig. 8 illustrates the measured constellation diagrams with QPSK and 16-QAM modulation schemes with the channel band width of 5 MHz. At -0.3 dBm of channel power, the Error Vector Magnitude (EVM) is 1.83 and 2.47 % for QPSK and 16-QAM modulation signals, respectively.

Since the transmitter operates from 1.8 to 2 GHz covering LTE Band I and II with FDD duplex spacing of 80 and 190 MHz, the Rx-band noise floor is tested at those offset frequencies. With LTE channel bandwidth of 5 MHz, at 1.95 GHz carrier, the measured noise floor is -154.5 dBc/Hz for both 80 and 190 MHz offsets.

In Table I, the measured results are summarized in comparison with other works. Compared to the state-of-the-art design [2], which is implemented without DACs, dissipates 125.4 mW, the proposed transmitter dissipates 70.8 mW from 1.2 V supply for the baseband filters, quadrature modulator, driver amplifier and LO/clock generator. Since the difference between the proposed transmitter and [2] is filter parts, it could be seen that the DT baseband filter occupies a smaller area. To compare our chip size with [7], the core analog areas are used. Analog section in the proposed transmitter including the DACs, baseband filters, quadrature modulator, driver amplifier and LO/clock generator is 20% smaller that of [7] which consists of three parallel DRFM paths. Due to adopting more paths, the power consumption is also significantly increased in [7].

V. CONCLUSION

A low-power small-size transmitter with discrete-time base-band filter is implemented in for LTE application in a 65 nm CMOS process. Instead of using high-order continuous-time lowpass filter, a simple 2nd-order discrete-time filter is adopted after the DAC to suppress out-of-band noise, distortion and spurious emissions with the help of a high over sampling ratio. Although the test chip is designed for LTE band I and II, the proposed transmitter architecture could be applied for multi-band multi-standard applications.

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