A Rectifier for Piezoelectric Energy Harvesting System with Series Synchronized Switch Harvesting Inductor

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***Abstract*—In this paper, a rectifier with series Synchronized Switch Harvesting Inductor (Series SSHI) is proposed for piezoelectric (PE) energy harvesting system. The serial inductor helps to flip the voltage across the internal capacitor of the PE transducer instead of wasting the capacitor voltage by discharge. Active diodes are used for the switches to further improve the extraction efficiency. From measurements, the proposed rectifier shows a power extraction efficiency of 3.3 times that of the active full bridge (FB) rectifier, and more than 90% of the power conversion efficiency.**

Keywords—Vibration energy harvesting, SSHI rectifier, full-bridge rectifier, piezoelectric.

I. INTRODUCTION

Nowadays, the demand of using green energy harvested from ambient environment to supply applications like wireless sensor nodes is rapidly growing. Harvesting vibration energy through piezoelectric transducer is a popular method which can supply up from 10's to 100's of μW available power. An interfacing circuit, a rectifier normally, is needed to efficiently convert the AC current at the output of PE device into a DC signal that can be used for circuits as well as to store in power storage elements. The role of interfacing circuit is very critical because it directly decides the amount of energy that can be extracted from PE devices.

The full-bridge rectifier is widely used piezoelectric energy harvesting system, however, the main limitation is the poor efficiency. Many rectifier circuits have been proposed for the PE energy harvesting systems [1-13]. There are two main approaches of research directions, improving the power conversion and the extraction efficiencies. In the first approach, to reduce the diode forward voltage drop, the passive diodes are replaced by active diode. The active diode is implemented by comparator, or op-amp based active diodes. In the second approach, to reduce the power loss due to the internal capacitor of transducer, several rectifier architectures are proposed. To reduce the discharge process in each half cycle of transducer current, the reset switch tactic is proposed, in which the internal switch is reset when the transducer current crosses zero[1,4,11]. By using this technique, the wasted energy by the discharge process is reduce to zero, therefore the extracted power can be doubled. However, the charging process still wastes power. To reduce the power loss during the charge process, the capacitor voltage flipping technique is proposed [2,4,5] using an off-chip inductor in parallel with the PE transducer. In the bias flipping technique, the inductor is connected in parallel with PE transducer only when the current from the PE crosses zero. Then a resonant loop that includes the inductor and internal capacitor of the PE transducer is formed to flip the voltage across the internal capacitor which eliminates the charging process. In each half cycle of the operation, the inductor should be disconnected immediately after all the energy from inductor is transferred back to the internal capacitor. Therefore, the timing of connecting and disconnecting the inductor is very important; affecting extraction efficiency. To precisely control the inductor ON-time, [4] uses a complex circuit with external tuning and needs external voltage for control of switches. By inserting a passive diode in the resonant loop to prevent the inverse current, [2] simplifies the inductor ON-time control. However, two passives diodes are needed for the two flipping processes of plus to minus and vice versa. In [3] a derivative circuit is needed to detect the zero-crossing point of the current increasing the complexity.

This paper presents a rectifier that adopts a series synchronized switch harvesting inductor where the flipping inductor is connected not parallel but in series with the PE transducer. The serial configuration helps to simplify the control circuit and reduce the number of passive diodes while achieving the same extracted power as the rectifiers reported in [2-4]. Moreover, in the proposed rectifier, all the passive diodes are replaced by active diodes to reduce the voltage drop for further improvement of extraction efficiency.

II. PROPOSED RECTIFIER

Fig.1 (a) shows the proposed series SSHI rectifier with transducer and load. The transducer can be modeled as a sinusoidal current source $i_P(t) = I_P \sin(2\pi f_P t)$ in parallel with an internal capacitor, C_P and resistor, R_P [1,4]. Where I_P varies with the mechanical excitation level of piezoelectric element but is assumed to be relatively constant with any load and f_P is excitation frequency. Different from the conventional

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rectifier, the proposed rectifier includes two diodes D_1 and D_2, two switches SW_1 and SW_2, and one inductor L_F. The replacement of two diodes with two switches permit the current flow in two directions, and the inductor help to flip energy across internal transducer's capacitor.

The operational principle of the series SSHI rectifier is explained by the current and voltage waveforms shown in Fig. 1(b) with the assumption that the diodes are ideal. Starting from t_1, when $V_{CB}<V_{rect}$, switch SW_1 is OFF, switch SW_2 is ON, and both of diodes are OFF because $V_C<V_{rect}$, thus no current flows to the output. The current source keeps charging C_P until t_2 when $V_C = V_{rect}$. From t_2, the diode D_1 is turns ON while diode D_2 is still OFF; current flows to the output then. At t_3 when i_P crosses zero and changes the direction to discharge C_P leading to the V_C reduction; then the diode D_1 is turned OFF. At that time CLK changes from high to low, as a result, SW_2 is OFF and SW_1 is ON. As soon as SW_1 is ON, point A is connected to V_{rect}, otherwise, capacitor voltage still keeps at $V_{CB} \approx V_{rect}$, therefore, $V_C \approx 2V_{rect}$ is larger than V_D. Because of that, the diode D_1 is turned ON again making the resonant loop C-D-A-B. The resonant loop including inductor L_F and capacitor C_P help to flip the voltage across C_P. At first, the energy stored in capacitor C_P transfers to the inductor, after that, this energy is transferred back to capacitor C_P; however, the sign of voltage across capacitor is flipped. Due to the presence of the diode D_1 in the loop, the current flows only from C to D to A. Therefore, the flipping procedure will automatically finish after all energy from inductor L_F is transferred back to C_P without any additional control circuit as in [4]. A similar effect occurs in the negative half cycle of transducer current; then the voltage across the capacitor C_P is change from $-V_{rect}$ to $+V_{rect}$ after the flipping processes.

Actually, due to the parasitic resistances of the switches SW_1, or SW_2, the voltage drop across the diode, and the parasitic resistor of the inductor, the voltage across C_P is flipped to $\pm V_f$ (with $V_f<V_{rect}$) instead. Then in every half cycle, some amount of power loss occurs during charging of C_P from $\pm V_f$ to $\pm V_{rect}$ ($\Delta V_1 = V_{rect} - V_f$) while similar power loss occurs during charging (discharging) process of C_P from $\mp V_{rect}$ to $\pm V_{rect}$ ($\Delta V_2 = 2V_{rect} >> \Delta V_2$) in the conventional rectifier [4]. Thus, the flipping process using resonant loop significantly reduces power loss leading to much higher extracted power from the transducer. Since the smaller the value of $\Delta V_1 = V_{rect} - V_f$, the lower the power loss, and the higher the power extraction efficiency, therefore, the power extraction efficiency of the rectifier is inversely proportional to the flipping ratio given by

$$\eta_F = \frac{V_f + V_{rect}}{2 \cdot V_{rect}} \tag{1}$$

By the similar calculations reported in [3], the maximum output power of the proposed rectifier is given by

$$P(\max) = \frac{I_p^2}{4\pi^2 C_P f_P (1-\eta_F)} \tag{2}$$

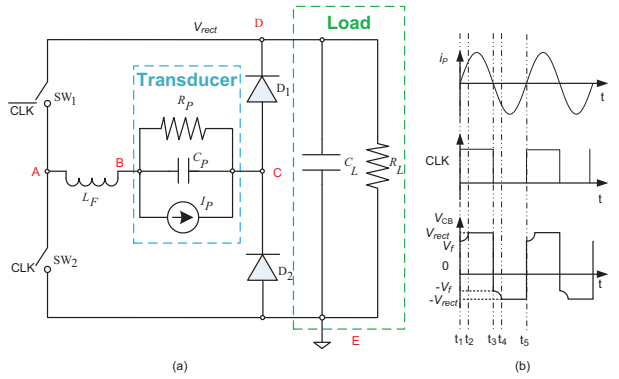

Fig. 1: (a) The proposed series SSHI rectifier circuit. (b) Current and voltage waveforms

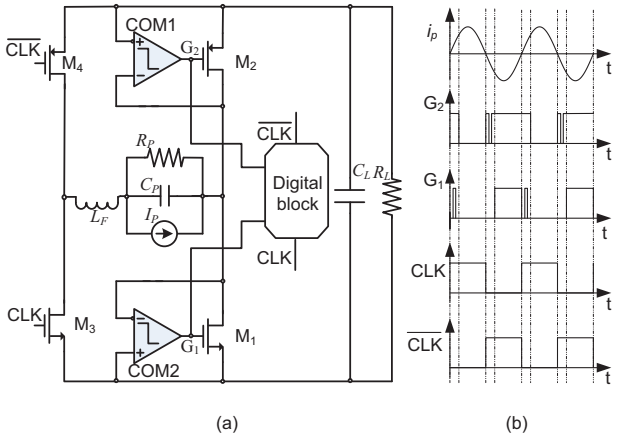

Fig. 2 The proposed rectifier with serial synchronized switch harvesting inductor

when $V_{rect} = \frac{I_P}{4\pi C_P f_P (1-\eta_F)}$. (2) can be used to calculate the maximum extracted power of all of full bridge rectifiers and other variants of full bridge rectifiers. In the active full bridge rectifier, there is no flipping effect, $\eta_F = 0$; then the maximum power extraction is $\frac{I_p^2}{4\pi^2 C_P f_P}$ when $V_{rect} = \frac{I_P}{4\pi C_P f_P}$. In the switch only rectifier reported in [4,11], $\eta_F = 0.5$; then the maximum extracted power is $\frac{I_p^2}{2\pi^2 C_P f_P}$ when $V_{rect} = \frac{I_P}{2\pi C_P f_P}$. These results agree with the calculations reported in [1,4,5]. Similarly with [2-4], an off-chip inductor is added in the proposed rectifier to further increase the flipping ratio (>0.5). Simulations show that the proposed series SSHI rectifier can provide the flipping ratio of 0.7 that is same value as that of the parallel SSHI rectifier reported in [4] (estimated by authors). From (2), with $\eta_F = 0.7$, the proposed rectifier can achieve an extracted power 3.3 times higher than that of the active FB rectifier.

Circuit implementation – Fig. 2(a) shows the rectifier circuit detail, in which the passive diodes are replaced by active diodes. Diode D_1 is replaced with ground compatible

TABLE I: PERFORMANCE COMPARISONS WITH PREVIOUSLY REPORTED RECTIFIER FOR PE SYSTEM

Publication	JSSC 06 [13]	TPE 12 [11]	TPE 10[2]	JSSC 10 [5]	This work
Technique	0.35 µm CMOS	0.18 µm CMOS	Discrete	0.35 µm CMOS	0.18 µm CMOS
$V_{In,peak}$ (V)	0.6	3	20	2.4	2.23
V_{rect} (V)	0.5	2.78	3.75	3.2	3.6
f_C (Hz)	280-430	200	185	225	200
Architecture	Active FB	Resetting	Flipping Capacitor	Flipping Capacitor	Flipping Capacitor
Flipping Efficiency	0	0.5	~0.65	~0.7	0.7
Inductor(uH)	NO	NO	1000	820	390
External Supply	NO	YES	YES	YES	NO
P out(uW)	23	81	1230	68	74
Area (mm^2)	0.16x0.10	0.25x0.65	NA	4.25	0.08x0.2
Compare with Active FB	0.85X	1.9X	2.3X	3.3X(4X*)	3.3X

(*) Theoretical in Eq.(2) predicts 3.3X but the authors claimed 4X.

comparator COM_1 and a transistor M_1; the other diode is replaced supply compatible comparator COM_2 and transistor M_2. As mention before, in each cycle of the rectifier operation, each diode is turned on in two times: when current from transducer flows to load, and when the resonant loop is created. Therefore, the waveform of comparator's output, G_1 and G_2, are as the way shown in Fig. 2(b). In Fig. 2(b) the G_1 and G_2 signals are the inputs of digital block that detects the zero-crossing point of the transducer current and generates CLK and $\overline{CLK}$ signal as shown in Fig.2 (b). The CLK and $\overline{CLK}$ signal returns to control the transistor M_3 and M_4 which works as switches.

Fig.4 shows the common gate amplifiers that work as comparators: (a) ground compatible comparator and (b) supply compatible comparator. Since the comparators should be supplied by the harvested energy and the output power of the transducer is in range of 100 µW, the power consumption of the comparators should be minimized. In this work, transistors in the comparator are designed to operate in sub-threshold region. Total current consumption of the each comparator is 90nA. Moreover, the supply independent current bias circuit with supply ram-up is used to make the current consumption of comparator independent of the supply voltage variation.

III. SIMULATION AND MEASUREMENT RESULTS

The simulation and measurement are carried out for the proposed rectifier shown in Fig.3 with transducer model values of I_P= 70µA, f_P=200Hz, C_P=25nF and R_P=1MΩ, and the inductor value of 390µH is used and load is varied from 50KΩ to 200KΩ with a 5KΩ step. From the simulation the maximum extracted power of proposed rectifier occurs at 160KΩ resistor at the load. Fig. 4 shows the comparison between the active FB rectifier and proposed rectifier on V_{CB} and V_{rect} with the same load of 160KΩ. The simulation shows that, the flipping efficiency of conventional rectifier is 0 while, the proposed rectifier $\eta_F = 0.7$. Theoretically, by using (2),

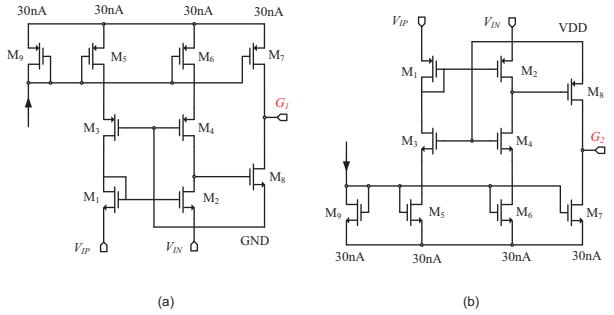

Fig. 3 Circuit schematics of (a) Ground comparator ;(b) VDD comparator

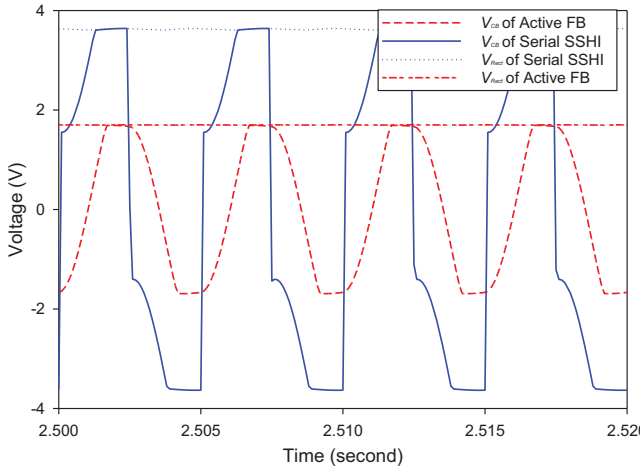

Fig. 4. Simulated waveform of active FB rectifier and proposed rectifier in V_{CB} and V_{rect}

with $\eta_F = 0.7$, the maximum extraction power is 82.7µW at V_{rect}=3.71V, however, because of power consumption of the system, simulation results shows that the maximum extracted power of proposed rectifier is 75µW with V_{rect}=3.63V. Under the same conditional, the active full bridge rectifier extract 18.1 µW when V_{rect}=1.7V

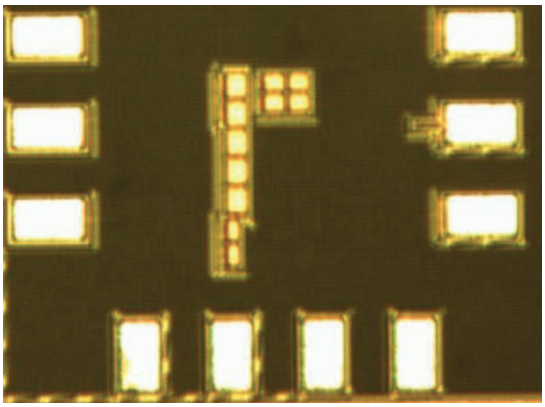

Fig. 5 The micrograph of the proposed rectifier

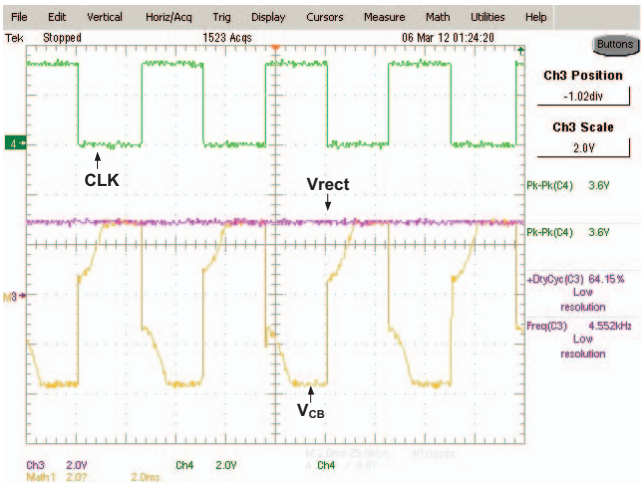

Fig.6. Measurement wave form of output voltage across the piezoelectric harvesting V_{CB}, control signal CLK and output voltage (V_{rect})

The proposed rectifier is fabricated in 0.18um CMOS technology, which occupies an active area of 0.08x0.2mm^2 as shown in Fig. 5. Fig. 6 shows the measured V_{CB} , V_{rect} and CLK signal of the proposed rectifier at the maximum extraction power case with R_L equals 175KΩ. Owing to the polarity flipping of the internal capacitor when current source cross zero, V_{CB} changes from -3.6V to 3.6V when CLK change its level. Because of the very small voltage drop across the two active diodes, ($|V_{dsp}|+V_{dsn}$), the output voltage of the proposed rectifier is almost 3.6V. The measured maximum extracted power of proposed rectifier is 74uW. Table I compares the performance of the proposed design to recent, state-of-the-art rectifiers for PE energy harvesting applications. In table I, by using capacitor polarity flipping, the extracted power of rectifiers increase significantly in comparison with active full bridge and capacitor resetting architecture based rectifiers. In comparison with the same capacitor polarity flipping architecture (parallel SSHI) that introduced in [4], the proposed rectifier requires the smaller inductor and chip sizes yet achieves the same performance because the proposed rectifier don't need two DC-DC converts for detecting current zero-crossing points and control switches The two DC-DC converters in [4] led to big chip size in comparisons with proposed rectifier. Compared to the state-of-the art designs for PE energy harvesting, the proposed rectifier not only shows a higher extraction efficiency, but smaller size as well.

IV. Conclusion

This paper has identified problems that exist with the rectifiers that are used in piezoelectric energy harvesting systems. The proposed rectifier overcomes the drawback of previous rectifiers. By using series SSHI, the voltage across the internal capacitor of PE transducer is flipped to extract more power; simultaneously, diodes are replaced by active diodes to reduce the voltage drop. Furthermore, a new effective control scheme is proposed to control switches. The measurement result show that the extracted power of proposed rectifier 74μW with flipping efficiency 0.7 and shown that more than 90% of the power conversion efficiency can be achieved.

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