A Zero Current Detector with Low Negative Inductor Current Using Forced Freewheel Switch Operation in Synchronous DC-DC Converter

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***Abstract*— In DC-DC converter at light load, discontinuous conduction mode (DCM) and pulse frequency modulation (PFM) mode are usually used to improve efficiency instead of using low efficient continuous conduction mode (CCM) in a pulse-width modulation (PWM) control system. For these control modes in light load condition, the zero-current detector (ZCD) to prevent reverse current flowing back to the power source is essential. This paper presents a zero current detection method with enhanced time response of the freewheel switch operation. The proposed ZCD was simulated using a 0.18-µm CMOS process in a test system of PWM voltage mode type-III buck converter, with input voltage of 3.3V. The test system works in CCM at heavy load, PFM at light load, and DCM in a short transient of decision to change from CCM to PFM. The PWM switching frequency is 2MHz, and testing output voltage is 1.8V with load current from 20mA up to 300mA. Under the same test condition, the proposed ZCD shows maximum improvement of 6.9% efficiency in PFM compared to the conventional method, making the overall efficiency greater than 89.7%.**

Keywords*— *DC-DC converter; buck converter; zero-current detection; discontinuous conduction mode (DCM); pulse frequency modulation (PFM); freewheel switching; SOC

I. INTRODUCTION

In DC-DC converter, an inductive-switched converter with PWM control is usually used for high conversion efficiency. PWM can be operated in two modes: (1) continuous conduction mode for heavy load; and (2) discontinuous conduction mode for light load. However, PWM shows a low conversion efficiency at light load. Therefore, another control method, usually pulse-skipping mode (PSM), or pulse frequency modulation (PFM) is used instead [6], to increase conversion efficiency at light load. Regardless of all light load control methods, a zero current detector is necessary to impede negative inductor current flowing back to the source in order to reduce the root mean square (RMS) current, and hence, reducing conduction loss and improve conversion efficiency at light load.

Conventionally, the zero current crossing point can be simply detected by tracing the zero crossing point of the LX node, which is the crossing point of the inductor and the high side and low side switches. This detection method is based on the fact that, at the falling edge of the inductor current, LX node has a negative potential voltage. The reason is that: At this time, the current flows through low side switch from the power ground node to LX through the inductor, which implies that the potential voltage of LX node is lower than the ground voltage, i.e. LX node voltage is negative. When the inductor current decreases from this point, voltage potential at LX node also increases from negative voltage. Hence, when the inductor current crosses zero, LX node's potential is also ground. Therefore, by comparing LX voltage node with ground, zero inductor current crossing point can be detected [2][7][8]. In addition, at light load current condition, the change in LX voltage potential during conduction period of the low side switch is also very small:

$$-LX = R_{ON} * I_L \quad (1)$$

in which R_{ON} is the ON resistance of the low side switch, and I_L is the inductor current.

This small voltage potential change of LX node usually cannot overcome offset voltage of comparator; hence, usually a preamplifier stage is required before the comparator stage to overcome this difficulty [2].

Up to now, the studies of ZCD circuit only focus on the comparator speed and the correctness of the detection time of the zero inductor current crossing point [2][7][8]. Based on this assumption of incorrect ZCD detection time, a PID control circuit is also studied to reduce absolute negative inductor current as in [8]; however, an absolute negative inductor current of about 8mA still presents, according to the simulation result in the study. The reason for the non-negligible negative inductor current (even when using PID control) is not only just the PID error, but also another important cause as well: For the correctness of freewheel switch function during the present of negative inductor current, the voltage potential of LX node should be larger or equal to that of the output voltage. However, before the negative inductor current is detected, LX voltage potential is below ground. In addition, the LX node attaches to the two large parasitic capacitors of the two power switches, while inductor current at during this time is very small (near zero). Therefore, charging time for LX node by inductor current will be very slow. During this charging time, the freewheel switch is unable to perform its designed function.

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In this paper, a proposed ZCD circuit is implemented using the conventional zero current crossing detection method based on LX crossing ground voltage detection, with a proposed forced operation for freewheel switch to re-direct negative inductor current back to the load. In addition, a positive rising edge SR flip-flop is also proposed and used in the proposed ZCD circuit to avoid false zero current detection due to noise and possible oscillation of LX voltage node.

II. Overall Voltage Mode Type III Buck Converter

The overall architecture of the test system can be seen in Fig. 1. The basic buck converter system is designed with PWM control using voltage mode [3] compensation type III [4]. According to the current load condition, the circuit can operate mainly in two modes: CCM at heavy load, or PFM at light load.

In order to reduce output voltage drop when load current changes from low to high, usually the output voltage level of PFM is designed to be a little higher than the designed one of PWM. When the load condition is in between heavy load and light load, there is a potential of continuous changing mode between PWM and PFM. This effect causes more ripples to the output voltage due to voltage droop effect when load condition changes. To reduce the number of mode-switching events, a counter is implemented to make decision of changing mode: The counter counts the number of detected zero-current events to make decision of changing mode.

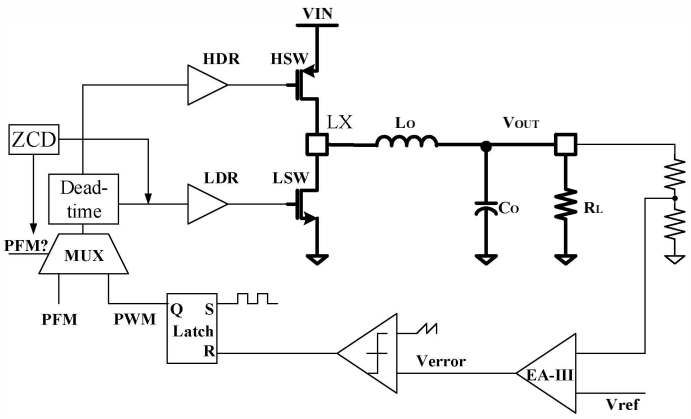


Fig. 1. Overall Voltage Mode Type III Buck Converter Architecture.

III. Zero Current Detector Operation

Shown in Fig. 2 is the architecture of the conventional ZCD, which is based on the detection of zero voltage potential of LX node as described in part I. Because the inductor current is a continuous function, after ZCD event, even when the two power switches are turned off, absolute negative inductor current still presents and will be diminished via the parasitic capacitor paths of the power switches. In order to reduce the absolute negative current flowing back to the power source, which indicates a power loss, and to suppress EMI due to LX oscillation, a freewheel switch is usually used as in Fig. 3 [2][5][7][8]. The operation of this freewheel switch also can be seen in Fig. 3: After zero inductor current is detected, both two power switches will be turned off, and the freewheel switch is turned on, providing a current path for the negative inductor

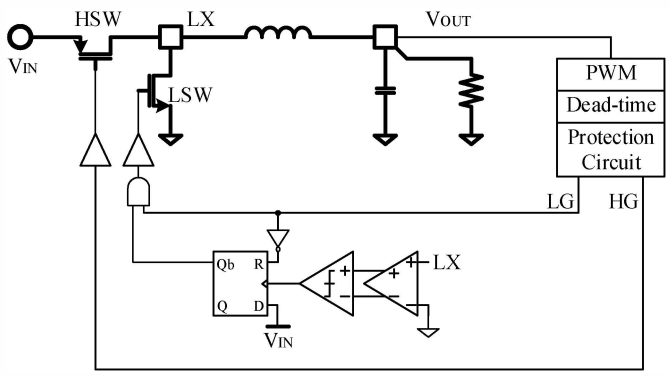
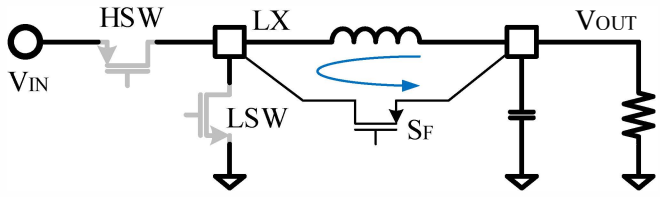


Fig. 2. Conventional ZCD circuit.



NOTE: Normal inductor current direction from LX to V_{OUT} is indicated as positive direction; hence, a reverse inductor current direction will be indicated as negative current.

Fig. 3. Effect of using freewheel switch to re-direct negative inductor current back to load side.

current to flow back to V_{OUT}. By doing so, the negative inductor current can be reduced; thus, lowering the power loss.

The proposed ZCD circuit will also employ these two important ZCD circuit parts in its design.

A. Proposed ZCD Circuit

Shown in Fig. 4 is the overall architecture of the proposed ZCD circuit. The main detection circuit is based on the conventional ZCD, in which zero inductor current crossing point is detected by comparing LX voltage node to ground. In order to avoid false ZCD detection due to noise at node LX, a proposed positive rising edge SR flip-flop is added to mask the zero current detection noise. Detailed of the proposed structure for the positive rising edge SR flip-flop will be discussed in section *B*. Detailed of the ZCD comparator and its preamplifier are also shown in section *C*.

In order to enhance the time-response of the freewheel switch to operate correctly, i.e. to conduct and re-direct negative inductor current back to the load side, a proposed pre-charged switch S_{PC} will be used to pre-charge for node LX to rise faster after the zero inductor current event is detected. The gate control for this switch S_{PC} is also shown in Fig. 4.

Shown in Fig. 5 is the waveform of the ZCD control signals generated from the proposed circuit in Fig. 4. According to the ZCD control scheme, a noisy ZCD detection signal will be masked until the beginning of the next switching period, using a proposed positive rising edge SR flip-flop. The high side switch conduction period is decided by the PFM duty detection. Then the low side switch conducts until the ZCD signal is triggered. Pre-charged switch S_{PC} will work for a short time period to pre-charge LX voltage node to increase from ground voltage potential to V_{OUT} level; then, free-wheel

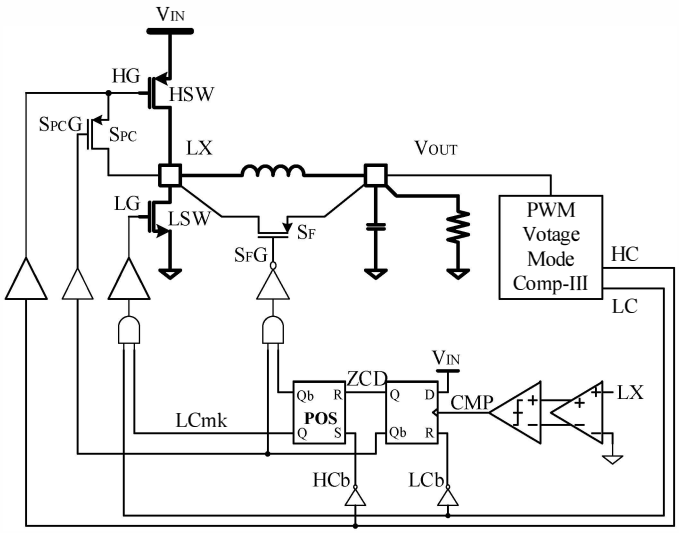


Fig. 4. Proposed ZCD circuit tested in PWM voltage mode buck converter with on-chip compensation type III.

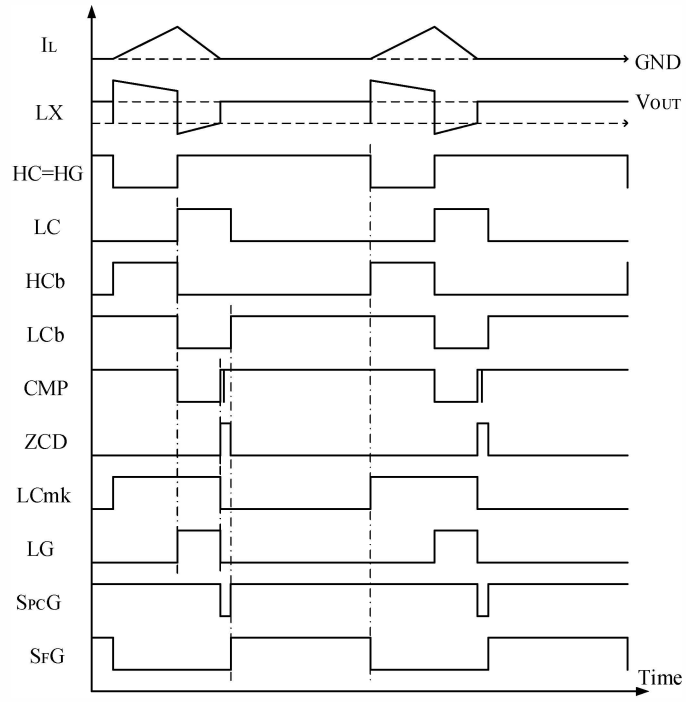


Fig. 5. Waveform of the ZCD control signals at light load in two DCM/PFM periods.

switch S_F will conduct to re-direct negative inductor current flowing to the supply power side back to the load side. Hence, the absolute negative inductor current can be diminished.

B. Proposed SR Flip-Flop Used in the Proposed ZCD and SR Latch for the PWM and PFM Control

The proposed positive rising edge SRFF for the proposed ZCD circuit and a simple structure of SR latch for PWM and

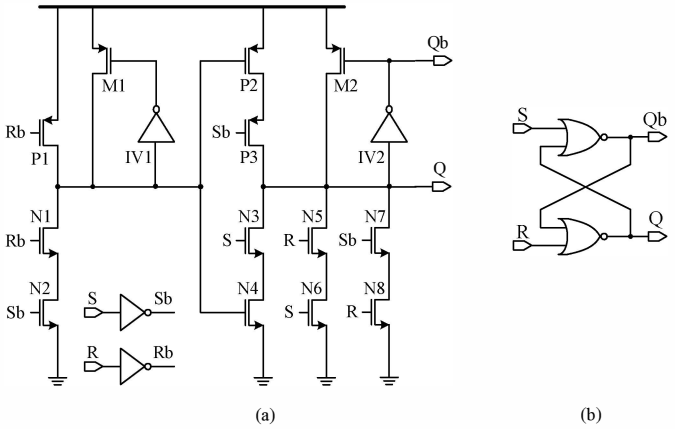


Fig. 6. (a) Proposed Positive Rising Edge SR flip-flop used in ZCD circuit, and (b) Conventional SR latch used in PWM control.

TABLE I. TRANSISTOR PARAMETERS OF THE PROPOSED POSITIVE RISING EDGE SR FLIP-FLOP

	P1	P2, P3	M1, M2	N1~N8	IV1, IV2 PMOS	IV1, IV2 NMOS
W/L	1.2/0.5	2.4/0.5	0.6/1.0	1.2/0.6	1.2/0.5	0.6/0.6

NOTE: The unit is μm.

TABLE II. TIMING CHARACTERISTICS OF THE PROPOSED RISING EDGE SR FLIP-FLOP AND THE CONVENTIONAL SR LATCH

Type	**Timing Chracteristic**		
	SR	***Q***	***State Description***
Positive Rising Edge SRFF	00	Q_{prev}	Hold
	0↑	0	Reset
	↑0	1	Set
	↑↑	-	Not allowed
Conventional SR Latch	00	Q_{prev}	Hold
	01	0	Reset
	10	1	Set
	11	-	Not allowed

NOTE: 0 indicates digital ground voltage level; 1 indicates digital high voltage level; ↑ indicates a rising signal from digital ground to digital high voltage level.

PFM detection are shown in Fig. 6 (a) and (b). Because the period of PFM can be long in order to save energy, positive feedback loops M1-IV1 and M2-IV2 [9] are necessary to compensate for the discharged charge loss at latch phase of the positive rising edge flip-flop. The reference transistor size is given in TABLE I. To diminish transistor mismatch during manufacturing, an SR flip-flop with a larger scaling size according to this table is still able to work, with expected slower speed due to larger parasitic capacitors. The timing characteristics of the proposed positive rising edge SRFF and SR latch are given as in TABLE II.

C. ZCD Comparator with Pre-Amplifier:

Fig. 7 shows the schematic of the ZCD comparator with a simple preamplifier structure. Fig. 7 (a) is the bias voltage circuit used for the ZCD comparator and the pre-amplifier. The bias circuit uses the wide-swing constant transconductance bias circuit structure [1] for the converter to be able to work in a wide range of input voltage supply. This bias circuit is also used for bias voltage supply for the other circuit block of the converter such as the error amplifier, and other comparators. Fig. 7 (b) shows a simple preamplifier which is usually used in

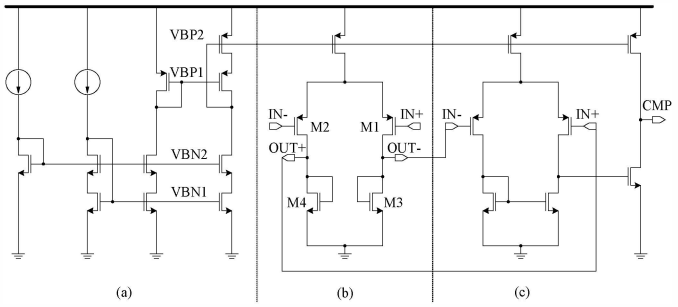


Fig. 7. ZCD comparator with pre-amplifier: (a) Wide-swing bias circuit; (b) pre-amplifier; (c) comparator.

high-speed ADC/DAC comparator. The gain of this preamplifier is:

$$A_V = \frac{g_{m1}}{g_{m3}} \tag{2}$$

Finally, Fig. 7 (c) shows the main structure of the comparator. For manufacturing consideration, one may consider to implement offset voltage cancellation to reduce offset variation of the comparator comes from transistor mismatch.

IV. Simulation Results

The proposed ZCD circuit is simulated for a PWM voltage mode buck circuit, with input voltage from 2.2V to 5.5V, to get output voltage from 1V up to 90% of input voltage, using a 0.18µm CMOS process. The PWM switching frequency is 2MHz, using converter switches with ON resistance R_{ON} of 300mΩ, inductor filter with inductance value of 1.1µH and capacitor filter with capacitive value of 10µF and equivalent series resistance of 20mΩ, for load current below 300mA. For design under higher load current condition, reducing ON resistance of the switches, decreasing switching frequency and increasing filter inductance are necessary to get the conversion efficiency of higher than 90% (typical acceptable conversion efficiency of DC-DC converter). For the comparison purpose between the proposed ZCD's performance and the conventional ZCD's performance, forced DCM operation at 2MHz switching frequency is simulated to get the simulation results as shown in Fig. 8 and Fig. 9. In addition, the normal operation of the converter using both PFM and PWM is also simulated to obtain the simulation results in Fig. 10 and Fig. 11, with input voltage of 3.3V and output voltage of 1.8V.

Fig. 8 and Fig. 9 show comparisons between the proposed ZCD and the conventional ZCD under the same test condition: The conventional ZCD is implemented using the same detection circuit including comparator type, flip-flops and latches type, and buffer type, except the part related to the pre-charging switch S_{PC} compared to the proposed ZCD. The solid line and the dot line shown in Fig. 8 are the LX voltage waveform using the proposed ZCD and the normal ZCD, respectively. At the zero current crossing point detected, using the proposed ZCD with the pre-charged switch S_{PC}, rising time of LX node is faster compared to that from the normal ZCD without the pre-charge switch S_{PC}. Shown in Fig. 9 are: (1) the inductor current in dot red waveform; (2) the summation of the inductor current and freewheel switch current for the proposed ZCD in solid blue line; and (3) the one for the conventional ZCD in dashed green line. With the help of the pre-charge switch S_{PC} as in the proposed ZCD, the LX voltage node rises faster. Therefore, the freewheel switch can operate faster, and the corresponding total current of inductor current and freewheel switch current from the proposed ZCD is much smaller: The maximum absolute negative inductor current reduces from 18mA to 8mA. Furthermore, peaking inductor current at the ZCD detected can be brought down by reducing size of the pre-charged switch S_{PC}, with the price of increasing the maximum absolute negative inductor.

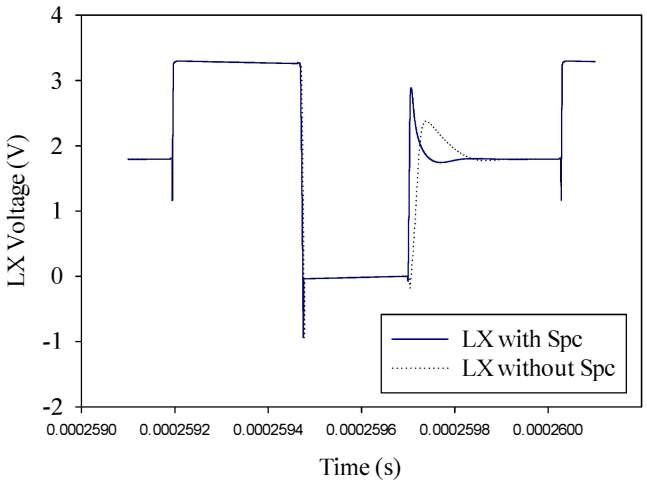


Fig. 8. Simulated DCM LX voltage node in a period for the PWM switching frequency of 2MHz.

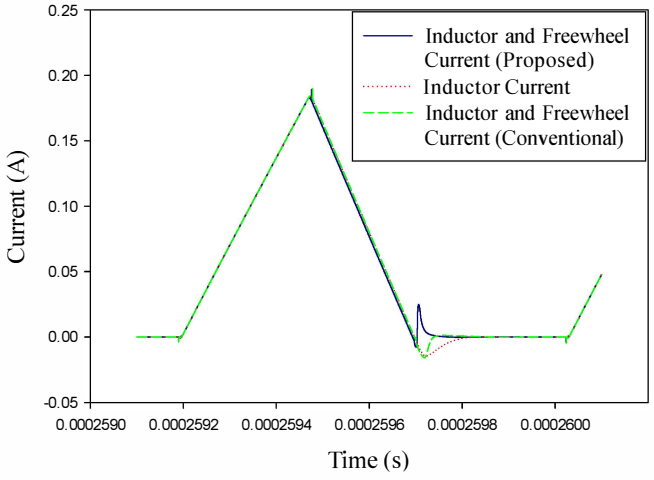


Fig. 9. Simulated DCM inductor current curve in a period for the PWM switching frequency of 2MHz.

Shown in Fig. 10 is the simulation result of maximum absolute negative inductor current under different load conditions from 20mA to 120mA, when the system works in PFM mode, using the proposed ZCD. The simulation shows

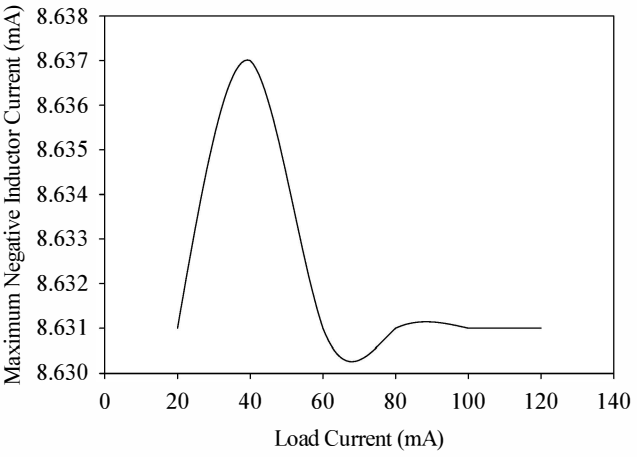


Fig. 10. Simulated maximum absolute of negative inductor current by the proposed ZCD when load current varying.

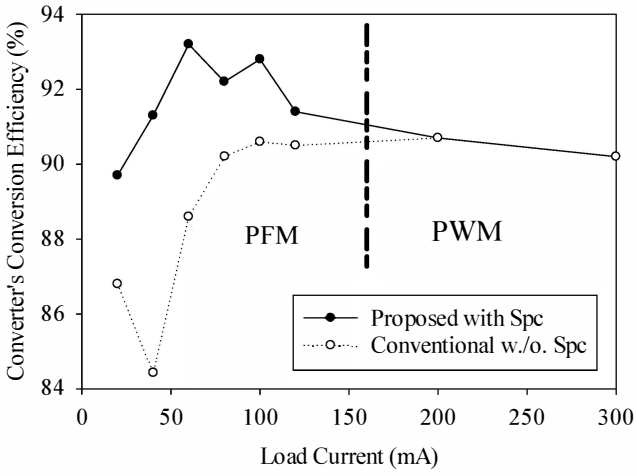


Fig. 11. Simulated efficiency of the converter using the proposed ZCD: PFM is detected under load condition below 120mA; PWM with switching frequency of 2MHz is detected under load condition above 200mA.

that the maximum absolute negative inductor current value is quite stable when the load current varies.

Finally, shown in Fig. 11 is the simulated conversion efficiency of the proposed ZCD compared to that of the conventional ZCD: The simulation result indicates an overall improvement of efficiency in PFM, and almost the same efficiency in CCM. Maximum efficiency improvement is 6.9% at 40mA load current. There is an abnormal high efficiency point from the conventional ZCD due to low PFM switching frequency required for very light load of 20mA. Contradictorily, not much efficiency improvement coming from the proposed ZCD compared to the conventional one at this current load point is due to additional power consumption for the additional components (the pre-charged switch S_{PC} and the pre-charged switch's driver). For this reason, there is no benefit of obtaining lower than 8mA of maximum absolute negative inductor current because the efficiency will be worse.

V. Conclusions

A zero current detector with forced freewheel switching operation by pre-charging LX node was proposed and simulated for a voltage mode compensation type III buck converter, using a 0.18μm CMOS process. According to the simulation result, the proposed ZCD scheme does not affect the stability of the PWM compensation at heavy load in CCM, and shows an absolute overall power conversion efficiency improvement in PFM, with a maximum efficiency improvement of 6.9% at 40mA. The overall efficiency is higher than 90% for load current from 40mA to 300mA, and 89.7% for load current of 20mA. The buck converter uses PWM switching frequency of 2MHz, with 1.1μH filter inductor, 10μF filter capacitor, and two power switches each with ON resistance of 300mΩ. For design with heavier load current (above 300mA), lower switching frequency with higher filter inductor's value, and lower ON resistance of the power switches should be considered to get higher efficiency.

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