13.1 A 227pJ/b -83dBm 2.4GHz Multi-Channel OOK Receiver Adopting Receiver-Based FLL

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With growing interest in the internet-of-things (IoT), there has been increasing demand for wireless transmission of information captured by various sensors with minimum power dissipation, which is difficult to achieve with existing solutions such as Zigbee and Bluetooth-LE. Accordingly, there has been a high demand for an ultra-low power (ULP) transceiver that reduces the power by more than an order of magnitude relative to that of existing solutions. Most of the previously reported ULP receivers (RXs) are developed as single-channel devices focusing on low power consumption while adopting a high-Q MEMS device [1] or a crystal oscillator (XO) [2]. However, for proper utilization of the IoT, e.g., accommodating multiple sensors at the same time and place, multichannel operation is essential. There have been reports of super-regenerative [3,4] and injection-locking-based FSK [5] RXs as multichannel radios with a limited signal-to-interferer ratio (SIR), making them susceptible to the adjacent channel interferers. In [6], a 2-tone modulation scheme that sacrifices the spectral efficiency and data-rate is adopted for in-band interference tolerance. For multichannel operation with an adequate SIR, downconversion is an optimum solution. However, the power burden of PLL-based LO generation impedes its adoption for ULP RX. This work focuses on reducing the power of LO generation blocks in the ULP OOK RX. Considering the relaxed frequency stability requirement of OOK modulation, a receiver-based FLL (RBFLL) that adopts the RX chain as a part of the FLL as a substitute to the power-hungry divider is proposed. Implemented in 65nm CMOS, a 2.4GHz multichannel ULP OOK RX with the RBFLL achieves -83dBm sensitivity at 1Mb/s while dissipating 227μW from a 0.6V supply.

Figure 13.1.1 shows a block diagram of a conventional PLL where the divider scales down the frequency and phase of the VCO for comparison with those of an XO. In the receiver-based PLL (RBPLL) shown in Fig. 13.1.1, the divider is replaced with a mixer, IF-amp, and Schmitt trigger (ST). In the RBPLL, for the downconversion of, for example, a 2.398GHz continuous-wave (CW) signal to an IF frequency of 2MHz, the automatic-frequency-control (AFC) [4] block initially sets the binary-weighted capacitor bank to oscillate the VCO near 2.4GHz. The limited resolution of the capacitor bank and AFC leads to a VCO frequency offset of Δf, which is downconverted into an IF frequency of 2MHz + Δf. This IF signal, amplified by the IF-amp, drives the ST, which converts the sinusoidal wave into a digital signal. The phase-frequency detector (PFD) with a charge pump (CP) and a lowpass filter (LPF) generates an error signal by comparing the digitized IF signal with the 2MHz clock that comes from the XO. The error signal then corrects the phase and frequency of the VCO. In this work, the RF input of the ULP RX is OOK not CW. Therefore, the ST output is in the form of a return-to-zero (RZ) signal. As shown in Fig. 13.1.1, to process the RZ signal, the PFD is replaced with a rotational frequency detector (RFD), making it FLL instead of PLL. Since the information is contained in the amplitude, not the phase or frequency in OOK modulation, the FLL is sufficient for the ULP OOK RX. In the RBFLL, since the variations of the VCO frequency directly appear at the output of the ST, the gain from the VCO output to the ST output in the frequency domain is equal to 1. Therefore, the 2.4GHz VCO with an RX path that includes the OOK signal, mixer, IF-amp, and ST can be modeled as a 2MHz VCO. From the s-domain model of the RBFLL shown in Fig. 13.1.1, the transfer function of the RBFLL is given by eq. (1), where K_{VCO} is the VCO gain, K_{RFD} the RFD gain, and I_{CP} the current of the CP. Eq. (1) shows unconditionally stable FLL operation with one pole and ideally zero steady-state error for a step frequency change. Therefore, by re-using the RX chain of the radio, a ULP FLL can be implemented.

This concept of the RBFLL is applied to a 2.4GHz multichannel ULP OOK RX and the overall block diagram is shown in Fig. 13.1.2. The RX in Fig. 13.1.2 adopts a low-IF architecture for channel selection with relaxed filter performance and to obtain sufficient gain with low power at low frequency. Moreover, instead of adopting a power-hungry Q-VCO or 2x VCO with a frequency divider, the I/Q generation is implemented in the RF path [7]. The mixer downconverts RF I/Q signals to IF and a hybrid complex filter performs channel selection and image rejection. IF amplifiers provide enough gain to overcome the noise of the following envelope detector (ED), which demodulates the OOK signal. The OOK demodulator and symbol timing-recovery circuits convert the ED output into final digital bit streams. In Fig. 13.1.2, for the incoming OOK signal, the initial tuning for the VCO frequency is done by the AFC. The AFC then turns off to reduce power consumption. The frequency error (Δf) is subsequently compensated by the RBFLL.

Figure 13.1.3 shows the schematic of the LNA, which has been implemented as a single-ended topology to reduce power and remove the off-chip balun. In the LNA, M_1 and M_2 form a self-biased inverter-type amplifier. The center-tapped inductor T_1 works as a 1:1 transformer for g_m-boosting, doubling the g_m of M_1 and M_2 and reducing the NF. As a result, the LNA achieves 4 times larger g_m than that of a simple common-source type amplifier. Furthermore, to achieve maximum voltage gain, an off-chip inductor is adopted at the output to resonate the parasitic capacitance while presenting high impedance. M_{BIAS} is adopted for gain control. The LNA achieves 27dB voltage gain at 2.4GHz while dissipating 55μW.

The LC-VCO shown in Fig. 13.1.3 adopts two external inductors to reduce the power consumption and improve the frequency stability of the VCO, instead of adopting an FBAR, as in other low power VCOs [8]. The K_{VCO} of the VCO is minimized (≈2MHz/V) to further stabilize the oscillating frequency. The LC-VCO is designed to cover the frequency range of 2.36 to 2.5GHz by adopting a 10b MIM capacitor bank for coarse and fine binary-weighted tuning and a minimum size varactor is used for continuous tuning by the RBFLL. The VCO exhibits phase noise of 132.85dBc/Hz at a 1MHz offset while dissipating 78μW.

The ULP RX shown in Fig. 13.1.2 was implemented in 65nm CMOS consuming 227μW (227pJ/b) from a 0.6V supply. The power breakdown is shown in Fig. 13.1.4. The measured time-domain waveforms of 1Mb/s PRBS input data, the ED output, and demodulated output, respectively, are shown in Fig. 13.1.4. The measured sensitivity is -83dBm for a 1Mb/s, 2.4GHz OOK signal (Fig. 13.1.4). For the SIR measurement, a desired signal with 3dB higher power than the sensitivity level and a CW or OOK interferer signal is applied at the RX input. As shown in Fig. 13.1.4, at 10MHz offset, the RX tolerates 30.5dB and 22.5dB higher levels of CW and OOK interferers, respectively. The measured VCO spectra with AFC and RBFLL on/off are shown in Fig. 13.1.5. The RBFLL reduces the frequency error of the AFC from 1.067MHz to 100kHz. Residual frequency error is caused by the RX noise and other non-idealities. Figure 13.1.6 shows a performance summary of this work in comparison with state-of-the-art ULP RXs. As a multichannel ULP RX, the proposed RX shows performance comparable to that of single-channel ULP RXs with superior SIR performance relative to that of multichannel RXs. Figure 13.1.7 shows a die micrograph of the proposed ULP RX with a size of 1.17 mm^2.

Acknowledgements:
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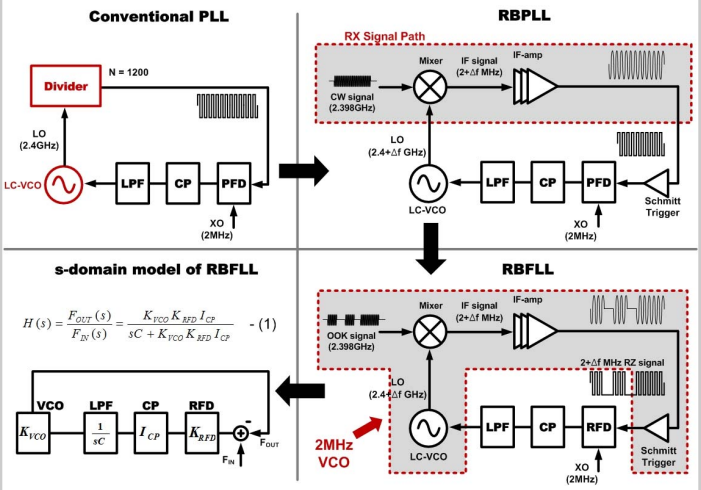

Figure 13.1.1: Block diagram for PLL, RBPLL, RBFLL, and the s-domain equivalent model of RBFLL.

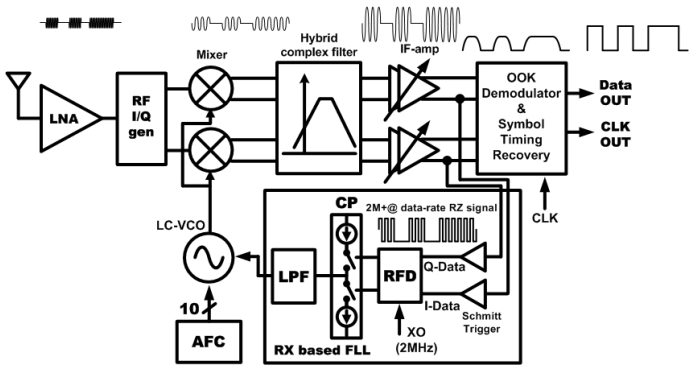

Figure 13.1.2: Overall block diagram of a 2.4GHz multi-channel ULP RX with proposed RBFLL.

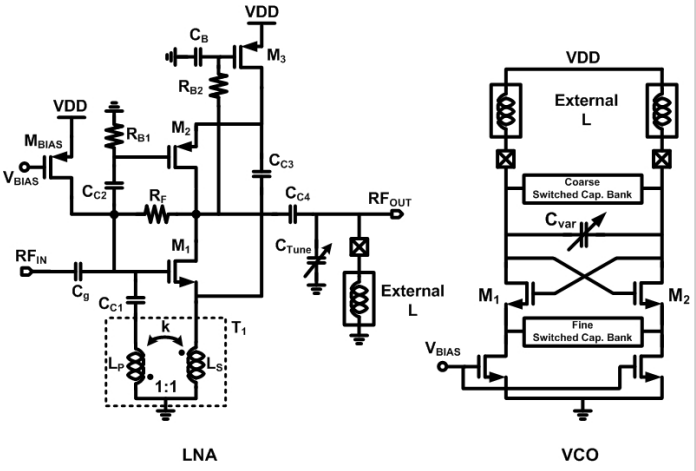

Figure 13.1.3: Schematic diagrams of LNA and VCO.

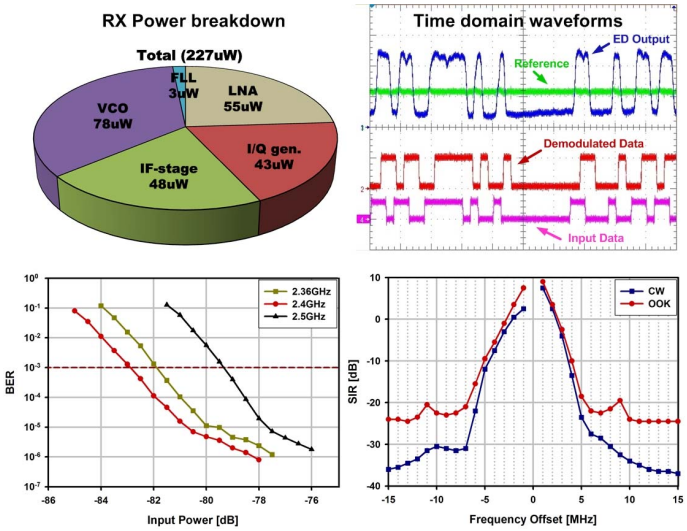

Figure 13.1.4: Power break-down and measurement results of time-domain waveforms, BER, and SIR to CW & OOK interferers.

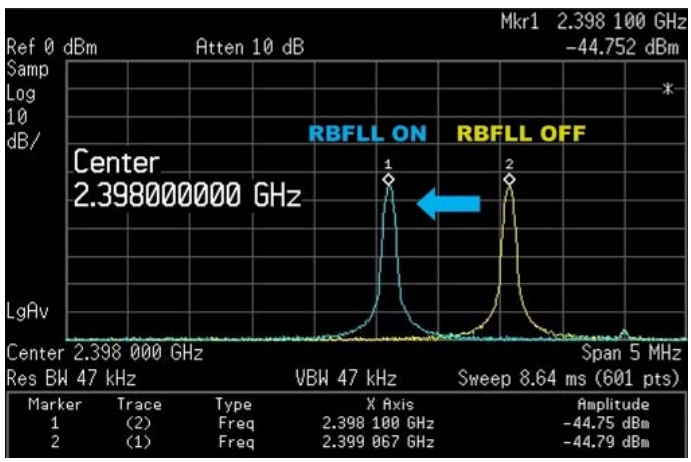

Figure 13.1.5: Measured VCO spectra with RBFLL on and off.

	This Work	[1]	[2]	[3]	[4]	[5]	[6]
Technology (nm)	65	90	130	90	180	180	90
Supply Voltage (V)	0.6	0.5	1	1/1.2	0.65	0.7	1
Modulation	OOK	OOK	FSK	OOK	FSK	FSK	2-tone
Architecture	Low-IF	Uncertain-IF	Low-IF	SRO	SRO	Inj. Lock	RF-ED
Frequency (MHz)	2400	2000	400	2400	2400	920	915
PDC (μW)	227	52	120	534	350/215	420	120
Data-Rate (Mb/s)	1	0.1	0.2	5	2/0.25	5	0.01
Energy efficiency (pJ/b)	227	520	600	106.8	175/860	84	12000
Sensitivity* (dBm)	-83	-72	-90	-75	-75/-86	-73	-83
SIR** (dB) @10MHz (CW/OOK)	-30.5/-22.5	>-10/ -	- / -	- / -	15/ -	>0***/ -	- / -20
Multi-channel	O	X	X	O	O	X	X

* Based on BER of 10^{-3}
** Wanted signal power = sensitivity +3dB
*** Wanted signal power = sensitivity +6dB

Figure 13.1.6: Performance summary in comparison with state-of-the-art ULP RXs.

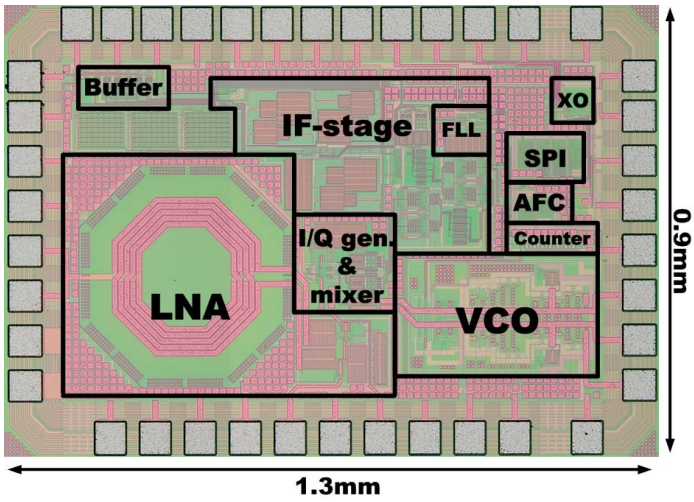

Figure 13.1.7: Die micrograph.

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