Proceedings of Asia-Pacific Microwave Conference 2014 **FR3D-5**

A Low-Power UWB Radar Transceiver with Fast Switching Wideband LNA for Short-Range Detection

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***Abstract* — This paper presents a short-range UWB radar that extends the detection-range. The minimum detectable-range is shortened by the adoption of an LNA with fast-switching operation, whereas the maximum detectable-range is improved by a wideband transceiver. To minimize the power dissipation, the radar transceiver is turned on/off in synchronization with transmit pulses. The proposed radar operates at 4 GHz with 1 GHz bandwidth, and measurements show the detectable-range of 0.1 to 1.5 m for an antenna gain of 2 dBi while consuming 2.13 nJ/pulse from a 1.2 V supply at 1 MHz PRF. The chip occupies an area of 1.98 mm^2.**

***Index Terms* — Low-noise amplifiers, pulse generation, switched circuits, transceivers, ultra wideband radar.**

I. INTRODUCTION

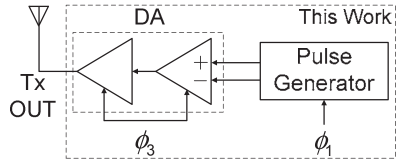
The demand for sensors that can perform short-range object detection has increased for security and traffic control systems. Sensors adopt various types of signals, such as ultrasound, image, optical, and electromagnetic wave. Among them, ultra-wideband (UWB) radar sensors are attractive for detecting objects at short distances because the wideband nature of the UWB signal allows very accurate ranging at a low cost, unlike other sensors.

There has been extensive research on UWB radar sensors for various applications [1], and a simple and low-power CMOS radar transceiver has been reported [2]. In the radar presented in [2], switching operation is adopted in a voltage-controlled oscillator (VCO) and a low-noise amplifier (LNA) for pulse-shaping and transmitter/receiver (Tx/Rx) isolation, respectively. However, slow switching-time and the narrow bandwidth of the LNA lead to deterioration of the minimum and maximum detectable ranges.

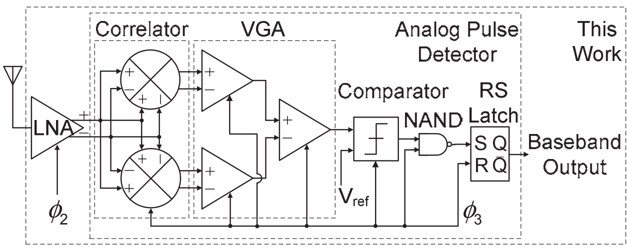
This paper proposes a low-power UWB radar transceiver that includes a fast-switching wideband LNA to improve the detection-range. The following sections describe the architecture, circuit design, and implementation details.

II. SYSTEM ARCHITECTURE

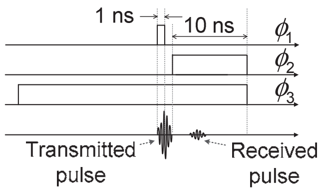
Fig. 1 shows the transceiver architecture and the power on-off diagram of the UWB radar. As shown in Fig. 1 (a), the transmitter generates and emits a UWB pulse signal by a pulse generator, a two-stage driving amplifier (DA), and an antenna.



(a) Transmitter architecture



(b) Receiver architecture



(c) Power on-off diagram of the constituting blocks

Fig. 1. UWB radar transceiver

As shown in Fig. 1 (b), the receiver, which comprises a low-noise amplifier (LNA) and an analog pulse detector, senses the presence of a UWB echo signal and outputs a baseband signal if an echo signal exists.

For such operations, each block of the UWB radar transceiver is turned on/off based on the switching signals ($\phi_{1,2,3}$) as shown in Fig. 1 (c). For the pulse generator, the switching signal ϕ_1, which is high (1.2 V) during half of the pulse-width (1 ns), is utilized to generate a triangular pulse signal. In Fig. 1 (c), to avoid Tx leakage signal, the switching signal ϕ_2 for the LNA goes high after the pulse generation. The switching signal ϕ_2 is kept high during 10 ns to receive echo signals from the range of 1.5 m. For more power reduction, the switching signal ϕ_3 is applied to other blocks.

III. Circuit Design

A. Transmitter

Fig. 2 shows the circuit schematic of the proposed transmitter. As shown in Fig. 2, the pulse generator uses a cross-coupled LC-VCO topology that includes two switches [3]. The LC-VCO comprises an LC tank (L_1 and $C_{1,2}$), cross-coupled transistors $M_{1,2}$, and a current source M_3. With the two switches $SW_{1,2}$, a triangular pulse signal can be generated by the on/off operation of the LC-VCO. As shown in Fig. 2, to drive an external antenna, the two-stage DA is used which consists of a source-follower (SF) – common-source (CS) amplifier $M_{4,5}$, a CS amplifier M_8, and switches $M_{6,9,10,11}$. The capacitors $C_{3,4,6,7}$ are AC-coupled capacitors, and the capacitors $C_{5,8}$ provide AC ground at the drain of the switches $M_{6,9}$. In the DA, the first stage converts differential pulse signals to a single-ended output, while the second stage amplifies the signal for a proper emission level.

Because the DA consumes a large amount of current, switching operation is adopted in the DA by the use of the switches $M_{6,9}$ with the switching signal ϕ_3 as shown in Fig. 1 (c). Since the bias-settling time can be shortened by the transistors $M_{10,11}$, the power consumption can be reduced more. At the gate of the transistor M_8, the transistor M_{10} provides a small amount of current to charge the bias voltage, while the transistor M_{11} bypasses the bias resistor R_B to reduce the RC time constant.

B. Low Noise Amplifier

Fig. 3 shows the proposed two-stage LNA. As shown in Fig. 3, the first stage consists of cascode common-gate (CG) ($M_{1,3}$) and CS ($M_{2,4}$) amplifiers, while the second stage uses a differential cascode CS amplifier ($M_{5\text{-}8}$). The two stages of the LNA utilize the output loads that comprise center-tapped inductors ($L_{1,2}$), capacitors ($C_{1\text{-}4}$), and parallel resistors ($R_{1\text{-}4}$). The center-tapped inductors compensate for the phase and gain differences of differential signals. The capacitors and resistors are used for output impedance matching at the center frequency of 4 GHz with a wide bandwidth.

In the UWB radar transceiver, the LNA dominates the detection-range. To extend the maximum detectable range, the LNA has to receive all of the power of the echo signals. Since the transmitted UWB pulse has wideband characteristics, the wideband bandwidth of the LNA is required. As shown in Fig. 3, the first stage, which uses a CG-CS topology, provides the wideband bandwidth for input matching [4], and to widen an output matching bandwidth, the resonant frequencies of the first and second output loads are slightly different. On the other hand, to reduce the minimum detectable range, a fast-switching LNA is required. In the proposed LNA, two fast-switching techniques are used; the two transistors $M_{9,10}$ are switched to bypass the bias resistors $R_{B2,\,B3}$ to reduce the RC time constants at the gates of the transistors $M_{5,\,6}$, and the inductor loads $L_{1,2}$ fix the drain-bias voltages of the transistors $M_{3,\,4,\,7,\,8}$ to VDD whether the LNA is turned on or off.

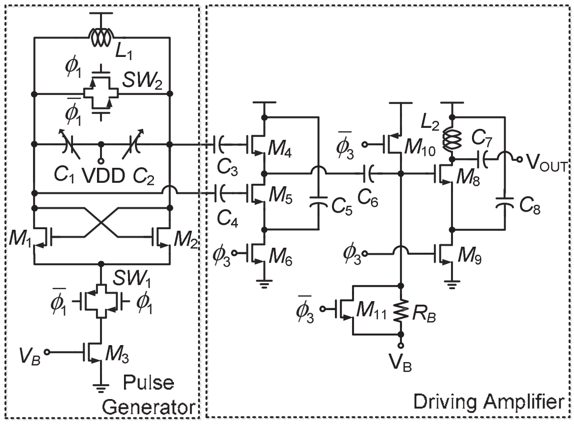


Fig. 2. The proposed transmitter

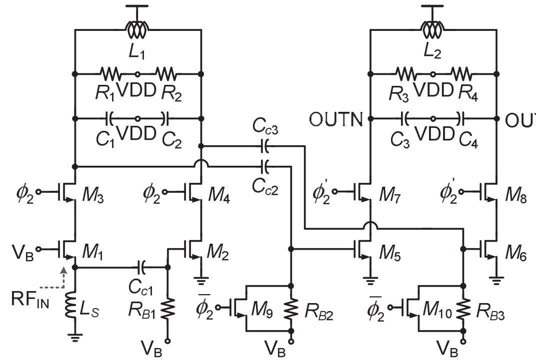


Fig. 3. The proposed LNA

To suppress switching noise from the first stage, the second stage is turned on slightly later than the first stage by using a delayed version (ϕ_2') of the switching signal ϕ_2.

C. Other Blocks

The analog pulse detector comprises a correlator, a VGA, a comparator, and logic gates, as shown in Fig. 1 (a). The correlator is designed as the current-reusing type [2], and the VGA consists of simple differential NMOS amplifiers. To reduce power consumption, the correlator and VGA are turned on/off based on the switching signal ϕ_3 as shown in Fig. 1(c). In the comparator, if an input signal of the comparator is bigger than the reference voltage, a baseband latched signal is generated. According to an input clock signal, the switching signals, shown in Fig. 1 (c), are generated by the timing controller (TC) which consists of NAND gates, inverters, and D flip-flops.

IV. Measurements

Fig. 4 shows a chip photo of the proposed UWB radar transceiver implemented in a 0.13 μm CMOS technology with a size of 1.65 mm × 1.20 mm. The LNA, analog pulse detector, transmitter, and TC consume 310, 30, 1300, and 490 µA, respectively, from a 1.2 supply voltage with a 1 MHz PRF. Considering the on-off operation, the energy consumption of the UWB radar transceiver is 2.13 nJ/pulse.

Fig. 5 shows the transmitted pulse, which was measured in time and frequency domains. As shown in Fig. 5(a), the pulse width and amplitude of the UWB pulse are 2 ns and 0.96 V_{PP}, respectively. As shown in Fig. 5 (b), the average power of the emitted pulse is -59 dBm, and the -10 dB bandwidth of the UWB pulse is 1.09 GHz, thus satisfying FCC regulations [5]. Fig. 6 shows the clock, transmitted RF pulse, and baseband output. To transmit and receive RF signals, two antennas are utilized which have the gain and bandwidth of 2 dBi and 2 GHz, respectively. As a target, a 0.1 m^2 metal plate was used. The reflected signals from the target are detected over the detection range of 0.1 to 1.5 m. From the transmitted power, antenna gain, RCS, and maximum detectable range, the minimum detectable signal power can be found [6], and the proposed radar receiver can detect an echo signal which has a peak power of -93 dBm.

V. Conclusion

This paper reported a low-power UWB radar transceiver with an improved detectable range through fast power-switching time and the wide-bandwidth of an LNA. The measured detection range is 0.1 ~ 1.5 m with an antenna gain of 2 dBi. The minimum detectable signal power is -93 dBm. The die size of the UWB radar transceiver, implemented in a 0.13 µm CMOS process, is 1.98 mm^2, and its core energy consumption is 2.13 nJ/pulse from a 1.2 V supply.

Acknowledgement

This work was supported by the IT R&D program of MOTIE/KEIT. [10047107, 0.13um-CMOS 24GHz ISM-band automotive short range radar]

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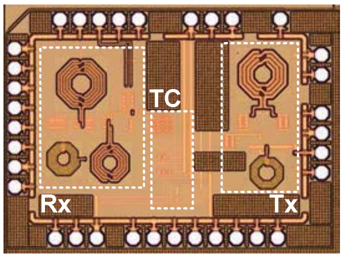
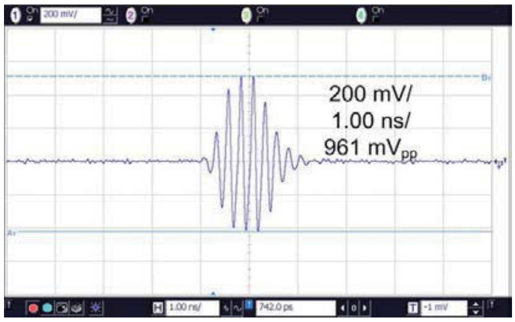
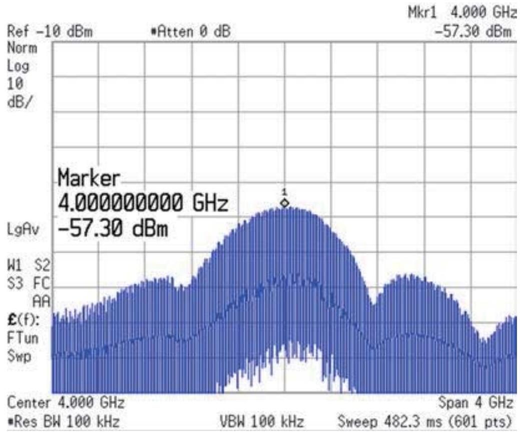


Fig. 4. Microphotograph of the UWB radar transceiver



(a) Time domain



(b) Frequency domain

Fig. 5. The measured Tx pulse

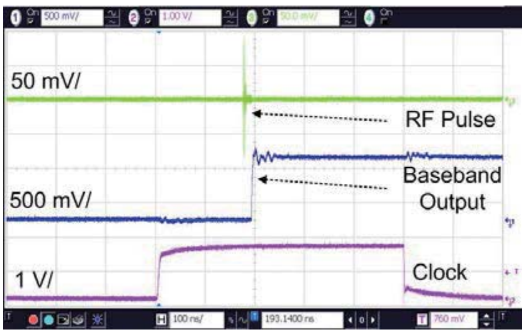


Fig. 6. The measured RF pulse and baseband output