Design and Analysis of Symmetric Dual-Layer Spiral Inductors for RF Integrated Circuits*

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Abstract

An area efficient and symmetric dual-layer spiral inductor structure is proposed and evaluated in comparison with the conventional single-layer spiral inductors. Measurements show that, for a given silicon area, the dual-layer inductor provides nearly 4 time the inductance of the single-layer inductor, while the quality factor is up to 2 times higher. For the same amount of inductance the dual-layer inductors show comparable to higher quality factor depends on frequency of operation. This paper demonstrates that, contrary to the common understanding, the dual-layer can be more useful for the RF integrated circuits than the conventional single-layered spiral inductors from the aspects of area efficiency and quality factor. The proposed dual-layer inductor can also be used as a high-frequency choke.

I. INTRODUCTION

Silicon based RF ICs are becoming ever increasingly competitive in the wide gigahertz frequency range applications. With technology scaling, the silicon processes provide high performance active devices for use in RF applications (e.g., 800 MHz – 2.5 GHz). Although significant progresses has been made, the low quality passive components presents a major huddle for the demand of low cost, low supply voltage, low power dissipation, and low noise implementation of RF integrated circuits.

Monolithic spiral inductors have been used in many microwave and RF ICs such as low noise amplifiers, mixers, voltage controlled oscillators, etc. The monolithic inductors are utilized to implement on-chip matching networks, passive filters, inductive loads, transformers, baluns, etc. The rising demand for the high quality monolithic inductors led to a significant progress in the silicon-based monolithic spiral inductor design techniques. Much of the effort has been given to the enhancement of the quality factors [1, 2, 3, 4].

In spite of all the progresses that have been made, the monolithic spiral inductors are rarely used for the consumer application RF ICs. This is because, in the consumer market, the issue of cost is the most dominating factor that determines the technologies to choose. Needless to say, the spiral inductors tend to be too expensive because of the amount of die area needed. Therefore, in order for the monolithic inductors to come out of the research laboratory and be accepted by the consumer application RF IC designers, it can be said that, the area efficiency is far more critical issue that needs to be resolved than the quality factor.

In this paper, a novel monolithic symmetric dual-layer spiral inductor is proposed and compared with the conventional single-layer structures. The new structure demonstrates better performance in symmetry, area efficiency, and quality factor, compare to the conventional structures. The design aspects of the single-layer versus double-layer inductors are discussed and the measurement results are analyzed.

II. INDUCTOR DESIGN

Figure 1 shows the layout of the conventional single-layer square spiral inductor. As can be seen from the figure, the three-turn inductor layout is simple and requires double metal process. Typically, the spiral inductors use the metal widths of 10~20 μm with minimum spacing and the metal thickness is the dominating factor that determines the quality factor in the RF frequencies (below 3 GHz). The hollow area in the center of the inductor helps to improve the quality factor of the inductor [5].

Figure 2 shows the layout of the proposed symmetric dual-layer square spiral inductor. In Fig. 2, placing the metal-2 layer (shown on the left side) on top of the metal-1 layer (shown on the right side) forms the final inductor. As can be seen from Fig. 2, following the numbered dashed line, the alternation of the metal layers leads to a perfectly symmetric inductor structure. Other similar forms of multi-level spiral inductors have been suggested [6], but their designs are not symmetric. Generally, it is nice to have symmetric passive elements and some RF designs require symmetric inductor [7].

Basically, the dual-layer spiral inductor is a cascaded

* This work was supported by the Ministry of Information and Communications Grant # 98-159-03

connection of two single-layer inductors. If we assume the self-inductance of the each layers in Fig. 2 as L_S, the inductance of each inductor layers in dual-layer configuration is the sum of the self-inductance of each layer plus the mutual inductance. Assuming 100% coupling between the 1st- and 2nd- layer, the overall inductance of the dual-layer inductor is expected to be $4*L_S$. The fact that same amount of inductance can be obtained utilizing only one fourth of the area is something that can not be underestimated.

Typically, at radio frequencies (0.3~3 GHz), the dominating factor that determines the quality factor of the spiral inductors is the metal resistance. From Fig. 1 and 2, assuming that the thickness of the 1st- and 2nd-metal are the same, the series metal resistance of the dual-layer inductor is approximately twice that of the single-layer inductor. For a simple equivalent model of a resistor and inductor in series, the quality factor of the single- and double-layer inductor can be expressed as $Q_{single} = \omega L_S/R_S$ and $Q_{dual} = 4\omega L_S/2R_S = 2Q_{single}$, respectively. Therefore, in principle, for a given inductor size, the dual-layer can not only provide 4 times higher inductance but two times higher quality factor than that of the single-layer inductor.

III. MEASUREMENT RESULTS AND DISCUSSIONS

Figure 3 shows the photos of the dual- and single-layer inductors fabricated on a 4-metal 0.35-μm CMOS process. The thicknesses of the 1st-, 2nd-, and 3rd-metals are about 0.6 μm and the 4th-metal thickness is about 1 μm. The resistivity of the 1st-, 2nd-, and 3rd-metals are 80 mΩ/square and the 4th-metal resistivity is 40 mΩ/square, respectively. Inductors are fabricated for two different hollow areas, 50x50 μm² and 100x100 μm². The number of turns covers 2 to 6. The metal line width of 10 μm and the spacing of 1 μm are used for all the inductors. The single-layer inductors used the 4th-metal for the spiral. The dual-layer inductors used the 4th-metal as the upper layer and both the 2nd- and 3rd-layers as the lower layer. Due to the discrepancies in metal layer thickness, the lower layer of the dual-layer inductors provides approximately the same metal thickness and resistance as the upper layer (4th-metal). Therefore, in both series resistance and the inductance wise, the inductors shown in Fig. 3 closely satisfies the conditions discussed in the previous section.

Figure 4 shows the inductance of the fabricated single- and dual-layer inductors as a function of the number of turns, for the hollow area sizes of 50x50 and 100x100 μm², respectively. In Fig. 4, the inductance of the dual- layer inductors show 3.5 ~4 times higher values than that of the single-layer for the corresponding 50x50 and 100x100 μm² hollow area sizes, respectively. This means that the mutual coupling between the upper and lower layers of the dual-layer inductors is very close to 1 and it is in good agreement with the prediction.

Typically, the quality factors of the reactive elements are determined from the admittance Y_{11}. This most widely used Q, which is referred as Q_{conv} in this paper, is given by $-Im(Y_{11})/Re(Y_{11})$, where Im and Re represents imaginary and real part. When the quality factors are estimated as Q_{conv}, the dual-layer inductors show significantly worse quality factor performances than what is expected from the discussions in the previous section. It can be shown that the significantly lower resonance frequency of the dual-layer inductors is the main cause for the poor quality factors. This is expected from the layout shown in Fig. 2 as the dual-layer inductors have extra capacitance between the upper and lower layer. It is this poor quality factor that excluded the dual-layer inductors from the list of the useful passive devices.

Lately, O [8] proposed a new method, more relevant to circuit design, for estimating quality factors. His method extract Q factors, which is referred as Q_{BW} in this paper, by numerically adding a capacitor in parallel to measured Y_{11} data of the inductor, and by computing the 3-dB bandwidth at the resonant frequency of the resulting network. As O proposed, the quality factor obtained using the new method suggest that the quality factor remains high and the inductors remain useful up to its self-resonant frequencies. Figure 5 compares the quality factor of the single- and dual-layer inductors following the O's method for 2 and 3-turn sizes (hollow area = 100x100 μm²). As can be seen from Fig. 5, the Q_{BW} of the dual-layer inductors are up to 2 times higher than that of the single-layer inductors, especially with smaller size and lower frequencies. The quality factor degradation at higher frequencies and for larger sizes might be explained by a few factors. In Fig. 2, the symmetric dual-layer inductor has additional series resistances due to the multiple switching between the upper and lower layers through vias. It is also well known that the losses within the semiconducting substrate contribute to the quality factor degradation [9]. The closer the metal layers to the substrate the higher the substrate loss. As described previously, the lower layer of the dual-layer inductors use 2nd-metal, therefore, it is closer to the silicon substrate than the metal layers (4th-metal) used for the single-layer inductors.

Perhaps it is more appropriate to compare the quality factor between the single- and dual-layer inductors of the same inductance. Fig. 6 shows the comparison. As can be seen from Fig. 6, the quality factor remains the same up to 2 GHz and then the quality factor of the dual-layer inductor gets higher than that of the single-layer inductor.

Figure 7 shows the impedance seen at port 1 and 2 of the inductors as a function of frequencies. Fig. 7(a) clearly demonstrates the symmetric nature of the dual-layer inductor compare to the conventional single-layer inductor shown in Fig. 7(b). In Fig. 7, the inductance of the 2 and 3 turn dual-layer inductors are the same as that of the 4 and 6 turn single-layer inductors, respectively. The lower resonance frequencies of the dual-layer inductors can be seen from the figure. From Fig. 7, the low resonance frequencies of the dual-layer inductors suggest another possible application, the RF choke. RF choke is one of the very frequently requested components in RF IC design.

Overall, with no reservation, the dual-layer seems have definite advantages over the single-layer inductors considering the area efficiency and quality factor.

IV. CONCLUSION

A novel symmetric dual-layer spiral inductor structure is proposed and the performance is estimated and compared to that of the single-layer. Inductors are fabricated based on a 4-metal 0.35 μm CMOS process. Measurement results demonstrate that, for a given silicon area, the dual-layer inductors can provide about 4 times higher inductance than that of the single-layer and up to 2 times higher quality factor. With even same value of inductance, the dual-layer inductors provide comparable to higher quality factors. Moreover, the proposed dual-layer structure is symmetric and proposes as a candidate for the high impedance choke at radio frequencies. The result of this work strongly suggests that the multi-layer inductors seem to be the choice of the monolithic inductors for many RF applications. From the cost driven designers stand point, this should be a remarkable fact.

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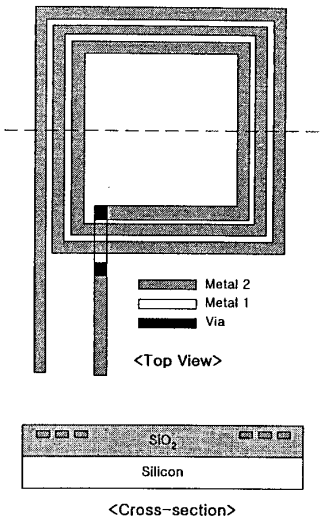


Fig. 1. Conventional single-layer inductor structure.

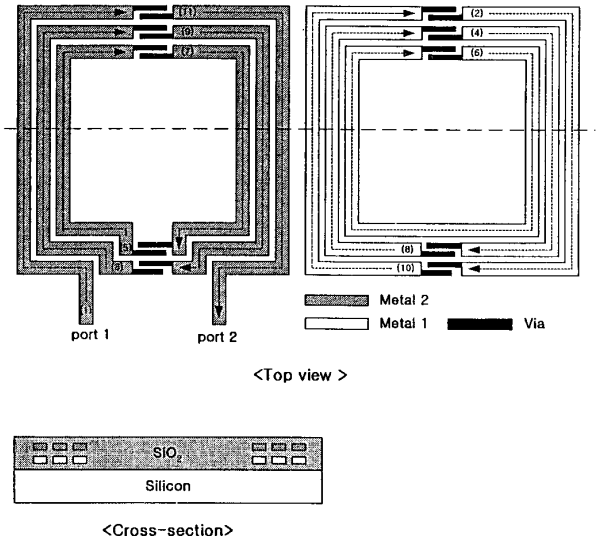
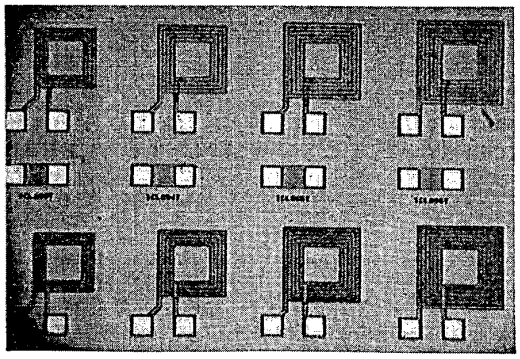
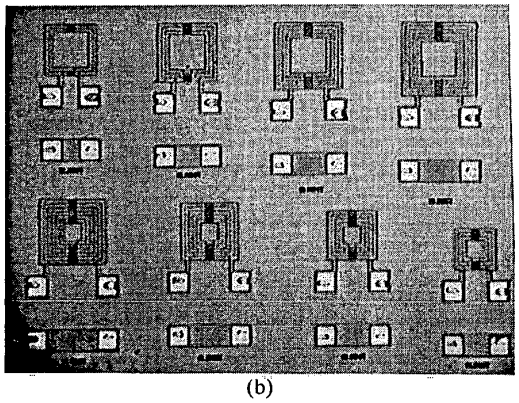


Fig. 2. Symmetric dual-layer inductor structure.



(a)



(b)

Figure 3: Photo of the fabricated inductors. (a) single-layer spiral inductors (b) symmetric dual-layer spiral inductors.

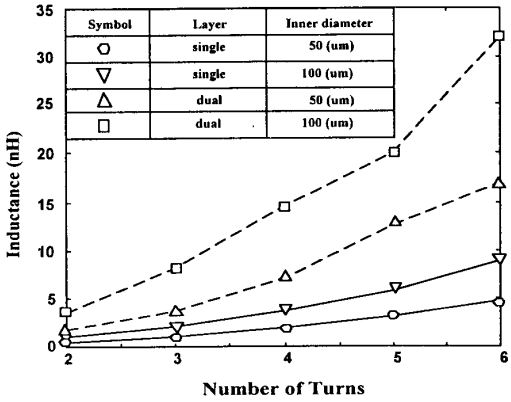


Figure 4. The inductance of the single- and dual-layer inductors as a function of the number of turns, for the hollow area sizes of 50x50 and 100x100 μm^2, respectively.

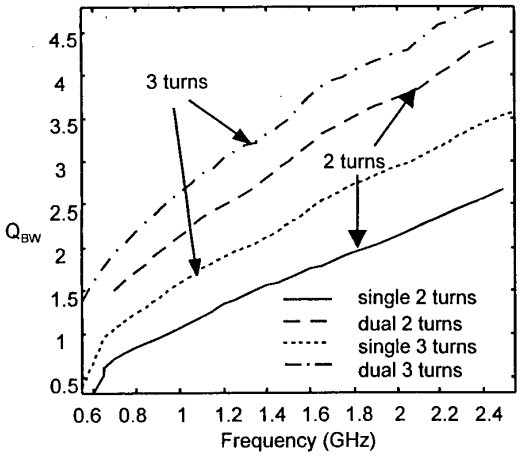


Fig. 5. The quality factor, Q_{BW}, of the single- and dual-layer inductors. Two and three turn inductors are compared. The size of hollow areas for these inductors is 100x100 μm^2.

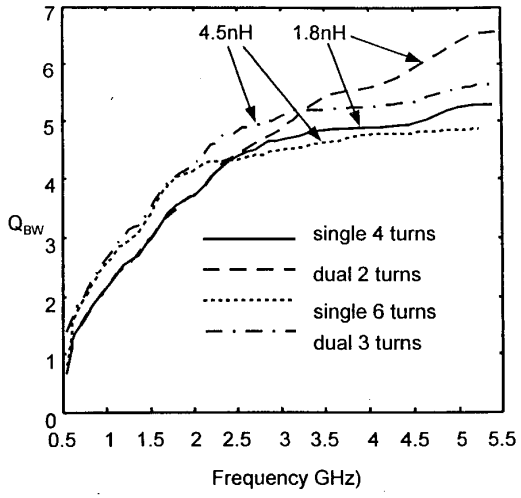
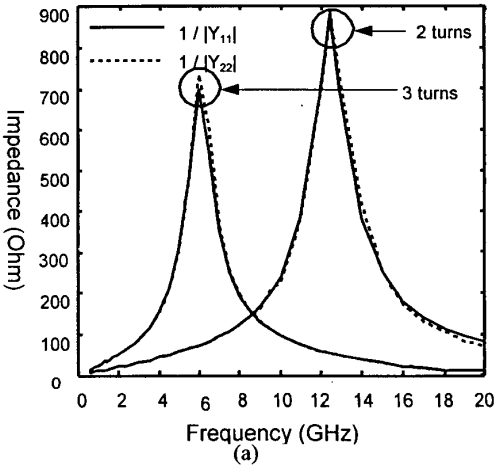
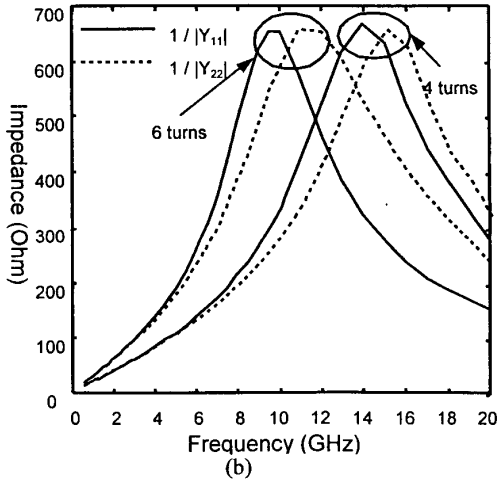


Fig. 6. The quality factor, Q_{BW}, of the single- and dual-layer inductors. Note that the inductance of the single- and the corresponding dual-layer inductance is the same.



(a)



(b)

Fig. 7. Impedances seen at each ports of inductors (a) dual-layer (b) single-layer.