An Adaptive Bias Circuits for High Effciency Power AMP

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Abstract: An adaptive bias circuit to improve the efficiency of the power amp is proposed that control the DC current of the power amp as a function of input power. The proposed circuit uses the class-AB characteristics of the common-source amplifier. The considerations for the optimum biasing of the power amp are discussed.

Keywords
Power amplifier, dynamic bias, high efficiency, CMOS.

I. Introduction

In the last few years, the explosive growth in the mobile communication markets lead to continuous development of the mobile phones. From the size and price wise, today's mobile phones have shown remarkable improvements. The battery is one of the main components that determine the size of the mobile phone. Since the power amplifier (PA) dissipates the highest amount of power, the power efficiency of the PA and the battery size has close relations.

Typically, the PAs used for the CDMA systems choose the class A topology in order to satisfy the high linearity requirements. The class A amplifiers are inherently poor in power efficiency, typically 25 ~ 35 % at its maximum output. Furthermore, due to the power control function of the CDMA system, the PA operates at much lower powers than its maximum output power, most of the time. Therefore, the effective efficiency can be significantly lower than the maximum efficiency. One way to improve the efficiency is to reduce the DC power consumption for the small input, by reducing the supply current and/or the supply voltage [1-5].

The advantage of controlling the gate and drain voltage of the power-amplifying transistor (PAT) has been well described by Yang [1]. However, the actual implementation of the gate and drain voltage control circuit has many practical limitations. The methods suggested in [1], couplers, DC-DC converter, and the digital control using switch controller and bias switch array, are not practical, especially with the mobile phones.

This paper presents an IC compatible gate control circuit and the methodology to improve the PA efficiency through the adaptive control of the gate voltage.

II. Gate Bias Control Circuit

Figure 1 shows the simplified schematics of the gate bias circuit. In Fig. 1, Q_1 works as a detection circuit and Q_2 with R_2 works as a gate control circuit.

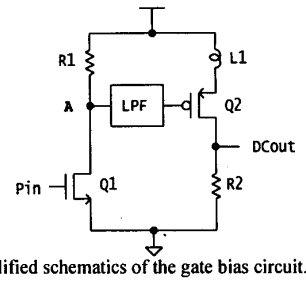

Fig 1. The simplified schematics of the gate bias circuit.

As described in [6], when the amplitude of the small-signal input (P_{in}) increases, the nonlinear characteristics of the common-source amplifier leads to an increase in the DC drain current of Q_1. Biasing Q_1 at low DC voltage (near threshold voltage) helps to accelerate this effect, as the phenomenon can be understood as a result of the class-AB operation of the amplifier. The increase in Pin generates higher order harmonics as well at the node A.

The low pass filter suppress the AC signals and transfer only the decrease in the DC voltage at node A. It is important that the AC signal at the DC_{out} would be low enough not to cause any problems.

Figure 2 shows a possible implementation of the adaptive bias circuit applied to a power transistor Q_3. In Fig. 2, L_3 and C_2 are used as an input matching components, and C_1, C_3, L_1, and L_2 are all part of the low pass filter. The detection transistor Q_1 should be small enough that it would have negligible effect on the input characteristics of the power amplifier.

Figure 3 shows the variation of the gate voltage for the transistor Q_3 (the power amplifying transistor: PAT) as a function of the input power based on simulations. A 0.35-micron CMOS transistor parameters are used for the simulations.

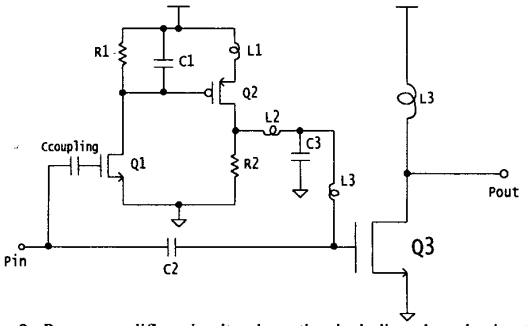

Fig 2. Power amplifier circuit schematics including the adaptive bias circuit.

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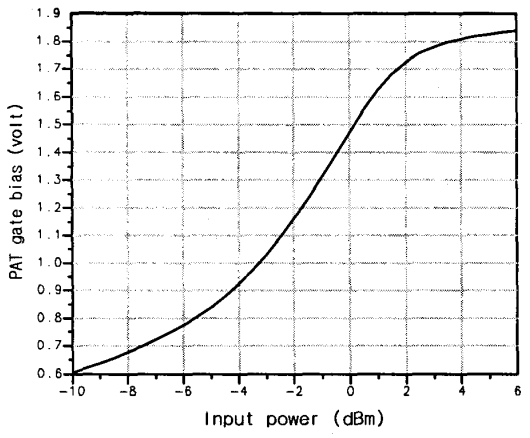

Fig 3. The variation of the DC gate voltage for the PAT (Q_3) as a function of the input power.

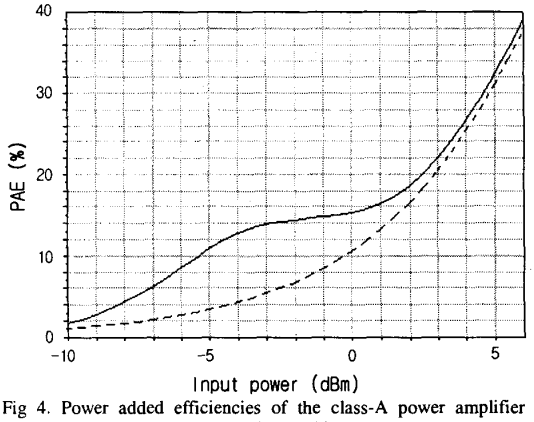

Fig 4. Power added efficiencies of the class-A power amplifier with (solid) and without (dotted) the adaptive bias network.

Figure 4 compares the power-added efficiency of the power amplifier shown in Fig. 3, with and without the adaptive bias network. As can be seen in Fig. 4, the adaptive bias circuit improves the efficiency significantly at the low input powers.

III. Optimizing Gate Bias

In controlling the PAT gate bias for a given input power, deciding the optimum gate voltage is an important consideration. If the PAT gate voltage is adjusted too low, the PA can operate outside the linear region. For the opposite case, the efficiency will be sacrificed. The optimized gate bias can be formalized as a function of the input power, satisfying both the linearity and the efficiency. Figure. 5 shows the maximum ranges for the output voltages and currents of the PAT for each gate bias. The I_D-V_{GS} is assumed linear considering low sub-micron CMOS technology.

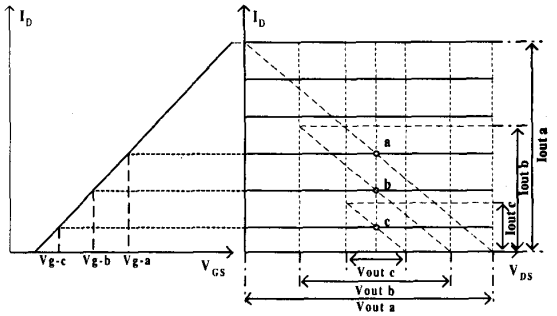

Fig 5. The I_D-V_{GS} and I_D-V_{DS} plots of a FET showing the load lines of three different bias points.

In Fig. 5, $V_{out\,a}$, $V_{out\,b}$, $V_{out\,c}$, $I_{out\,a}$, $I_{out\,b}$, and $I_{out\,c}$ represents the output voltage and current swing ranges without clipping for each gate bias. As can be seen from Fig. 5, for a given supply voltage and the optimum load impedance (Z_{opt}), the DC drain current determines the maximum output power. Therefore, the output power (P_O) can be expressed as a function of the DC drain current (I_D). Or, conversely, I_D can be expressed as a function of the P_O.

$$I_D = \sqrt{\frac{2 \cdot P_o}{Z_{opt}}} \qquad \text{eq (1)}$$

If we assume that the PA gain stays constant, $P_O = P_I + G$ where P_I is the input power and G the PA gain. Since we have assumed a linear relation between I_D and V_{GS}, I_D can be expressed as $I_D = G_m \cdot (V_{GS} - V_t)$ where G_m is the large-signal transconductance and V_t is the threshold voltage of the MOSFET. In summary, the PAT gate voltage V_{GS} can be given by

$$V_{GS} = \frac{1}{G_m} \cdot \sqrt{\frac{2 \cdot (P_I + G)}{Z_{opt}}} + V_t \qquad \text{eq (2)}$$

Equation (2) tells us that the optimum gate bias can be uniquely determined as a function of the input power for a given PA gain and the large-signal transconductance. In equation (2) the PA gain is assumed constant. This requirement may be satisfied by limiting the minimum gate bias range. Figure 6 shows the variation of the PA gain as a function of the gate voltage. In Fig. 6, the lower limit of the gate bias is set as the point where the PA gain drops 1-dB below the normal value. From [2], the upper limit of the gate bias can be set as $(V_{DD} + V_{TH})/2$ for maximum output power, where V_{DD} is the supply voltage and V_{TH} the threshold voltage.

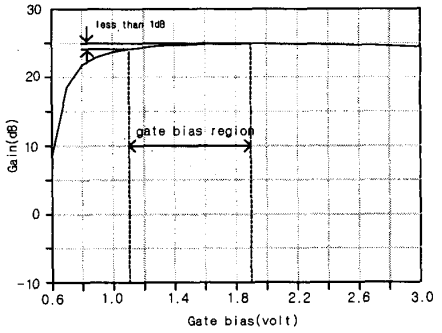

Fig 6. PAT Gain vs PAT gate bias voltage.

IV. Conclusion

An adaptive bias circuit to improve the efficiency of the power amplifiers at low output powers is presented. The proposed bias circuit utilizes the class-AB nature of the common-source amplifiers. The improvements in efficiency are demonstrated through simulations for a CMOS power amplifier. The guidelines for the optimum selection of the gate biases are suggested as a function of the power amp gain, the large-signal transconductance, and the input power.

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