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High-Q Poly-to-Poly Capacitor Design for RF Applications

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Abstracts

A very high-Q poly-to-poly capacitor structure and the measurement results are presented. The poly-to-poly capacitor is designed on a conventional 0.35 μm CMOS process. Through the layout optimization, the Q-factor greater than 120 is obtained at 2 GHz.

Introduction

CMOS technologies are increasingly competitive in the wireless applications. For low power high performance design, not only the high performance active devices, but the availability of high-Q passive components play a key role. Ideally, the capacitors should be cheap, area-efficient, linear, have low parasitic capacitances and resistances. With conventional silicon processes, the poly-to-n$^+$ and poly-to-poly capacitor types are generally provided. The poly-to-n$^+$ capacitors are typically the most area efficient, but the high parasitic series resistance, the strong voltage dependence, and the n$^+$-to-substrate parasitic capacitance limit the usefulness for RF applications. The poly-to-poly capacitors are commendable except the high series parasitic resistance. The metal-to-metal capacitor is the best option in performance, but not available in conventional CMOS process and requires additional process steps. This work reports a remarkable improvement in the quality factor of the poly-to-poly capacitors through the layout optimization.

Capacitor design

For a simple square type capacitor structure shown in Fig. 1, the small-signal equivalent circuit can be represented as shown in Fig. 2.

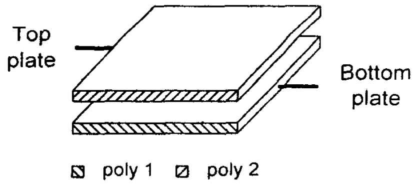

Figure 1. A simple square type capacitor structure.

In Fig. 2, the resistor R_C represents the series spreading resistance of the poly-silicon top and bottom plate, C_C the poly-to-poly capacitance, C_{ox} the bottom poly to silicon substrate parasitic capacitance, and R_{sub} the substrate resistance. From Fig. 1, the Q-factor seen from the top plate at a given frequency is proportional to $(\omega R_C C_C)^{-1}$. For the given square type poly-silicon plate, R_C is independent of the plate size. Therefore, in order to increase the Q-factor, the capacitor size should be minimized.

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Hence, in principle, the high-Q capacitor can be realized simply by paralleling a number of small unit cell capacitors.

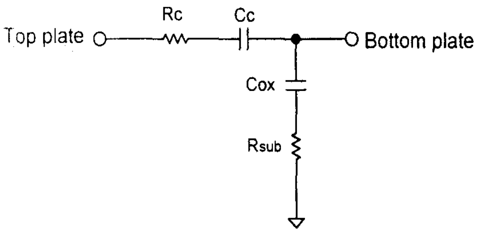

Figure 2. A small-signal equivalent circuit of a practical capacitor.

The maximum Q- factor of the capacitor is determined by the size of the unit cell. Similar idea has been reported in the previous work [1]. The problem with this approach is that the smaller the unit cell size the larger the bottom plate parasitic capacitance (C_{ox}) because of the surrounding bottom plate connection. Also, the mesh type interconnects combining each unit cell become quite complicated and the Q-factor is limited by them.

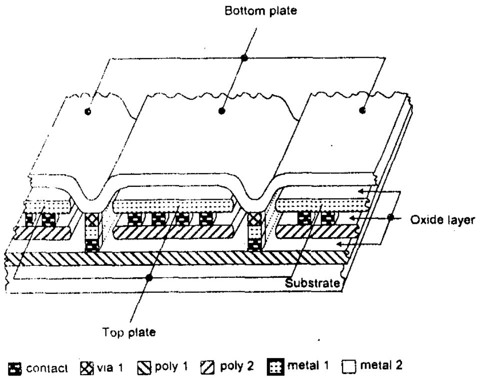

Figure 3. The structure of the high-Q poly-to-poly capacitor. test structure.

Figure 3 shows the proposed high-Q poly-to-poly capacitor structure. In Fig. 3, for the top plate, the long rectangular shape poly 2 plates are used covering most of the capacitor area except the long skinny slits. The same size metal 1 covers the top-poly plates and they are connected through multiple contacts. Therefore, the top-plate spreading resistance is, effectively and approximately, the same as the spreading resistance of one square metal plate. The bottom plate poly is accessed through the long skinny slits as shown in Fig. 3. As can be seen from Fig. 3, effectively, the bottom plate is composed of multiple rectangular plates connected in parallel. The overall aspect ratio and the sheet resistance of the bottom plate will determine the overall series resistance of the bottom-poly. Each of the rectangular bottom plates are initially accessed through the skinny metal lines (metal 1) from the outside, which could end up with the same interconnection problems as previous case. However, in this design, another metal plate (metal 2) is placed on top of the metal 1 and connected with the skinny interconnect lines through multiple via. Therefore, the metal 2 replaces the inductive and resistive parasitics of the skinny interconnects. As a result, for enough aspect ratio of the bottom poly, the spreading resistances of metal 1 and 2 plates dominate the overall series resistance of the capacitor, leading to a very high-Q capacitor structure.

Measurement Results and Discussions

The proposed high-Q capacitor is implemented in a 0.35 μm CMOS process. The poly-to-poly capacitor has 1 fF/μm^2. The thickness of poly 1, poly 2, and the interpoly oxide are 0.275 μm, 0.18 μm, and 0.037 μm, respectively. The sheet resistance of poly 1, poly 2, metal 1, and metal 2 are 7.49, 7.78, 0.085, and 0.085 Ω/ , respectively.

The two-port S-parameters of the fabricated capacitors are measured on-wafer and the one-port Q-factor is extracted from Y_{11} and Y_{22}. The bond-pad parasitics are Y-parameter de-embedded. Considering the small series resistance of the capacitors, it is critical to make sure that the contact resistance between the probe-tip and the test structure is negligible. Figure 4 shows the Q-factor of a 1 pF poly-to-poly capacitor as a function of frequency.

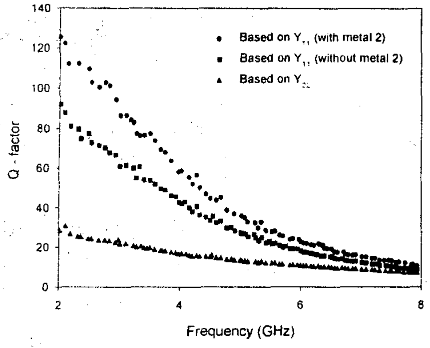

Figure 4. The measured Q-factor of the poly-poly capacitors as a function of frequency.

In Fig. 4, the top curve represents the Q-factor based on Y_{11}, which represents the Q-factor when the signal is applied on the top plate port and the bottom plate port is grounded. As can be seen from Fig. 4, the Q-factor is higher than 120 at 2 GHz, and the extrapolated Q-factor at 1 GHz is 266. Table 1 summarizes the Q-factors of lately published high-Q capacitors [1-6].

Table 1: Q-factors, published and this work.

Ref.	Capacitor type	Frequency (GHz)	Q - factor
[1]	MOS	0.9	> 100
[2]	poly-to-poly	1	185
[3]	poly-to-poly	2	> 100
[4]	MIM	2	> 100
[5]	MIM	2	60
[6]	MIM	2.5	80
This work	poly-to-poly	2	>120

As shown in Table 1, the Q-factor of this work is better than that of the MIM capacitor [4-6]. The bottom curve of Fig. 4 shows the Q-factor based on Y_{22} meaning the signal is applied at the bottom plate port with top plate grounded. The Q-factor at 2 GHz is less than 30. The degradation in Q-factor reflects the effect of substrate resistance (see Fig. 2). In Fig. 4, the middle curve represents the Q-factor based on Y_{11} when the metal 2 (see in Fig. 3) is not used. At 2 GHz, the Q-factor is >80 which is respectful, but clearly demonstrates the degradation in Q-factor by the interconnect parasitic.

Figure 5 shows the extracted capacitances. In Fig. 5, the parasitic capacitance C_{ox} is approximately 20% of the poly-to-poly capacitance C_c

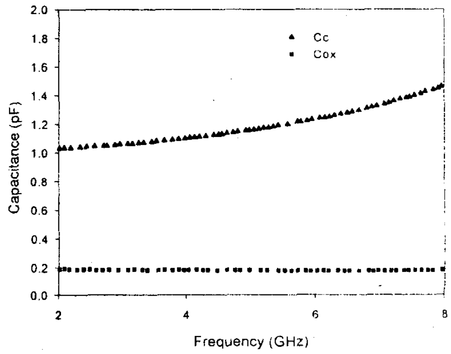

Figure 5. The measured poly-to-poly capacitance (C_c) and the substrate capacitance C_{ox} as a function of frequencies

Conclusion

A very high-Q poly-to-poly capacitor structure is proposed and implemented on a conventional 0.35 μm CMOS process. Based on the on-wafer measurement, the quality factor greater than 120 is obtained at 2 GHz from a 1 pF capacitor. To the author's knowledge, it is the highest quality factor that has been reported which is realized on silicon technology. The design and the measurement details are described.

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