A LOW POWER, HIGH GAIN LNA TOPOLOGY

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Abstract: A novel high gain and low noise amplifier topology is proposed. The proposed LNA topology is a current sharing two-stage cascade amplifier adopting a series inter-stage resonance. The performance of the proposed topology is compared with the existing high gain amplifiers, qualitatively and quantitatively. The simulation results at 2.4 GHz based on 0.35 μm CMOS technology are also provided. The proposed topology demonstrates excellence over the existing high gain topologies in gain and noise figure.

Index Term - RF, low noise amplifer, CMOS, low power, LC resonance

I. Introduction

Continued improvements in Si technology have made GHz circuits feasible, even in CMOS. The storng demand for portable wireless communicaion systems drives RF IC based on CMOS technology. CMOS technology is attractive considering the low cost and high density integration. Recently, highly integrated CMOS RF ICs has been introduced at the commercial market, for example, the bluetooth applications which requires very low cost RF transceiver. The problem with CMOS technology for RF applications is the low transconductance. It is very difficult to obtain high gain with CMOS process, especially at low power and high frequencies.

II. Existing LNA topology

Achieving high gain with CMOS amplifier usually involves high power. However, due to the square-root dependence of the MOS transistor transconductance on the drain current, increasing power is not an efficient way of boosting gain.

Methods of acquiring higher gain without significant increase in power dissipation have been introduced through current sharing techniques. Some of the typical examples are shown in Fig. 1, 2, 3, and 4. Figure 1 is a cascode amplifier. In Fig. 1, R_G is the bias resistor and Z_L the load impedance. The cascode amplifier is composed of common-source and common-gate amplifiers in cascade. The common-gate stage provides low impedance at node X, shown in Fig. 1, leading to negligible Miller effect on the common-source stage. The common-base stage has inherently wide-bandwidth characteristics. The high output impedance of the common-base stage along with the extended overall bandwidth leads to high gain at high frequencies, which explains the popularity of the cascode in CMOS LNAs [1].

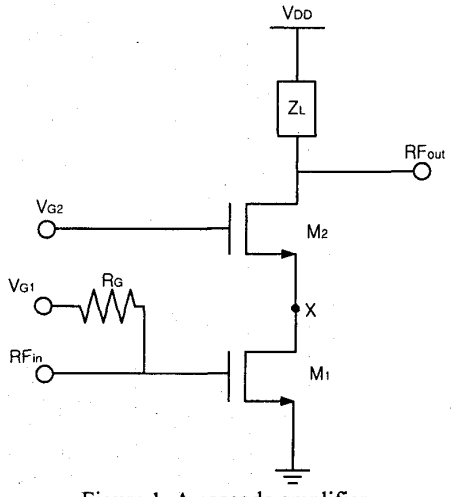

Figure 1. A cascode amplifier

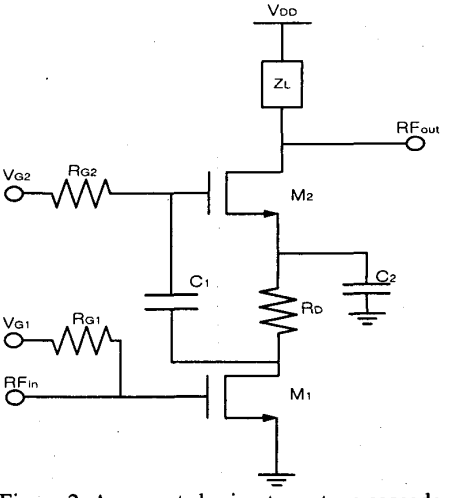

Figure 2. A current sharing two-stage cascade amplifier with resistive 1st-stage load.

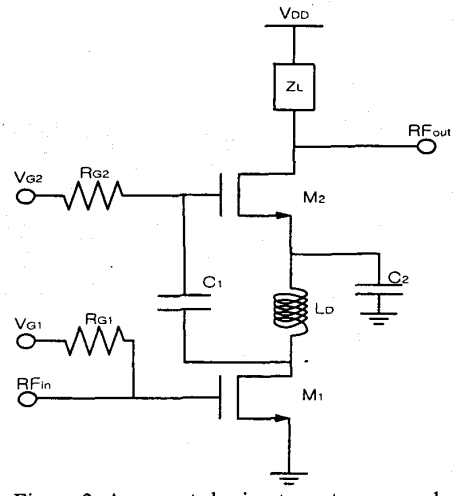

Figure 3. A current sharing two-stage cascade amplifier with inductive 1st-stage load.

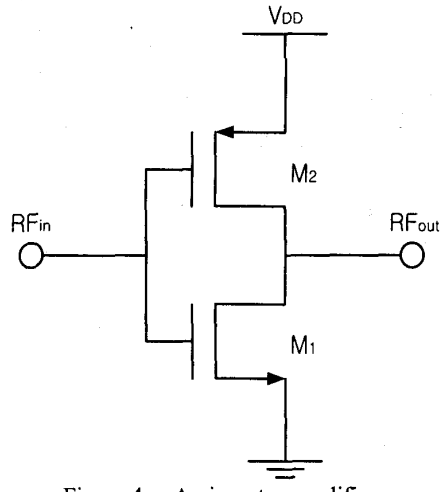

Figure 4. An inverter amplifier.

Note that the transconductance of the cascode amplifiers are limited by the transconductance of the common-source stage only. Figure 2 shows an approach to boost gain through the multiplication of the transconductances of the two cascading stages [2]. In Fig. 2, R_D is the load resistor, R_{G1} and R_{G2} the bias resistors, respectively, C_1 the coupling capacitor, C_2 the bypass capacitor, and Z_L the load impedance. In Fig. 2, the two cascading common-source amplifiers share the same supply current to reduce the power consumption. However, the two common-source amplifiers experience the Miller effect. Figure 3 is a variant of Fig. 2 where R_D is replaced with a choke (L_D) in order to reduce the DC voltage drop.

Figure 4 is the well-known CMOS inverter topology. When used as an amplifier, the overall transconductance is the sum of transconductances of each transistor [3]. In Fig. 4, the N- and P-MOSFET common-source amplifiers are effectively in parallel combination. Compare to the previous topologies, this circuit involves more components for the input and output matching. Furthermore, the P-MOS transistor performance is considerably worse than that of the N-MOS at high frequencies, yet the output impedance is reduced in half.

Considering the over all transconductance, the cascade topology (Fig. 2 and 3) provides the maximum gain at low frequencies, the inverter (Fig. 4) is the next, and the cascode (Fig. 1) is the last. As frequency goes up, the cascade topology would be affected the most by the Miller effect, the inverter would be the next, and the cascode would be the least affected. However, since these amplifiers are categorized as tuned amplifiers, the general bandwidth concept cannot be directly applied [4]. From the simulation, for a 0.35 CMOS process at 2.4 GHz, the higher gain is obtained from the cascade than the cascode topology.

III. Proposed LNA Topology

Figure 5 shows the small-signal equivalent circuit of the 2nd-stage of the cascode amplifier shown in Fig. 1. In Fig. 5, Y_{sub} represents the parasitic admittance between the node X and the silicon substrate. This admittance is composed of the drain (M_1) and source (M_2) junction capacitances in series with the respective substrate resistances.

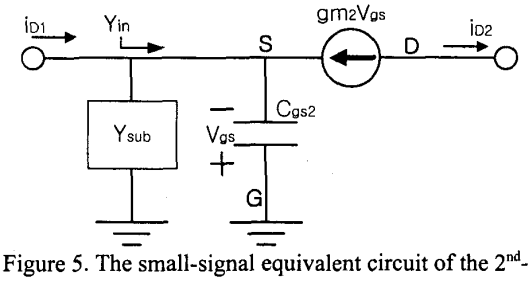

Figure 5. The small-signal equivalent circuit of the 2nd-stage of the cascode amplifier.

The power loss through Y_{sub} can be significant in CMOS RF IC design [5]. In Fig. 5, i_{D1} and i_{D2} represent the drain currents of M_1 and M_2. From Fig. 5, i_{D2} can be expressed as

$$i_{D2} = \frac{g_{m2}}{sC_{gs2}+Y_{sub}+g_{m2}} i_{D1} \qquad (1)$$

where g_{m2} is the transconductance of M_2 and C_{gs2} the gate-source capacitance of M_2. As can be seen from eq. (1), at high frequencies, depends on the transistor sizes and the resistivity of the silicon substrate, the current gain of the common-gate stage can be significantly degraded by Y_{sub} and C_{gs}. Typically, in CMOS RF amplifiers for portable applications, the transistor sizes tends to be maximized to improve the gain and noise figure for the limited amount

of bias current. Therefore, with practical cascode type RF amplifiers based on CMOS, the current gain of the common-gate amplifier tends to be considerably less than one, which leads to less overall power gain. Furthermore, the high Y_{sub} at node X in Fig. 1 leads to higher noise figure [6]. The noise signals generated from the transistor M_2 are amplified by the transistor itself as the impedance at node X degrades.

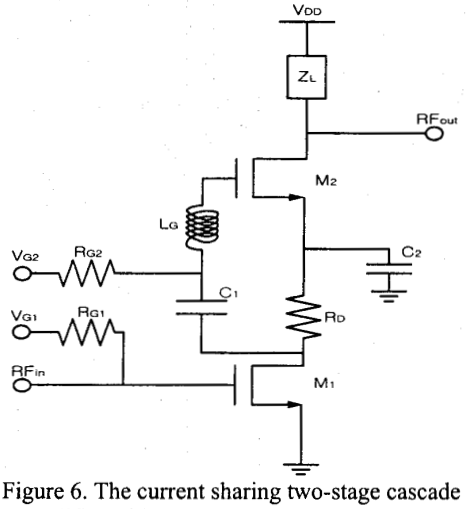

Figure 6. The current sharing two-stage cascade amplifier with a series inter-stage resonance.

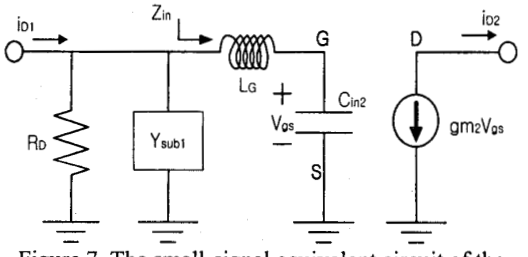

Figure 7. The small-signal equivalent circuit of the inter- and 2nd-stage of the proposed LNA architecture.

Figure 6 shows the proposed low power and high gain LNA topology which is a variant of the circuit shown in Fig. 2 and 3. In Fig. 6, R_D C_1, C_2, R_{G1}, R_{G2}, and Z_L does the same function as in Fig. 2. The difference between Fig. 2 and Fig. 6 is that, instead of cascading the two common-emitter amplifiers directly as in Fig. 2, the L_G in Fig. 6 is in series resonance with the input capacitance of the 2nd-stage, C_{in2}. The series resonance of L_G-C_{in2} provides low impedance at the drain of the transistor M_1 such that the 1st common-emitter stage do not experience the Miller effect at the frequency of interest, which is different from the case shown in Fig. 2. There is no voltage gain from the input of the amplifier to the drain of M_1, but, there is a voltage gain from the drain of M_1 to the gate of M_2 when the quality factor of the resonant circuit L_G-C_{in2} is greater than one. Therefore, effectively, there is a voltage gain from the input node of the 1st-stage to the input node of the 2nd-stage amplifier, however, the 1st-stage amplifier do not experience the Miller effect. The low impedance created at the drain node of M1 obviates the Y_{sub} problem discussed with the cascode amplifier.

The principles of the high gain characteristics of the proposed topology can also be understood from current gain aspects. Figure 7 shows the small-signal equivalent circuit of the inter- and 2nd-stage part of the proposed LNA. In Fig. 7, Y_{sub1} represents the parasitic admittance between the drain of M_1 and the silicon substrate. From Fig. 7, the output drain current i_{D2} can be given by

$$i_{D2} = \frac{g_{m2}}{sC_{in2}} \frac{R_D \| Y_{sub1}^{-1}}{(R_D \| Y_{sub1}^{-1}) + Z_{in}} i_{D1} \qquad (2)$$

where C_{in2} is the input capacitance of the 2nd-stage and Z_{in} as shown in Fig. 7. For $C_{in2} \cong C_{gs2}$ and at the frequency of resonance (ω_0), where $Z_{in} << (R_D \| Y_{sub1}^{-1})$, eq. (2) can be approximated as

$$i_{D2} \cong \frac{\omega_T}{\omega_0} i_{D1} \qquad (3)$$

In eq. (3) ω_T represents the cutoff frequency of M_2. From the above discussions, the 1st-stage of the proposed amplifier is in a situation similar to the 1st-stage of cascode amplifier, no Miller effect. However, as can be seen from eq. (3), there exists a current gain from the output of M_1 to the output of M_2, while there was current loss with the cascode topology as seen in eq. (1). In the newly proposed topology, the noise contribution of R_D is negligible due to the small Z_{in}. In conclusion, the proposed topology allows the implementation of low noise and very high gain amplifier at low power.

IV. Simulation Results

Table 1. The simulated results of three different LNA topology. Simulations are done at 2.4 GHz. For all three cases, the supply voltages and currents are 2 V and 2.5 mA, respectively.

Topologies	Power Gain[dB]	NF [dB]
Cascode	12.6	1.36
Current sharing two-stage cascade	15.6	1.42
Current sharing two-stage cascade with series inter-stage resonance	21.0	1.24

Three different topologies of LNAs, circuits shown in Fig. 1, 2, and 6, are designed for 2.4 GHz applications for the supply voltages and currents of 2 V and 2.5 mA. For all three cases the input side are matched to 50 Ω through the series addition of inductors at the source and gate node of transistor M_1 [1]. An *R-L-C* resonance circuits are used for Z_L for all three circuits. A 0.35 μm CMOS technology is used for the simulation and the RF

transistor models are used, and the on-chip spiral inductor models are used for the inductors. Table 1 summarizes the simulation results. As can be seen from Table 1, the proposed topology demonstrates best performance in gain and noise figure.

V. Conclusion

A new high gain and low noise amplifier topology is proposed. The proposed architecture is composed of two common-source amplifier stages sharing the same bias current. The interstage between the 1st and 2nd amplifier is combined through a series inter-stage resonance. The performance of the proposed topology is compared with prior high-gain topologies through analysis and simulation. The simulation result of proposed architecture demonstrates, with a 0.35 μm CMOS technology, the highest gain of 21 dB at 2.4 GHz while drawing 2.5 mA from a 2 V supply.

Refercences

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