A Dual-Band Receiver Architecture for PCS and IMT-2000

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Abstract

A dual-band receiver architecture for PCS and IMT-2000 is described. The proposed architecture is suitable for high-level integration and minimizes the hardware duplicity by adopting a single wide-band high-performance image-rejection mixer in conjunction with a frequency doubler. Along with the architectural aspects of the dual-band receiver, the circuit implementation details are described.

Introduction

Generations of wireless communication services expanding to the higher frequency band, the demand for the multi-band RF transceivers are ever increasing. The request for the backward compatibility as well as the prevalence of software defined radio concept [1] is the further cause of the instigation for the multi-band transceivers. Amid exuberant discussions about the software-defined radio, few were able to propose practical multi-band transceiver architecture. The challenge is to minimize the hardware duplicity. Previously reported dual-band architectures employ dual-hardware for all the RF blocks [2, 3]. This work presents a novel dual-band receiver architecture for PCS and IMT-2000 that unifies the RF mixer.

Dual-Band Architecture

Figure 1 shows the block diagram of the proposed receiver architecture. In Fig. 1, it is assumed that the PCS and IMT-2000 system occupies 1.84 ~ 1.87 GHz (30 MHz) and 2.11 ~ 2.17 GHz (60 MHz) bands, respectively. The IF frequency is assumed to be the same as what the current PCS system uses (220 MHz). As can be seen in Fig. 1, separate low noise amplifiers (LNA) are allocated for PCS and IMT-2000 frequency bands excepts that the outputs of the LNAs are combined into one and directly cascaded with the following down-conversion mixer. Since the LNAs are directly connected to the mixer on the silicon chip, impedance matching is not required. The dual LNAs are adopted considering the two duplexers needed as well as the isolations needed between the two services. Only one of the LNA is expected to operate at each time while the other LNA is in power-down mode. The LNA has to provide high amount of isolation in its power-down mode.

From Fig. 1, the overall RF input bandwidth for the image-rejection mixer is 330 MHz (= 2.17 GHz – 1.84 GHz). The corresponding overall LO (local oscillator) frequency ranges are 200 MHz, 1.89 ~ 1.95 GHz for IMT-2000 and 2.06 ~ 2.09 GHz for PCS, respectively. The close proximity of the PCS and IMT-2000 frequency bands and

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the careful selection of the LO frequencies allows a single down-conversion mixer feasible.

Figure 2 shows the block diagram of the wide-band and high performance (image-rejection wise), image-rejection mixer. The proposed mixer architecture is similar to what is reported in [4] but more complete. Figure 2 also shows the image rejection process. Analysis of the image rejection mixer shows that the proposed architecture inherently compensates the gain and phase mismatches, leading to ideally infinite image-rejection ratio [5]. Note that the proposed image-rejection mixer does not require any low-pass filters like the conventional Harley and Weaver architectures [6]. This means that the proposed image-rejection mixer can be applied to higher microwave frequencies where the active low-pass filters are not technically feasible.

Figure 3 shows an actual implementation of the four mixers and the output summing/ subtraction circuits of the image-rejection mixer. As can be seen in Fig. 3, the output summing/subtraction circuits are easily realized by the proper combination of the mixer output currents.

To secure accurate quadrature signals, three- and two-stage poly-phase filters are used for RF and LO signals, respectively. The operating frequency of the each poly-phase filters is distributed over the frequency of interest. Even though the IF frequency is fixed, a two-stage poly-phase filter is used on the IF signal to minimize the effect of process variation. Based on 0.25 micron CMOS process, the simulation result of the complete image-rejection mixer showed more than 40 dB image rejection over the frequency bands of interest.

As can be seen from Fig. 1, there is a partial frequency overlap between the mixer LO signal and the IMT-2000 transmit signal. This situation could lead to a potential interference problem. Moreover, in any case, having LO signal near the transmit frequency band is not recommendable. To avoid this situation, a frequency doubler block is added. As shown in Fig. 1, the externally injected LO signal frequencies (near 1 GHz) are spaced far enough from any of the RF and IF signals. Figure 4 shows the circuit schematics of the frequency doubler along with the active balun for single-to-differential conversion. A BJT version of the same frequency doubler circuit has been reported previously [7]. The reported BJT version had 10 dB rejection on fundamental frequency up to 14 GHz. The simulation result of the MOSFET version, shown in Fig. 4, demonstrated more than 40 dB rejection at RF frequencies. The active balun is added to be able to drive the poly-phase filter differentially. From the simulation, the active balun provided phase and amplitude mismatches less than 1 degree and 0.6 dB, respectively, up to 2 GHz.

Conclusions

A novel dual-band architecture for PCS and IMT-2000 is presented. The proposed architecture is composed of dual LNAs, a single image-rejection mixer, and a frequency doubler. This architecture is suitable for single-chip dual-band receiver integration and reduced hardware duplicity more than previous works. The image-rejection architecture can be applied to higher microwave frequency applications also.

Simulations show more than 40 dB image rejection over the frequency band of interest, and excellent frequency doubler and balun performances are predicted. The proposed receiver circuit is in the phase of layout.

Acknowledgement

This work is supported by the Ministry of Information and Communications, Korea, Grant # 99-S-016

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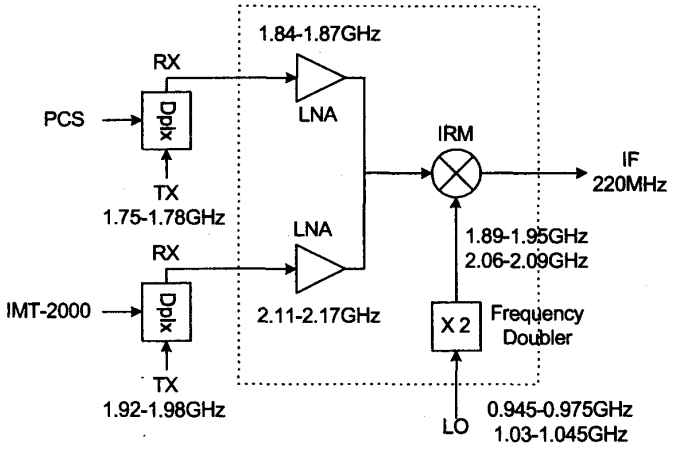

Figure 1: The dual-band receiver architecture.

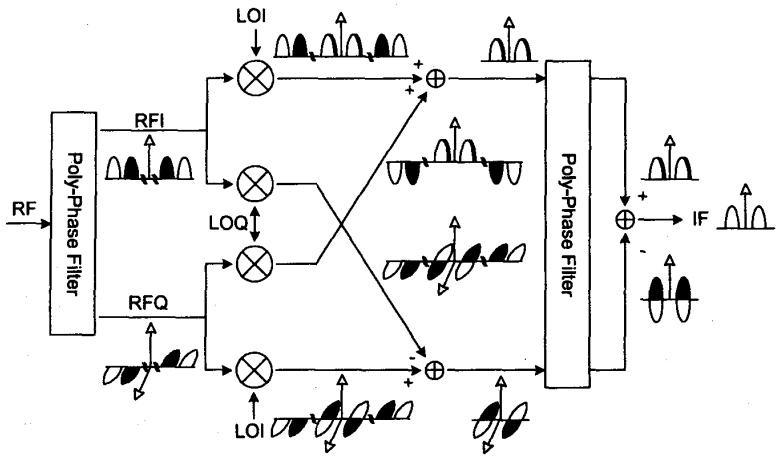

Figure 2: The image-rejection mixer architecture.

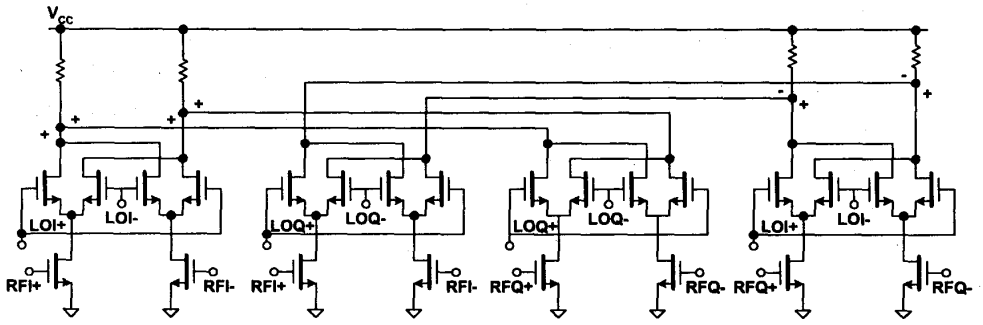

Figure 3: The core part of the image-rejection mixer schematics.

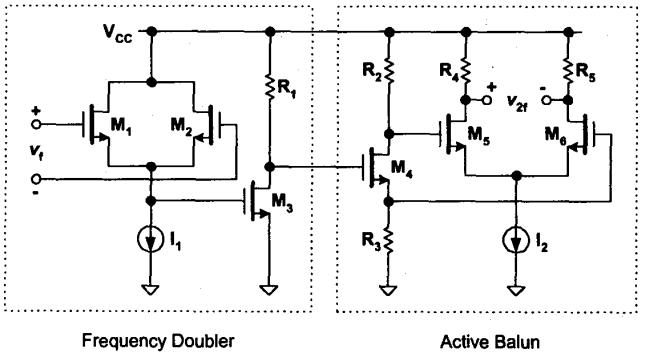

Figure 4: The frequency doubler and active balun schematics