LOW FREQUENCY NOISE IN SIMOX MOSFET'S

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An extensive study has been made of low frequency noise in MOSFET's built in a variety of SIMOX processes. Most of the devices studied showed very high noise levels dominated by generation-recombination noise. Among the devices measured were NMOS and PMOS FET's with superficial Si layers ranging in thickness from 0.3 μm (no epi layer) to 2.5 μm (with epi). SIMOX implant doses ranged from 1.4×10^{18} cm^{-2} to 1.8×10^{18} cm^{-2}. Anneal times varied from 3 to 16 hours and anneal temperatures varied from 1150 °C to 1275 °C. Work is in progress to characterize devices annealed at higher temperatures.

In all cases, the devices were measured in saturation with fixed drain current. Noise power was generally found to vary in inverse proportion to the square of channel length and in direct proportion to a power of the drain current which varied between one and two. The back surface condition was varied from accumulation to inversion. The shape and level of the measured noise spectra varied strongly as a function of back or front surface potential; in most devices, the noise rose sharply (more than 10dB) as the back surface entered strong inversion and then dropped gradually for increased back channel drive. Minimum noise was typically observed for depleted back channels. Even these minimum noise levels were much higher than the typical noise of high-quality bulk MOSFET's. In a typical measurement on an NMOS FET (W/L = $50\mu m/2\mu m$, Si film thickness = 1.3 μm and Id = 100 μA) the minimum noise was found with the back gate potential near zero volts. At 1 kHz the spot noise was 34×10^{-21} A^2/Hz, corresponding to a corner frequency (where the noise projected at 1/f would equal the thermal noise) of 6.2 MHz. Good bulk MOSFET's have corner frequencies below 1 kHz. These levels of noise are high enough to cause serious problems for analog applications and might be troublesome in some digital applications as well.

The measured spectra lead to the following conclusions: (1) classic 1/f noise, generally attributed to random fluctuations of mobility, was not observed, and was probably masked by other processes; (2) over the measured frequency range (10 Hz to 10 kHz) the noise was dominated by fluctuations in the channel carrier concentration due to trapping; (3) from the shape of the specta and their strong dependence on surface potential, the traps are not located in either the top or bottom oxide layers (as in the McWhorter model, which predicts a pure 1/f spectrum with a smooth surface potential dependence), but in the bulk; (4) a few distinct trap levels, each with an associated time constant, interact most strongly with channel carriers when the Fermi level aligns with the trap level, explaining the strong dependence on surface potential. It appears likely that these traps are associated with the dislocations typically generated in the SIMOX process.

Decomposing measured spectra into individual trap contributions is very time-consuming; since the results are strongly dependendent on the (still evolving) fabrication process, a detailed low-frequency noise modeling effort seems impractical at this time. Work is in progress, however, to demonstrate how improved processing and proper choice of operating conditions can reduce noise levels.

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