A 6-b 1-GS/s Adaptive Input Dynamic Range ADC Using Double Reference-Level for Radar System

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Abstract

This paper presents a 6-b 1-GS/s adaptive input dynamic range using double reference level for a radar system. For adopting the input dynamic range, the 1-b sub ADC generates an output bit depending on an input signal voltage, which selects one between double reference-level ladders of the 6-b core ADC to determine the input dynamic range. By the adaptive input dynamic range, the ADC can reduce the quantization error for small-amplitude input signal while providing rail-to-rail input dynamic range for wide-power range of radar echo signal. Simulation results show that the proposed ADC achieves 7.01-bits of ENOB for a Nyquist 1.2 V_{pp} differential input signal while consuming 134.1 mW of total average power from a 1.5V supply.

Keywords: A/D converter, adaptive input range, extended resolution, flash ADC, radar system, rail-to-rail.

1. Introduction

In recent years, interest in automotive-radar sensors has been increased for drivers' safety and convenience. A radar echo signal has wide-power range since location and radar cross section (RCS) of targets are unknown. Thus, an ADC for radar is required to have wide input dynamic range to digitalize an input in wide-power range. However, a least significant bit (LSB), that is a unit reference voltage step, becomes larger when an input dynamic range is extended with same resolution of ADC. An ADC with large LSB can cause loss of amplitude information of an analog input signal. In many radar systems, time-domain information of echo signal is used to detect location of target and the number of targets. Therefore, a wide input dynamic range ADC that can reduce the loss of time-domain information of an input is required for radar system. This paper reports proposed adaptive input dynamic range ADC using double reference levels to reduce the loss of amplitude information of radar echo signal.

2. Architecture

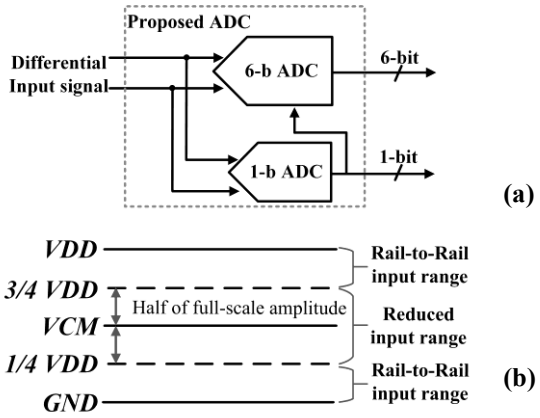

Figure 1. (a) The block diagram of the proposed ADC and (b) the adaptive input dynamic range depending on input signal voltage.

Figure. 1 shows the architecture of the proposed adaptive input dynamic range ADC. As shown in Figure. 1(a), the ADC consists of a 1-b sub ADC for deciding input dynamic range and a 6-b core ADC for digitalizing radar echo signal. As shown in Figure. 1(b), the proposed ADC provides rail-to-rail input dynamic range for the wide power range of input. When small input signal is entered, thus wide input dynamic range is not required, the ADC adopts the reduced input dynamic range for less quantization error.

The differential input signals are connected to the input nodes of two ADCs and the 1-b sub ADC compares an amplitude of the differential input signals to half of full-scale amplitude. Then, this ADC generates one bit for the 6-b core ADC to adopt the input dynamic range. When the input amplitude is larger than half of full-scale amplitude, one bit become high then the core ADC has rail-to-rail input dynamic range. While the input amplitude is smaller than half of full-scale amplitude, one bit become low to reduce the input dynamic range of core ADC by half of rail-to-rail. Thus LSB of ADC is also reduced by half to

reduce loss of amplitude information. Due to this operation, for small-amplitude input signal, the ADC has same value of LSB as one of 7-bit resolution in rail-to-rail input dynamic range.

3. Design of the proposed ADC

The 6-b core ADC is adopted a flash architecture for fast speed [1] and the comparator consists two stage of a preamplifier and a dynamic latch. The preamplifier is a switched-capacitor type for rail-to-rail operation [2]. The 1-b sub ADC consists two comparators with reference voltages that are 3/4 VDD and 1/4 VDD and a digital NAND gate. Two outputs of comparators are entered the NAND gate and the NAND generates final output of the sub ADC.

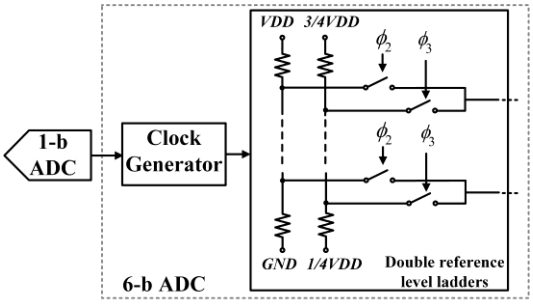

Figure 2. The reference generator of the proposed ADC.

Figure. 2 shows double reference-level ladders of the 6-b core ADC for adaptive input dynamic range. As shown in Figure. 2, the ADC utilizes two reference ladders connected to the input node of the switched-capacitor preamplifier for generating two input dynamic ranges. The clock generator provides switch signals for the reference generator by the output bit of the sub ADC.

A switched-capacitor preamplifier has two-phase operation of sample mode and hold mode. In sample mode, the input nodes of the preamplifier are connected to the analog input signal. While, in hold mode, the input nodes are connected to the reference ladder thorough the switch of ϕ_2 or ϕ_3. As shown in Figure.1 (b), when the input voltage of the ADC is larger than 3/4 *VDD* and smaller than 1/4 *VDD*, the clock generator provides *VDD* for ϕ_2 and *GND* for ϕ_3 to adopt rail-to-rail reference voltage. On the other hand, when the input voltage is smaller than 3/4 *VDD* and larger than 1/4 *VDD*, the clock generator provides *GND* for ϕ_2 and *VDD* for ϕ_3 to adopt the reduced input dynamic range from 1/4 *VDD* to 3/4 *VDD*.

4. Simulation results

The proposed adaptive input dynamic range ADC is designed in a 0.13-μm CMOS process with supply voltage of 1.5 V. The simulation results are obtained at 1-GS/s.

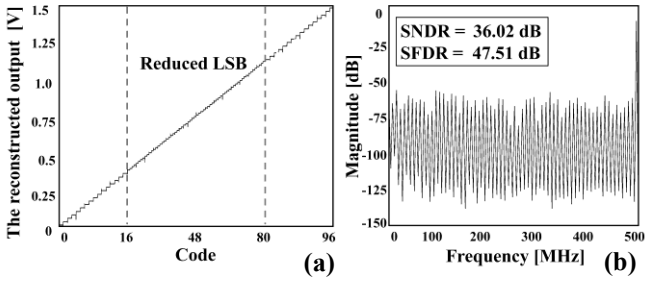

Figure 3. Simulation results. (a) rail-to-rail ramp input test and (b) FFT spectrum for a Nyquist 1.2V_{pp} input.

Figure. 3(a) shows the results for a rail-to-rail ramp input. As shown in Fig. 3(a), the total code of ADC is increased from 64 of 6-b resolution due to the reduced LSB for small-amplitude input signal. Figure. 3(b) shows the FFT spectrums of the proposed ADC for a Nyquist 1.2 V_{pp} differential input signal. The obtained SNDR/SFDR from the proposed ADC and the 6-b rail-to-rail ADC, without adaptive input range, are 36.02 dB/47.51 dB and 29.75 dB/40.97 dB, respectively. The peak SNDR and ENOB, calculated from the obtained SNDR, are 43.98 dB/7.01 bits and 37.71 dB/5.97 bit, respectively. Total average power consumption is 134.1 mW from 1.5 V supply voltage except clock buffers. The simulation results prove the proposed ADC performs rail-to-rail operation while increasing 1-b resolution for a small-amplitude input signal.

5. Conclusion

This paper presents a proposed 6-b 1-GS/s adaptive input dynamic range ADC using double reference-level for radar system. The ADC adopts the 1-b sub ADC and two reference voltage ladders of the 6-b core ADC for changing the input dynamic range depending on an input amplitude. The ADC is suitable for a radar system due to that the ADC can cover the wide power range of radar echo signal and reduces the quantization error for small-amplitude input signal to save envelop information with less loss.

Acknowledgment

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References

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