A 5.2-GHz LNA in 0.35-μm CMOS Utilizing Inter-Stage Series Resonance and Optimizing the Substrate Resistance

Choong-Yul Cha and Sang-Gug Lee

***Abstract*—A current-reused two-stage low-noise amplifier (LNA) topology is proposed, which adopts a series inter-stage resonance and optimized substrate resistance of individual transistors. The characteristics of the series inter-stage resonance in gain enhancement are analyzed and compared with other alternatives. The contradicting effects of substrate resistance on common-source and common-gate amplifiers are analyzed and proposed guidelines for high-gain operation. The LNA is implemented based on a 0.35-μm CMOS technology for 5.2-GHz wireless LAN applications. Measurements show 19.3 dB of power gain, 2.45 dB of noise figure, and 13.2 dBm of output IP3, respectively, for the dc power supply of 8 mA and 3.3 V.**

***Index Terms*—CMOS, low-noise amplifier (LNA), RF, series inter-stage resonance, substrate resistance effect, wireless LAN.**

I. Introduction

WIRELESS communications at gigahertz frequencies are a huge market that drives the semiconductor technology toward low-cost solutions. CMOS technology is an attractive solution due to the low cost, high-level integration, and even high performance in terms of cutoff frequency [1], [2]. Many existing wireless systems operate around 2-GHz frequency bands with data rates below 2 Mb/s. By the pressing demand for wireless multimedia services, the operational frequencies are forced to move up to meet the higher data rate. WLANs operating in 5-GHz frequency band is expected to be a widely used system for the next-generation multimedia wireless applications [3]. For high-frequency design, more advanced technology will certainly provide better performance. However, with consumer application products, the production cost is one of the most important parts of the technology selection, meaning that, for circuit designers, obtaining better performance with less advanced technology is the most challenging responsibility. The major problems of CMOS technology at high frequencies are the low transconductance and signal loss through the conducting silicon substrate. Typically, high-gain and low-noise implementation of low-noise amplifiers (LNAs) involves high power dissipation, which is not a desirable option with portable wireless systems. In high-frequency LNAs, the signal loss through the drain/source to substrate parasitics can severely degrade the noise figure (NF) and power gain [4]–[7].

This brief proposes a novel low-power, high-gain, and low-noise amplifier by optimizing the circuit topology and the transistor structure. In Section II, the series inter-stage resonance technique in a two-stage amplifier is analyzed and compared with other high-gain amplifier topologies. In Section III, the effect of substrate resistance on the high-frequency characteristics of the common-source and common-base transistors are investigated and verified. Section IV presents the proposed 5.2-GHz LNA topology and measurement results. Section V concludes the brief.

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II. High-Gain Amplifier Topologies—Series Inter-Stage Resonated Amplifier

Many high-gain amplifier topologies have been proposed as a way to satisfy the requirement for low power dissipation as well as high performance. The cascode and inverter [8] are some of the widely used high-gain amplifier topologies. However, with the cascode amplifier, it is well known that the high-frequency noise and gain can be significantly degraded by the substrate parasitics at the drain node of the common-source stage [9], [11]. Similarly, the high-frequency gain of the inverter can also be significantly degraded by the substrate parasitics. Because, with reactive parallel resonance or reactive matching at the output node, the effect of low-quality-factor substrate impedance can degrade the resonated peak impedance significantly, leading to gain degradation.

Fig. 1(a) shows the proposed current-reused high-gain two-stage amplifier topology. In Fig. 1(a), L_d and Z_L are the loads for each common-source amplifier, C_1 is the coupling capacitor, C_2 is the bypass capacitor, and R_g is the bias resistor. The proposed amplifier is the current-reused two-stage common-source amplifier with capacitive inter-stage coupling [10] except the extra inductor L_g. In Fig. 1(a), the value of L_g is adjusted for the series resonance with the input capacitance of the second stage. The simple two-stage cascaded common-source amplifier can suffer from gain degradation, as in the case of the inverter, by the low-quality-factor substrate impedances at the drain nodes of each amplifier. In addition, the considerable voltage gain at the drain nodes of the first stage can lead to stability problems. The series inter-stage resonated topology shown in Fig. 1(a) is less susceptible to the substrate effect and provides high gain with fewer stability problems, as described in the following.

Fig. 1(b) shows the small-signal equivalent circuit for the portion of the circuit enclosed by the dashed box in Fig. 1(a) in order to estimate the current gain from the drain of M_1 to that of M_2. In Fig. 1(b), $Z_{\rm sub}$ represents the parasitic impedance from the drain node of transistor M_1 to ground through the silicon substrate. As a simple model, $Z_{\rm sub}$ is composed of the M_1's drain junction capacitance $C_{\rm jd}$ in series with the effective substrate resistance $R_{\rm sub}$. R_s is the parasitic series resistance of L_g. $C_{\rm in2}$ is the equivalent input capacitance of the second stage, which is

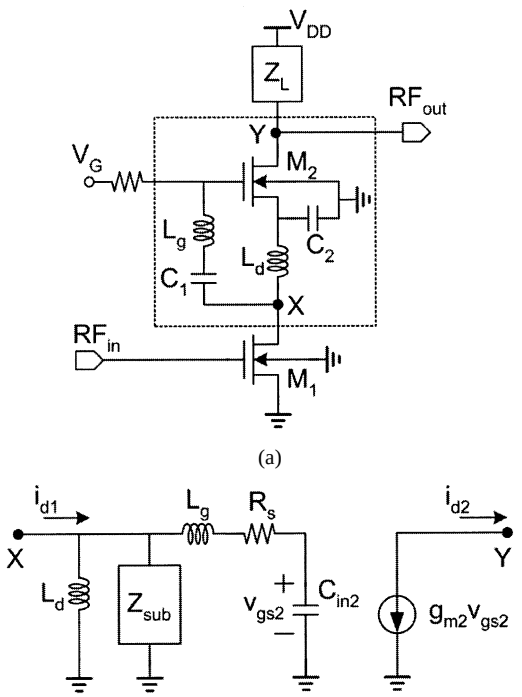

Fig. 1. (a) Current-reused two-stage cascade amplifier with series inter-stage resonance. (b) Small-signal equivalent representation of the circuit from node X to Y.

the sum of the gate–source capacitance $C_{\rm gs2}$ and the Miller capacitance of M_2. The $V_{\rm gs2}$ and g_{m2} represent the gate-to-source voltage and the transconductance of M_2, respectively.

The current-amplifying characteristic of the series inter-stage resonated amplifier can be understood by analyzing the circuit shown in Fig. 1(b). From Fig. 1(b), the current gain i_{d2}/i_{d1} can be expressed as

$$\frac{i_{d2}}{i_{d1}} = \frac{g_{m2}}{sC_{\rm in2}} \frac{sL_d \,||Z_{\rm sub}}{sL_d \,||Z_{\rm sub} + sL_g + R_s + 1/sC_{\rm in}}. \quad (1)$$

From (1), when L_g resonates with $C_{\rm in2}$ and, compared with R_s, if $sL_d \,||Z_{\rm sub}$ provides sufficiently high impedance, then $i_{d2}/i_{d1} \cong g_{m2}/sC_{\rm in2}$, regardless of the quality factor Q of the inductor L_g. Furthermore, if $C_{\rm in2} \cong C_{\rm gs2}$ (for example, when the second stage is a cascode amplifier as in the case of the LNA topology described in Section IV), (1) can be approximated as

$$\frac{i_{d2}}{i_{d1}} \cong \frac{g_{m2}}{sC_{\rm gs2}} \cong \frac{\omega_T}{\omega} \quad (2)$$

where ω_T represents the cutoff frequency of M_2 and ω the frequency of operation. Note that (2) is valid regardless of the size of transistor M_2, meaning that the size of M_2 can be small for higher cutoff frequency as well as higher linearity. As can be seen from (2), the proposed series resonance can provide a significant current gain from the drain of M_1 to that of M_2, leading to high overall power gain.

The significance of the newly proposed amplifier is the low impedance, and therefore the voltage gain as well, established at the drain of M_1 as in the case of the cascode amplifier through the series resonance of L_g and $C_{\rm in2}$. Therefore, the stability of the proposed amplifier is better than that of the simple two-stage cascaded common-source amplifier. Moreover, the low impedance established at the drain node of M_1 obviates the signal loss through $Z_{\rm sub}$, as in the other topologies discussed above.

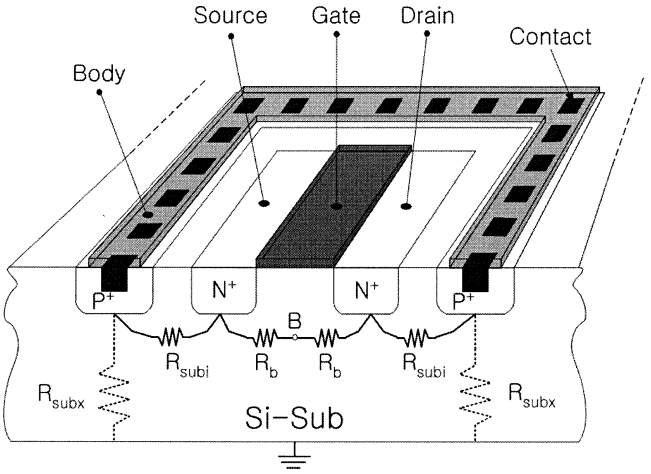

Fig. 2. Cross section of an RF CMOS transistor showing the parasitic resistances.

III. Optimizing Small-Signal Substrate Resistance in RF CMOS Amplifier

In CMOS technology, as discussed above, the substrate parasitic impedance can affect the high-frequency performance of the circuit as well as the transistor itself. Fig. 2 shows the cross-section of a RF CMOS transistor with equivalent parasitic substrate resistances. In Fig. 2, R_b, $R_{\rm subi}$, and $R_{\rm subx}$ represent the effective body, intrinsic substrate, and the extrinsic substrate resistances, respectively [12]–[14]. Fig. 3 shows a cascode amplifier with parasitic resistances and capacitances relevant to the discussions in this section. In Fig. 3, $C_{\rm jd}$ and $C_{\rm js}$, are the drain-to-substrate and source-to-substrate junction capacitances, respectively, and $C_{\rm gs}$ is the gate-to-source capacitance. With transistor M_1 in Fig. 3, the body terminal is assumed to be connected to external ground, while with M_2, the body terminal is assumed to have the option of either being externally grounded or left open (note the switch). With the open switch, the body terminal of M_2 is connected to ground through $R_{\rm subx}$.

In Fig. 3, with common-source transistor M_1, the high substrate resistance lowers the output resistance and the transconductance of the transistor. The well-known method to minimize these substrate effects is to reduce the substrate resistance $R_{\rm subi}$ by placing substrate contacts surrounding the MOSFETs and connecting the body terminal to the external ground such that $R_{\rm subx}$ becomes zero [4], [5].

However, with the common-gate stage in Fig. 3, the situation can be different. Typically, R_b is small [14] and $C_{\rm jd}(=C_{\rm js})$ is about 30%∼50% of $C_{\rm gs}$. Note that in Fig. 3, neglecting R_b, the components $C_{\rm jd2}$, $C_{\rm js2}$, $C_{\rm gs2}$, and M_2 constitute an oscillator topology with inductive termination at the output [15]. The combination of $C_{\rm jd2}$, $C_{\rm js2}$, $C_{\rm gs2}$, and M_2 provide negative resistance at the drain node of M_2. This means the increase in the Q of the output impedance, which leads to increase in the tuned output impedance. Note that the larger the value of $R_{\rm sub}$, the lower the frequency where the positive feedback kicks in. Therefore, at high frequencies, the maximum available gain of

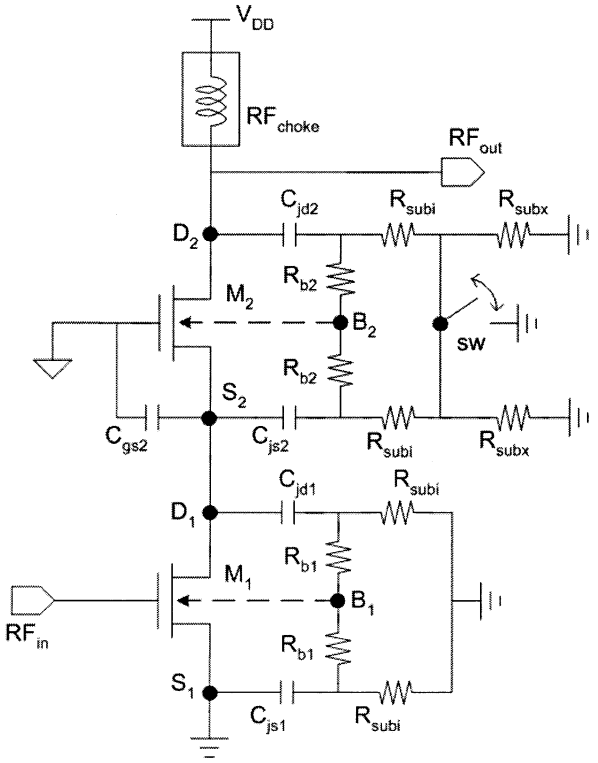

Fig. 3. Cascode amplifier with parasitic capacitances and resistances.

the cascode amplifier with open switch can be higher than that of the shorted case. Another perspective of the given situation is that the maximum available gain of the cascode amplifier can be improved significantly by adding an additional capacitor between the drain–source terminals.

IV. LNA Design and Measurement Results

Fig. 4 shows the schematic of the proposed 5.2-GHz LNA. As can be seen from Fig. 4, the proposed LNA is a current-reused two-stage amplifier with series inter-stage resonance. The first stage is common source and the second stage is the cascode topology. In Fig. 4, L_{g1} and L_o represent external inductors and C_o the external capacitor. L_{g1} is used for the gain and noise matching [16], and L_o and C_o for the output gain matching. L_{s1} and L_{s2} are the high-Q on-chip inductors. L_{s1} is used for gain, linearity, and noise-matching purposes. L_d is the load for the first stage, and L_{g2} is the series inter-stage resonance inductor. The capacitor C_1 is for the coupling and C_2 and C_3 are for the bypassing. The resistors R_{g1} and R_{g2} are for the dc biasing. In Fig. 4, resistor R_{bx} is an additional resistor which is connected between the body node of M_3 and the external ground to increase the substrate resistance of the corresponding transistor. As discussed previously, R_{bx} helps to improve the high-frequency performance of the second stage, which is the cascode amplifier. The cascode second stage helps improve the reverse isolation of the overall amplifier.

Note that the degeneration inductor L_{s2} introduces a small amount of real impedance seen from the drain node of the first-stage amplifier, but the advantage of the series inter-stage resonance, which is described in Section II, is little disturbed. From the circuit simulation, the insertion of L_{s2} helped to improve the

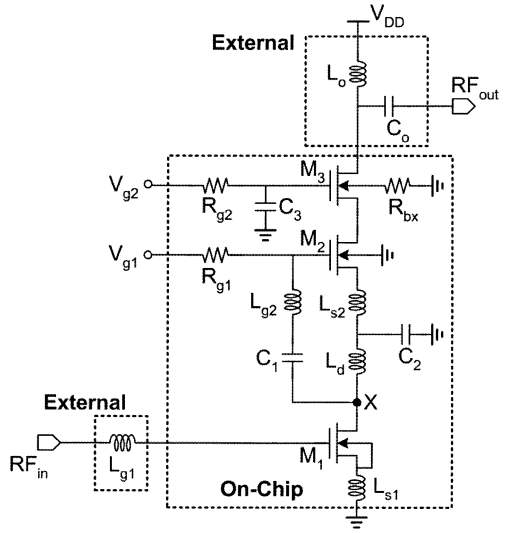

Fig. 4. Proposed 5.2-GHz LNA schematic.

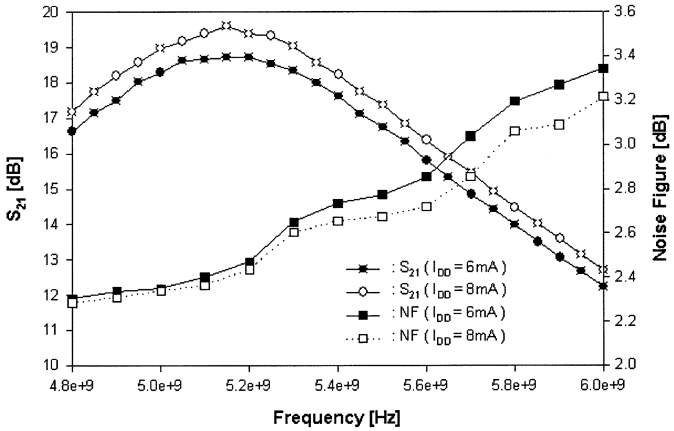

Fig. 5. Measured LNA power gain and NF as a function of frequency.

NF of the overall amplifier, which could be result of the degeneration effect L_{s2} on the noise sources of M_2.

The circuit shown in Fig. 4 is optimized for 5.2-GHz operation and fabricated based on a 0.35-μm epi-CMOS technology. Fig. 5 shows the power gain and NF of the proposed amplifier for two different supply currents, $I_{DD} = 6$ mA and $I_{DD} = 8$ mA, and the supply voltage is 3.3 V. As shown in Fig. 5, the fabricated LNA has peak gain of 19.3 dB and NF of 2.45 dB at 5.2 GHz for the supply current of 8 mA. The measured output IP3 is 13.2 dBm [17]. Table I summarizes the measurement results and compares them with previous work. As can be seen from Table I, in spite of the inferior technology used, the proposed LNA shows an impressive performance that is better than or comparable to that of the previous work. Note that from Fig. 4, had the L_{s1} been replaced with an external high-Q inductor, the NF of the proposed LNA could have approached 2 dB. Fig. 6 shows the microphotograph of the fabricated LNA.

V. Conclusion

The design of a high-performance LNA at high frequencies based on CMOS technology is challenged by many issues, such as low transconductance, signal loss through the silicon

TABLE I
COMPARISON OF 5-GHz RANGE CMOS LNA PERFORMANCES: PUBLISHED AND THIS WORK

Reference	[9]	[18]	[19]	[20]	This Work
Frequency [GHz]	5.2	5.8	5.25	5.2	5.2
Technology [μm]	0.25	0.25	0.25	0.25	0.35
Supply [V]	2	2	3	1.5	3.3
Current [mA]	3.6	10	8	6	8
Power Gain [dB]	18*	10	14.4	17	19.3
Noise Figure [dB]	4.8	3	2.5	2.1	2.45
OIP3 [dB]	-	12	12.9	-	13.2

* Voltage gain

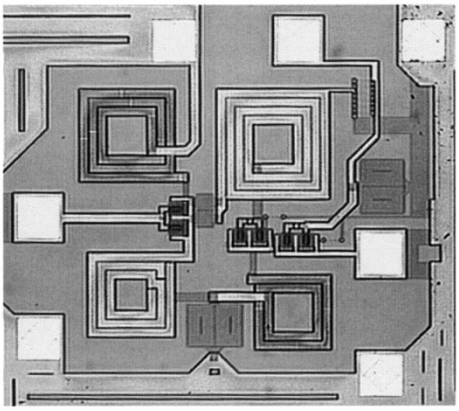

Fig. 6. Microphotograph of the fabricated 5.2-GHz LNA.

substrate, and high power dissipation. In this brief, a current-reused high-gain two-stage amplifier topology, utilizing the series inter-stage resonance, is proposed and compared with other reported topologies. It was explained and analyzed that, compared with the other reported topologies, the proposed amplifier topology can provide high gain without compromising stability and can minimize the signal loss from the drain to the silicon substrate.

The small-signal substrate resistance effect in RF CMOS cascode amplifiers has been investigated. For a common-source amplifier, the output feedthrough to the body node degrades the output resistance and transconductance considerably. Therefore, the substrate resistance should be minimized. However, in a cascode amplifier, the high-frequency maximum available gain can be improved when the substrate resistance of the common-gate transistor is maximized. The enhancement of the power gain is explained by identifying the resulting oscillator configuration of the common-gate topology at high frequencies.

A 5.2-GHz two-stage high-performance LNA is designed by combining the series inter-stage resonance and the substrate resistance optimization technique based on a 0.35-μm CMOS technology. The first stage of the amplifier is common source and the second stage is the cascode amplifier. Measurement results of the fabricated LNA at 5.2 GHz show power gain of 19.3 dB, NF of 2.45 dB, and IP3 of 13.2 dBm, with the dc power dissipation of 8 mA from a 3.3-V supply.

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