Analog Integr Circ Sig Process (2013) 74:661–665
DOI 10.1007/s10470-012-0016-4

MIXED SIGNAL LETTER

A high-precision spread spectrum clock generator based on a fractional-N phase locked loop

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Received: 23 September 2012 / Accepted: 11 December 2012 / Published online: 6 January 2013

Abstract A low jitter Spread Spectrum Clock Generator (SSCG) based on a fractional-N Phase Locked Loop (PLL) capable of generating various Electromagnetic Interference (EMI) reduction levels is proposed. A digital compensation filter is fully integrated in the design to prevent various triangular modulation profiles from being distorted by the prohibitively small PLL loop bandwidth. A simple but comprehensive logic design included in the digital filter provides independently controllable modulation frequency, f_m, and modulation ratio, δ_m within all modulation modes (up, down, center). The proposed SSCG is designed in a 0.18 μm CMOS standard cell library and operates at 72 MHz with f_m ranging from 58 to 112.5 kHz and δ_m ranging from 0.75 to 2 %.

Keywords EMI reduction · Frequency modulation · Triangular modulation profile · Spread spectrum clock generator · Fractional-N PLL

1 Introduction

The Spread Spectrum Clocking (SSC) technique diminishes EMI noise by modulating clock signals with a predefined modulation profile [1]. SSC can be accomplished by implementing a modulated PLL referred to as a SSCG. A SSCG based on fractional-N PLL provides EMI reduction by oversampling a predefined modulation profile through a ΔΣ modulator. Since the signal experiences low-pass filtering traveling from the feedback divider to the PLL output, the SSCG noise performance is enhanced due to the elimination of quantization noise generated by the ΔΣ modulator. However, the modulation profile also experiences this filtering action resulting in a distorted modulation waveform. Therefore, a trade-off between noise performance and modulation profile distortion limits the usage of fractional-N PLL based SSCGs in variable EMI reduction level applications. In addition, due to the monotonic behavior of up/down counter, an SSCG based on fractional-N PLL can operate in only upward or downward modulation mode.

Two reported techniques, two-point modulation technique and adaptive bandwidth technique, improve the performance of fractional-N PLL based SSCGs by intervening in the PLL loop [2, 3] which need an extra area and power for additional circuits. This letter provides another technique to improve SSCG performance without PLL loop intervention. A digital filter with compensation bandwidth generates a flat response from the feedback divider to PLL output. Hence, the small PLL bandwidth allows the triangular modulation signal to pass unaltered while attenuating the quantization noise of ΔΣ modulator.

2 Proposed circuit implementation

Figure 1 shows the architecture of the proposed SSCG and its signal paths. As shown in Fig. 1a, the proposed SSCG consisting of two main blocks: the fractional-N PLL and Triangular Profile Generator (TPG). In the TPG block, the control bits of the Multi Modulus Divider (MMD) determine the modulation frequency, f_m and the control bits of

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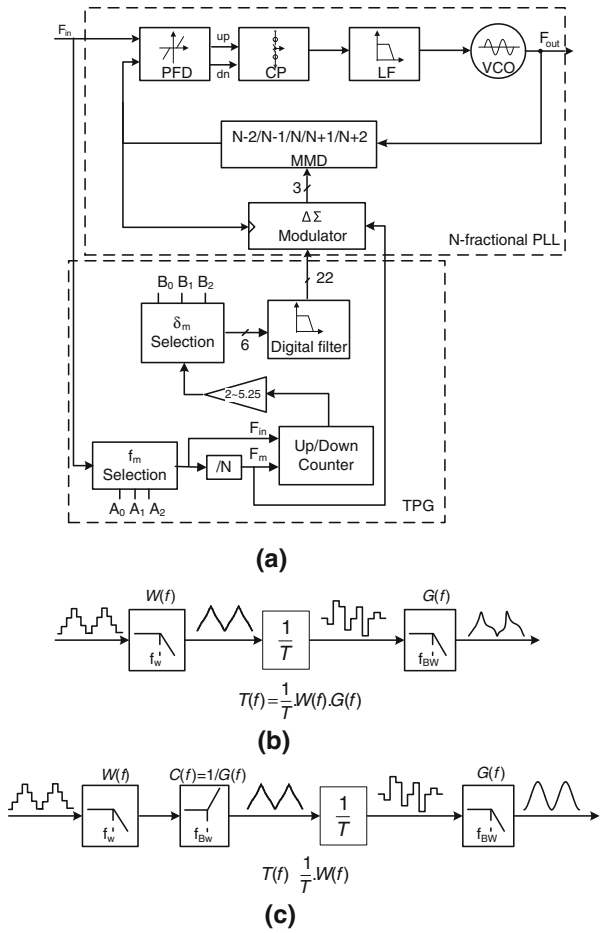

Fig. 1 The architecture of the proposed SSCG based on Fractional-N PLL and its signal paths

the channel selector decides the modulation ratio, δ_m. The 1/N divider cascaded with the up/down counter separates the control of f_m and δ_m. Because the reference clock of the PLL limits the counting clock of the up/down counter, the digitalized triangular profile at the output of the up/down counter has a non-smooth shape. The digitalized triangular modulation profile is a binary sequence in which each symbol (group of binary bit) contains the counted number. To sharpen the digitalized triangular profile, a digital finite impulse respond filter (FIR) interpolates a short bit sequence to long bit sequence, which is matched with the required input bit sequence of the ΔΣ modulator (in this case from 6 bits to 22 bits). Figure 1(b) illustrates the signal path from the up/dn counter output to PLL output in the linear model of the proposed SSCG. $W(f)$ and $G(f)$ are the transfer functions of the FIR filter and PLL low-pass filter, respectively, $1/T$ is transfer function of the ΔΣ modulator. As labeled in Fig. 1(b), the 3 dB bandwidths of $W(f)$ and $G(f)$ are defined as f_w and f_{BW}, respectively. When f_{BW} is optimized for low jitter performance, the triangular modulation profile is also distorted by $G(f)$. In order to mitigate the distortion on the triangular modulation profile while maintaining small f_{BW}, the compensation filter, $C(f) = 1/G(f)$, is cascaded with a digital FIR filter. Hence, the overall transfer function $T(f)$ shown in Fig. 1(c) depends only on the 3 dB bandwidth of the FIR filter leading to a flat frequency response from the input of FIR filter to the PLL output. The compensation filter is designed by convolving the time domain versions of $W(f)$ and $C(f)$. The resulting FIR coefficients are then implemented [4].

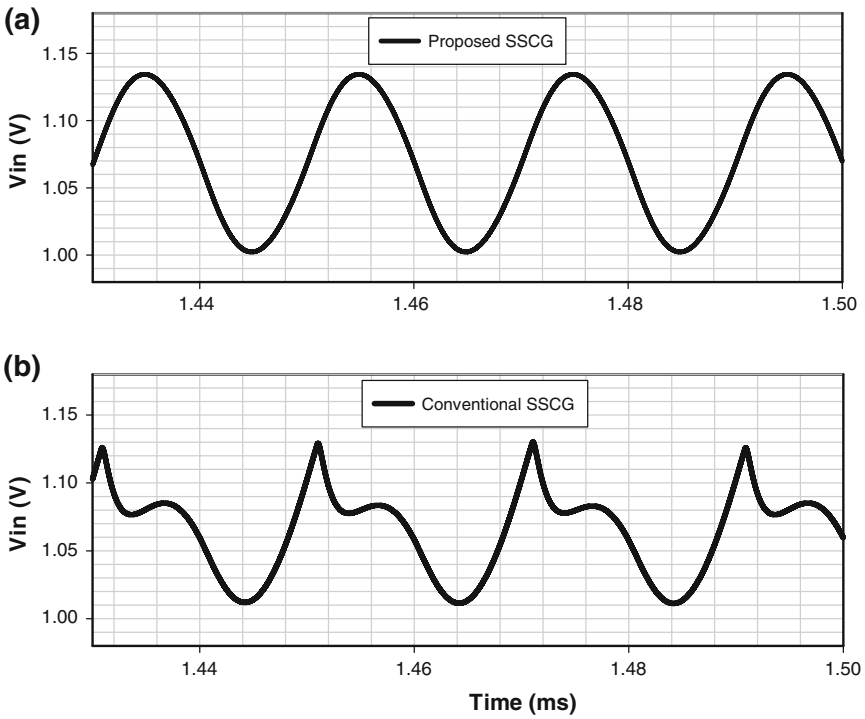

Fig. 2 Simulated control voltage of VCO block with/without compensation FIR filter

In the SSCG based on fractional-N PLL, upward or downward modulation mode is easily realized by setting the up/down counter increments to either upward or downward. However, due to the monotonic characteristic, the up/down counter statement does not support to the creation of center modulation mode which has upward modulation in the half of f_m's period and downward modulation in the other half or vice versa. In the proposed SSCG, center modulation mode is accomplished by toggling the MMD upward and downward consecutively. The output of the ΔΣ modulator is oriented to dither the MMD following (N − 1/N/N + 1/N + 2) division chain for upward modulation and (N + 1/N/N − 1/N − 2) division chain for downward modulation. The modulation frequency, f_m controls the transition from upward modulation to downward modulation and vice versa.

3 Measured results

An SSCG based on a fractional-N PLL is designed for LCD timing controller applications in 0.18 μm CMOS process. The proposed SSCG is simulated with $N = 30$, 120 kHz loop bandwidth, 20uA charge pump current, 100 MHz VCO gain at the typical operation frequency, 24 MHz. The TPG block generates the various independently controllable f_m (from 58 to 112.5 kHz) and δ_m (from 0.75 to 2 %) in upward, downward and center modulation modes. The triangular modulation profile is confined in the bandwidth of the 16-tap compensation digital FIR Gaussian filter. The coefficients of the compensation digital FIR Gaussian filter are calculated as

$$p_c[k] = \left(1 - \frac{1}{2.\pi.\xi.\omega_n.\sigma}.\left(\frac{k}{\sigma}\right) + \frac{1}{(2.\pi.\omega_n.\sigma)^2}.\left(-1 + \left(\frac{k}{\sigma}\right)^2\right)\right).p[k] \quad (1)$$

where ξ, ω_n are damping factor and natural frequency of PLL, $p[k]$, σ are coefficient and window width of the Gaussian FIR filter, N_{MMD} is the product of the digitalized triangular symbol rate and the sampling rate of the normal Gaussian FIR filter.

$$p[k] = \frac{1}{4}.\frac{1}{\sqrt{\pi}.\sigma}e^{-\left(\frac{k}{\sigma}\right)^2} \quad \sigma = \frac{1.178}{\pi}.N_{MMD}$$

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Figure 2 illustrates improvement of the modulation profile when the compensation FIR filter is applied. In Fig. 2(a), the proposed SSCG provides the triangular shape a modulation frequency of 50 kHz under a 50 kHz PLL loop bandwidth. Note that this performance cannot be obtained from a conventional SSCG as shown in Fig. 2(b). Figure 3 represents measurement results of the proposed

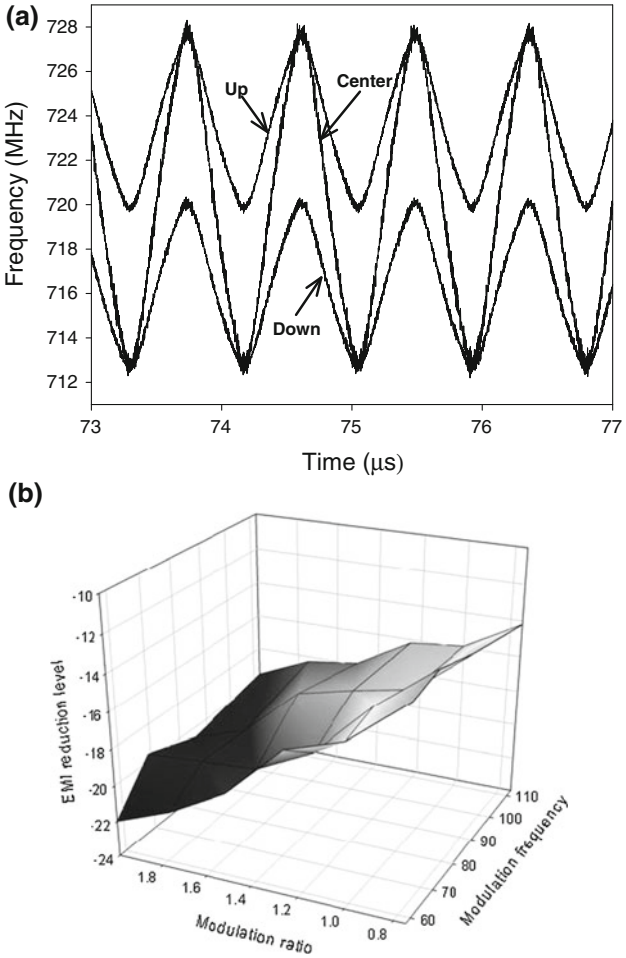

Fig. 3 Measured frequency deviation and EMI reduction of the proposed SSCG in up/down/center modes and corresponded jitter performance

SSCG. The achieved up/down/center modes are shown in Fig. 3(a) where the un-modulated frequency is 720 MHz, $f_m = 112.5$ kHz, $\delta_m = 1$ %. Although using the small loop bandwidth, the spread output contains some interference among the modulated frequency. It can be explained as the mismatch between the bandwidths of C(f) and G(f) caused by process variation. The largest time deviation on the frequency modulation profile is 0.03 μs for the modulated triangular waveform of 8.8 μs. Fig. 3(b) presents the EMI reduction amounts of every case of the independently controllable δ_m and f_m.

4 Conclusion

The proposed SSCG based on a fractional-N PLL generates a precise triangular modulation profile while also utilizing a noise-optimized PLL loop bandwidth, which provides efficient EMI reduction. The EMI reduction level is set

with the independently controllable variables f_m and δ_m over three modulation modes. The mismatch of the bandwidths of C(f) and G(f) is an object for further study.

Acknowledgments This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (No. R11-2005-029-06011-0).

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