The Effects of Carrier-Velocity Saturation on
High-Current BJT Output Resistance

Sang-Gug Lee and Robert M. Fox, Member, IEEE

Abstract—Modern Bipolar Junction Transistors (BJT's) tend
to operate with saturated carrier velocity in the collector space-
charge region. This paper presents a physical analysis of the
effects of velocity saturation on the output resistance of BJT's, especially for high current levels. Physical analyses show that
when the collector current density approaches a critical value,
the Early voltage can increase significantly due to carrier-ve-
locity saturation as the resulting base push-out partially offsets
base-width modulation. This effect is also demonstrated in sim-
ulations with PISCES and MMSPICE.

I. INTRODUCTION

ANALOG circuits such as operational amplifiers typi-
cally employ active loads to achieve high gains. The voltage gain and frequency response of such circuits thus depend on the transistors' small-signal output resistance. In most contemporary bipolar junction transistors (BJT’s), high electric fields occur in the collector junction space-
charge region due to the high epilayer doping or high re-
verse-bias voltage. These high fields tend to saturate the
free-electron drift velocity.

This work is a study of the effects of carrier-velocity
saturation, especially for high current levels, on the out-
put resistance characteristics of BJT's. Analytical expres-
sions for normalized BJT output resistance are derived for
an idealized structure as an aid to qualitative understand-
ing. MMSPICE [1] and PISCES-II [2] simulations are also
provided.

II. ANALYSIS

In a recent letter, Roulston [3] presented an improved
model for the Early voltage $V_A$ in n-p-n transistors with
very narrow base widths (less than 0.1 μm). Roulston
concluded that, due to carrier-velocity saturation, a sub-
stantial improvement in Early voltage is expected in nar-
row-base transistors compared to estimates based only on
the base doping level and width. Liou's [4] correction to
this work led to the following:

$$V_A = V_{B0}[1 + D_nF_c/v_sW_{B0}]$$

where $V_A = W_{B0}/(dW_{B0}/dV_{CE})$ is the conventional
expression for Early voltage (neglecting velocity satur-
ation), $D_n$ is the electron diffusion constant, $F_c$ is an
empirical factor to account for built-in fields and bandgap
narrowing in the base region, $v_s$ is the electron saturation
velocity, and $W_{B0}$ is the quasi-neutral base width. For a
silicon bipolar transistor with a base width of 0.04 μm,
$D_n = 17 \text{cm}^2/\text{V} \cdot \text{s}$, and $F_c = 1$, this model predicts $V_A = 1.4V_{B0}$.

With carrier-velocity saturation the carrier concen-
tration in the space-charge region (SCR) is proportional to
the collector current, and the positions of the SCR bound-
daries become functions of the carrier concentration.
Roulston’s model accounts only for a reduction in the con-
centration gradient due to the nonzero carrier concen-
tration at the SCR boundary. From (1), this leads to sig-
nificant increase in $V_A$ only for very narrow base widths.
As is well known, at the level of collector current where
the SCR boundaries become strong functions of $J_C$, base-
width modulation due to increments in $V_{CE}$ tends to be
offset by base push-out (Kirk effect) [5] as the resulting
increase in $n_c$ (and $J_c$) redistributes the electric fields in
the SCR. This offsetting mechanism, which was ne-
glected in [3], can lead to a much more significant in-
crease in small-signal output resistance at high currents,
even for ordinary base widths.

Following is a derivation of this increase in output re-
sistance as represented by the Early voltage. The Early
voltage [6] can be considered as the output resistance nor-
malized by the collector current: $V_A = r_oI_c - V_{CE}$ where
$r_o$ is the output resistance and $I_c$ is the collector current.

To simplify the mathematics, base and buried-layer dop-
ings are assumed constant, and the buried-layer doping is
assumed much greater than the base doping, which is
much greater than epit doping. The base terminal is as-
sumed to be driven by a constant voltage source (Fig. 1)
and the emitter junction SCR width is assumed to be in-
dependent of the collector current. The base-collector bias
voltage and the resulting electric field are assumed to be
high enough to saturate the electron velocity even near the
SCR edge. By this assumption we are excluding the pos-
sibility of ohmic quasi-saturation even though, in prac-
tice, the transistor might enter that operating region at low
$V_{CR}$. Ohmic quasi-saturation is excluded from this analy-
sis since it can be treated without considering velocity sat-
uration.

Manuscript received October 16, 1990; revised May 17, 1991. This work
was supported by the Semiconductor Research Corporation under Contract
89-SP-087. The review of this paper was arranged by Associate Editor
The authors are with the Department of Electrical Engineering, University
of Florida, Gainesville, FL 32611.
IEEE Log Number 9105346.
Fig. 1. One-dimensional n-p-n transistor structure.

Three operating conditions are considered: (Case 1) forward-active with part of the epitaxial layer quasi-neutral, (Case 2) forward-active with the epilayer entirely space-charged, and (Case 3) nonohmic quasi-saturation.

A. Case 1

Fig. 2(a) shows the electron concentration and electric field distribution for the case of forward-active operation with part of the epilayer quasi-neutral (QN). In the SCR, the current flows predominantly by drift. Assuming velocity saturation, the collector current density $J_c$ can be expressed as

$$J_c = qn_c v_c$$  \hspace{1cm} (2)$$

where $n_c$ is the electron concentration in the SCR required to support the current. Equation (2) and the equality of charges on both sides of the collector junction lead to the relation

$$x_B (qN_A + J_C/v_i) = x_C (qN_{EPI} - J_C/v_i)$$  \hspace{1cm} (3)$$

where $x_B$ is the penetration of the SCR into the base, $x_C$ is the penetration of the SCR into the epilayer, $N_{EPI}$ is the epilayer doping concentration, and $N_A$ is the base doping concentration. Poisson's equation can be solved in the collector junction SCR to yield the following expression:

$$V_{CB} + \phi_C = \frac{1}{2\epsilon_s} \left[ (qN_A + \frac{J_C}{v_i}) x_B^2 + \left( qN_{EPI} - \frac{J_C}{v_i} \right) x_C^2 \right]$$  \hspace{1cm} (4)$$

where $V_{CB}$ is the collector junction reverse bias, $\phi_C$ is the collector junction built-in potential, and $\epsilon_s$ is the semiconductor permittivity. In (4) the potential drop across the QN portion of the epilayer is neglected for simplicity. The effect of this approximation on output resistance will be discussed later. From (3) and (4), $x_B$ can be written in terms of $V_{CB}$ and $J_C$ as

$$x_B = \sqrt{\frac{2\epsilon_s N_{EPI} (V_{CB} + \phi_C)}{qN_A (N_{EPI} + N_A)}} \left( 1 - \frac{J_C}{J_{EPI}} \right)^{1/2} \left( 1 + \frac{J_C}{J_A} \right)^{1/2}$$  \hspace{1cm} (5)$$

where

$$x_{B0} = \frac{2\epsilon_s N_{EPI} (V_{CB} + \phi_C)}{qN_A (N_{EPI} + N_A)}$$  \hspace{1cm} (6)$$

Fig. 2. Typical electron concentration and electric field distribution for (a) forward-active operation with part of the epitaxial layer quasi-neutral; (b) forward-active operation with the epilayer entirely space-charged, $J_C < J_{EPI}$; (c) forward-active operation with the epilayer entirely space-charged, $J_C > J_{EPI}$; (d) nonohmic quasi-saturation operation.

$J_{EPI} = qN_{EPI} v_i$, and $J_A = qN_A v_i$. $x_{B0}$ is the SCR penetration into the base which would result from neglecting velocity saturation (i.e., using the depletion approximation).

Fig. 3 shows a plot of $x_B/x_{B0}$ as a function of collector current density $J_C$. The QN base width ($W_B$) with carrier-velocity saturation can be expressed by

$$W_B = W_{JC} - x_B$$  \hspace{1cm} (7)$$

while the base width neglecting velocity saturation ($W_{B0}$) is expressed by

$$W_{B0} = W_{JC} - x_{B0}.$$

(8)

As can be seen from Fig. 3, as $J_C$ approaches $J_{EPI}$, $x_B$ decreases rapidly. Therefore, $dW_B/dV_{CE}$ differs significantly from the value $dW_{B0}/dV_{CE}$ found in Roulston [3, eq. (1)].
Fig. 3. Plot of the ratio $x_B/x_B$ as a function of collector current density $J_C$ for $N_A = 1 \times 10^{17} \text{cm}^{-3}$ and $x_{EP} = 1 \times 10^{17} \text{cm}^{-3}$.

$J_C$ can be expressed as

$$J_C = qD_n n(0) / W_B$$

(9)

where $x$ is an empirical factor that allows for drift current and $n(0)$ is the electron concentration at the edge of the emitter-base SCR in the base region (Fig. 2(a)). Using (2), (9), and the definition of the Early voltage, $V_A$ can be expressed as

$$x_B \equiv -W_{EP} \pm \sqrt{W_{EP}^2 \left[ 1 + \frac{N_{EP}(1 - J_C/W_{EP})}{N_A(1 + J_C/J_A)} \right] + \frac{2\epsilon_e(V_{CB} + \phi_C)}{qN_A(1 + J_C/J_A)}}.$$

(10)

Similarly, an expression for the Early voltage neglecting velocity saturation can be found from (8)–(10), assuming $n_c = 0$, as

$$V_{no} \equiv \frac{W_{EP}(V_{CB} + \phi_C)}{0.5x_B}.$$

(12)

Equation (11) is similar in form to (1) except for the addition of a third term in the brackets. The last two terms have only a small effect on $V_A$ except for very narrow base widths. For $J_C > 0.1J_{EP}$, however, (11) predicts more significant increases in $V_A$ due to the $(1 - J_C/J_{EP})^{1/2}$ dependence of $x_B$ in the factor $W_B(V_{CB} + \phi_C)/(0.5x_B)$ in (11).

Equation (11) is valid only up to the value of $J_C$ for which the base-collector SCR extends all the way to the buried layer for a given value of $V_{CB}$, i.e., when $x_C = x_{EP}$. The upper limit of validity for (11) can be found from (3) and (5) with $x_C$ replaced by $W_{EP}$

$$J_C \left|_{J_C = W_{EP}} \right. \equiv \frac{J_{EP}}{1 + \frac{N_A(x_{EP})^2}{N_{EP}W_{EP}}} \left[ 1 - \left( \frac{x_{EP}}{W_{EP}} \right)^2 \right].$$

(13)

where

$$x_{EP} = \frac{2\epsilon_e(V_{CB} + \phi_C)}{\sqrt{qN_{EP}(J_C/J_{EP} - 1)}}$$

(14)

is the value of $x_E$ obtained from the depletion approximation. For typical BJTs, $(N_A/N_{EP})(x_{EP}/W_{EP})^2 << 1$. Thus when $W_{EP} >> x_{CO}$, (11) is valid for values of $J_C$ very close to $J_{EP}$, so that the effect of carrier-velocity saturation on $V_A$ can be very large.

B. Case 2

As $J_C$ increases above $J_C \left|_{J_C = W_{EP}} \right.$ the collector-base SCR begins to uncover charge in the buried layer. The resulting electron concentration and electric field distribution are shown in Fig. 2(b). As the current increases above $J_{EP}$, the electron concentration in the epi rises above $N_{EP}$, leading to field and electron concentration distributions as shown in Fig. 2(c). Using charge neutrality and solving Poisson's equation over the collector junction SCR, $x_B$ for Case 2 (Fig. 2(b) and (c)) can be written as

$$V_A \equiv \frac{W_{EP}(V_{CB} + \phi_C)}{0.5x_B} \left[ 1 + \frac{2\epsilon_e(V_{CB} + \phi_C)}{qN_A(1 + J_C/J_A)} \right].$$

(15)

From (7), (10), and (15), the Early voltage $V_A$ can be expressed as

$$V_A = \frac{W_{EP}(V_{CB} + \phi_C)}{0.5x_B} \left[ 1 + \frac{2\epsilon_e(V_{CB} + \phi_C)}{qN_A(1 + J_C/J_A)} \right].$$

(16)

C. Case 3

Further increments in $J_C$ drive the BJT into nonohmic quasi-saturation (NOQS). Fig. 2(d) shows a typical electron concentration and electric field distribution in NOQS. In NOQS operation, the epi-SCR excess free-electron concentration ($n_c - N_{EP}$) is balanced by the heavily doped buried-layer charge. Solution of Poisson's equation leads to

$$x_{EP} \equiv \frac{2\epsilon_e(V_{CB} + \phi_C)}{\sqrt{qN_{EP}(J_C/J_{EP} - 1)}}.$$

(17)

where $x_{EP}$ is the epilayer SCR width in NOQS operation (Fig. 2(d)). In this case $W_B$ must be redefined as

$$W_B = W_C + W_{EP} - x_{EP}.$$

(18)

Combining this expression with (10) and (18) yields an Early voltage expression for NOQS mode
becomes proportional to \((J_c)^{1/2}\). For very high base-collector reverse biases or very narrow epi-thicknesses the epilayer can become completely depleted even at low currents. For this case (11) is not valid, and (16) is valid for any current up to the value of \(J_C\) given by (20). Equation (19) remains valid for NOQS operation. Fig. 5 shows the Early voltage variation as a function of \(J_C\) for \(k = 1, D_n = 17 \text{ cm}^2/\text{V} \cdot \text{s}\), and \(V_{CB} = 3 \text{ V}\) for a BJT with a 0.35-\(\mu\)m epi-thickness, which is thin enough to allow epilayer depletion at low currents. As shown in the figure, carrier-velocity saturation can still enhance the output resistance considerably in forward-active mode for \(J_C > J_{EPI}\).

### III. Numerical Simulations

A series of numerical simulations were performed using PISCES-II and MMSPICE to verify that these effects can indeed occur. In PISCES-II the effect of carrier-velocity saturation on Early voltage was studied by performing simulations with and without the field-dependent mobility which models carrier-velocity saturation. Several BJT structures were simulated, and the results were consistent with analysis. Fig. 6 shows a comparison of \(V_a\) behavior with and without field-dependent mobility for a transistor with a 1.9-\(\mu\)m-thick epilayer. As can be seen in Fig. 6, using the field-dependent mobility model, \(V_a\) increases considerably at high currents, whereas with the field-dependent mobility turned off, \(V_a\) increases only slightly (due to emitter-side base-width modulation). In the lower curve (with field-dependent mobility turned off) the Early voltage drops at high currents. This effect can be explained by the onset of ohmic quasi-saturation.

The physics-based BJT model in the circuit simulator MMSPICE [1] includes a charge-based model for advanced high-speed transistors based on one-dimensional analysis of carrier transport. The analysis accounts for high-current effects and impact ionization. The model covers all of the cases considered in the above analyses. Appropriate charge equations are applied to the various regions of the device, allowing for moving regional boundaries. The resulting set of coupled equations require iterative numerical solution. The highly physical basis of this approach allows the software to be used for device simulation as well as for circuit simulation.
Fig. 6. PISCES-II simulation of Early voltage variation as a function of collector current. The device was similar to MOSAIC III BJT [8] except the epi was extended to 1.9 μm. $N_{epi} = 1 \times 10^{16} \text{cm}^{-3}$, $W_{epi} = 0.15 \mu \text{m}$, and $V_{CE} = 10 \text{V}$.

Fig. 7. MMSPICE simulation results of Early voltage and SCR penetration into the base as a function of collector current for a typical analog BJT with $N_{epi} = 1 \times 10^{16} \text{cm}^{-3}$, base width $= 0.8 \mu \text{m}$, epi-width $= 7 \mu \text{m}$, and $V_{CE} = 15 \text{V}$.

We have modified MMSPICE to allow output of internal physical parameters (e.g., $x_{B}$, $x_{C}$, QN base width, and QN epi-width), in addition to the usual voltage and current outputs. Fig. 7 shows $V_{A}$ and $x_{A}$ variations for a typical analog BJT as a function of $I_{C}$ for a fixed $V_{CE}$. As can be seen in the figure, MMSPICE predicts substantial increases in Early voltage due to carrier-velocity saturation at high currents. Fig. 7 also clearly shows that the Early voltage enhancements are associated with variations in $x_{B}$.

IV. Conclusions

The analysis in Section II demonstrates that BJT output resistance can be raised significantly by carrier-velocity saturation. For typical base widths, there are usually small increases in output resistance at low currents, but the most important effects are predicted for currents close to the critical value $J_{epi}$. These effects are also predicted by PISCES and by the highly physical circuit/device simulator MMSPICE. In practice, thermal feedback tends to severely degrade the output resistance at high currents [9]–[11] which tends to mask the $V_{A}$ enhancement. With an operating point chosen near $J_{epi}$ it may be possible to design high-speed, high-power amplifiers with very high voltage gain if operation is restricted to frequencies high enough to avoid thermal feedback.

REFERENCES


Sang-Gug Lee was born in KyungNam, Korea, in 1958. He received the B.S. degree in electronic engineering from KyungPook National University, Taegu, Korea, in 1981, and the M.E. degree in electrical engineering from University of Florida, Gainesville, in 1989. He is currently working toward the Ph.D. degree at University of Florida, specializing in BJT small-signal modeling. From 1983 to 1986, he was an Instructor in the Department of Electronic Engineering at the Naval Academy, JinHae, Korea.

Robert M. Fox (S'78-M'80) was born in Birmingham, AL, on November 12, 1950. He received the B.S. degree in physics from the University of Notre Dame, Notre Dame, IN, in 1972, and the M.S. and Ph.D. degrees in electrical engineering from Auburn University, Auburn, AL, in 1981 and 1986, respectively. Since 1986, he has served as Assistant Professor of Electrical Engineering at the University of Florida, Gainesville. His research interests center on circuit design for advanced silicon technologies. Dr. Fox is a member of the Audio Engineering Society, ASEE, Phi Kappa Phi, andEta Kappa Nu.