Low power fully differential frequency doubler

Moon-Su Yang, Seung-Min Oh and Sang-Gug Lee

A novel fully differential frequency doubler is proposed based on CMOS technology, where a stacked push–push configuration is used to generate differential output. Compared to previously reported doublers, the proposed topology has advantages in power dissipation, fundamental frequency rejection, and simplicity. By utilising the proposed doubler, a low power direct-conversion up-mixer is designed for 900 MHz applications. The fabricated up-mixer shows 5.5 dB of power conversion gain and 7.5 dBm of output IP3, while dissipating total current of 4.5 mA from 1.25 V supply.

Introduction: A frequency doubler is a useful component in various RF applications: to avoid VCO injection pulling in direct-conversion transmitters [1], to prevent self-mixing in direct conversion receivers [2], and simply to extend the frequency of oscillation [3]. The important features of the frequency doubler are the conversion efficiency, fundamental frequency rejection, power dissipation, and simplicity as additional circuitry. A few frequency doubler topologies have been reported previously. Kimura and Asazawa [4] reported a frequency doubler based on a dual unbalanced emitter-coupled pair. In this topology, a differential output is obtained for the given differential input. Zhang and Yun [3] reported a push–push frequency doubler based on a differential pair. Zhang and Yun's topology is simple and dissipates half the amount of DC currents than that of Kimura and Asazawa's. However, Zhang and Yun's topology provides only single-ended output for the differential input. The frequency doubler proposed in this Letter dissipates the same current as Zhang and Yun's yet provides fully differential outputs.

Proposed frequency doubler: Fig. 1 shows the proposed frequency doubler, which is designed with a stacked push–push configuration using *N*- and *P*-MOS transistors to generate differential output. In Fig. 1, the large resistors R_B are included for DC biasing which makes no additional DC bias necessary. The output loads at nodes *A* and *B* are implemented with inductors considering the low supply voltage of 1.25 V.

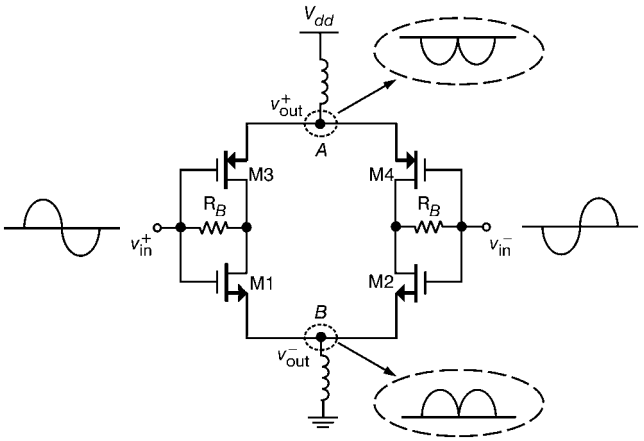

Fig. 1 *Proposed fully differential frequency doubler*

In Fig. 1, for the large differential input voltage v_{in}^{+} and v_{in}^{-}, the transistor pairs M_1–M_2 and M_3–M_4 operate as a switch. As shown in Fig. 1, during the first half cycle of the input signal, the transistors M_1 and M_4 are turned on and M_2 and M_3 are turned off. The outputs v_{out}^{+} and v_{out}^{-} follow v_{in}^{-} and v_{in}^{+}, respectively, as M_1 and M_4 constitute a source follower. Similarly, during the second half cycle of the input signal, the outputs v_{out}^{+} and v_{out}^{-} follow v_{in}^{+} and v_{in}^{-}. As a result, the frequency of the overall output waveforms, v_{out}^{+} and v_{out}^{-}, becomes two times that of the fundamental frequency as shown in Fig. 1. With increase in the frequency of operation, the output waveform of the proposed doubler shapes close to the sinusoidal wave. This is due to the limited cutoff frequency of the source follower transistors, yet it has no deteriorating effects on the frequency of interest. The difference in the transconductance of the *N*- and *P*-MOS transistors can lead to a mismatch in the amplitude of the two frequency-doubled output signals. This amplitude mismatch can be alleviated by optimising the size of the constituting transistors and the inductances at nodes *A* and *B*.

The performance of the proposed frequency doubler shown in Fig. 1 is evaluated with 450 MHz input signal, which is implemented in 0.25 µm CMOS technology. From the simulation, the frequency doubler shows good frequency conversion and −4 dB of gain. In addition, the frequency spectrum of v_{out}^{+} and v_{out}^{-} shows strong rejection, larger than 50 dB, to the fundamental and other higher odd-order harmonics of the fundamental. The bandwidth of the frequency doubler ideally can approach the cutoff frequency of the transistors as the source follower provides wide bandwidth during each half cycle of the fundamental frequency.

Direct-conversion up-mixer: By utilising the newly proposed differential frequency doubler, a direct-conversion up-mixer has been designed as shown in Fig. 2. In Fig. 2, the mixer core is designed based on the Gilbert-cell, and the output load of the mixer is implemented using an external LC network that converts the differential RF output to a single-ended RF signal [2]. The single-ended mixer output helps to reduce the power dissipation of the overall transmitter since it allows a single-ended driver amplifier. In Fig. 2, the output of the frequency doubler is applied directly to the up-mixer core without requiring buffer stages due to the low output impedance of the frequency doubler. The elimination of the buffer stages helps to achieve lower power dissipation.

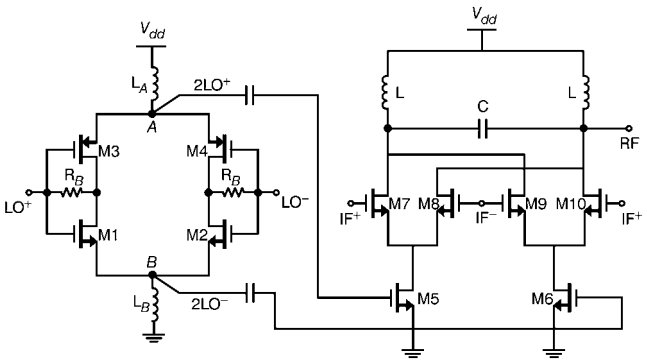

Fig. 2 *Proposed direct-conversion up-mixer*

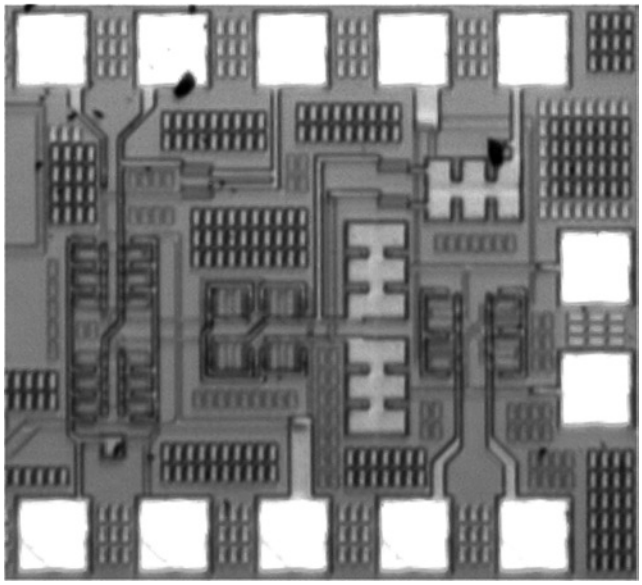

Fig. 3 *Microphotograph of fabricated chip*

The direct-conversion up-mixer shown in Fig. 2 has been fabricated based on 0.25 µm CMOS technology. Fig. 3 shows the microphotograph of the fabricated chip. The chip area is 0.5 mm^2. In the measurement, 10 MHz IF signal and 450 MHz LO signal are applied to the up-mixer. The measured up-mixer shows 5.5 dB of power conversion gain, 7.5 dBm of output IP3, and 40 dB rejection to the fundamental

LO signal, while dissipating 4.5 mA from 1.25 V supply. Of the total current, the frequency doubler dissipates 1 mA. The IP3 behaviour of the designed up-mixer is shown in Fig. 4.

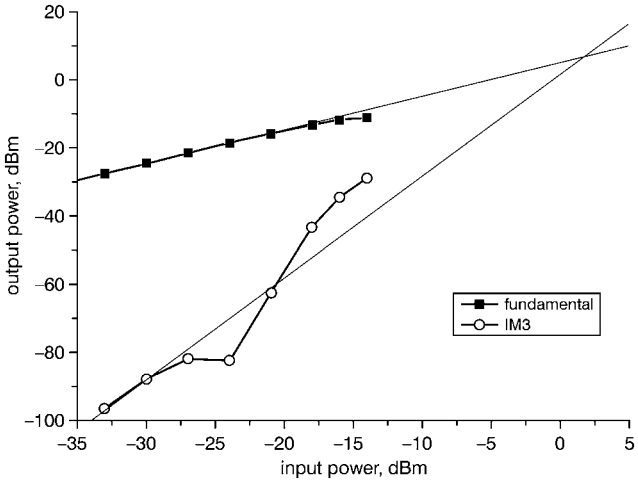

Fig. 4 *Measured IP3 behaviour of up-mixer*

Conclusion: A new fully differential frequency doubler is proposed. The proposed differential frequency doubler provides good conversion gain, high fundamental frequency rejection, and wide bandwidth, yet dissipates half current of the previously reported frequency doubler [4]. By adopting the newly proposed frequency doubler, a low power direct-conversion up-mixer has been designed. The designed up-mixer shows good conversion gain and linearity, and high rejection to the fundamental LO signal.

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