Brief Papers

A Very Low-Power Quadrature VCO With Back-Gate Coupling

Hye-Ryoung Kim, Choong-Yul Cha, Seung-Min Oh, Moon-Su Yang, and Sang-Gug Lee

***Abstract*—A new quadrature voltage-controlled oscillator (QVCO) topology is proposed where the back-gates of the core transistors are used as coupling terminals. The use of back-gates reduces the power dissipation and removes the additional noise contributions compare to the conventional coupling transistor based topology. The advantages of the proposed QVCO topology in comparison with prior works are exploited based on simulation. A QVCO based on the proposed topology with additional design ideas has been implemented using a 0.18-μm triple-well technology for 1 GHz-band operation, and measurement shows the phase noise of −120 dBc/Hz at 1-MHz offset with output power of 2.5 dBm, while dissipating only 3 mA for the whole QVCO from 1.8-V supply.**

***Index Terms*—Back-gate coupling, CMOS, low power, quadrature, voltage-controlled oscillator (VCO).**

I. Introduction

In THE last few years, the research and development of direct conversion radio transceivers have dramatically increased due to the need for low-power, low-cost, and highly integrated transceiver chips [1]. Many direct conversion architectures require quadrature local oscillator (LO) signals, and various quadrature signal generation techniques have been reported, such as the combination of voltage-controlled oscillator (VCO) and poly-phase filter [2], VCO at double frequency followed by master–slave flipflops, ring-type oscillators [3], and the quadrature voltage-controlled oscillator (QVCO) [4]. Among these quadrature signal generation techniques, the LC-tuned QVCOs are a popular topology to achieve low phase noise, but they tend to dissipate rather high power [5], [6]. Fig. 1 shows a conventional LC-QVCO schematic reported in [4]. In Fig. 1(a), each differential VCO consists of a cross-coupled pair of transistors (M_1–M_2 and M_3–M_4) with an LC-tuning circuit. The additional transistors (M_5–M_6 and M_7–M_8) are used for quadrature coupling between the two differential VCOs. In Fig. 1(a), the ports A, B, C, and D of each differential VCO are tied to the corresponding ports of the other.

Many works have been reported to improve phase noise and power dissipation based on the conventional topology shown in Fig. 1(a) [5]. However, in the aspects of phase noise and power dissipation, the presence of the additional coupling transistors in Fig. 1(a) makes it inherently inferior to the topology proposed in this work. The LC-QVCO topology proposed here enables quadrature coupling without requiring additional transistors. In Section II, new QVCO topology using back-gate coupling is introduced and the operational principles are described. In Section III, design and measurement results are reported. Section IV concludes.

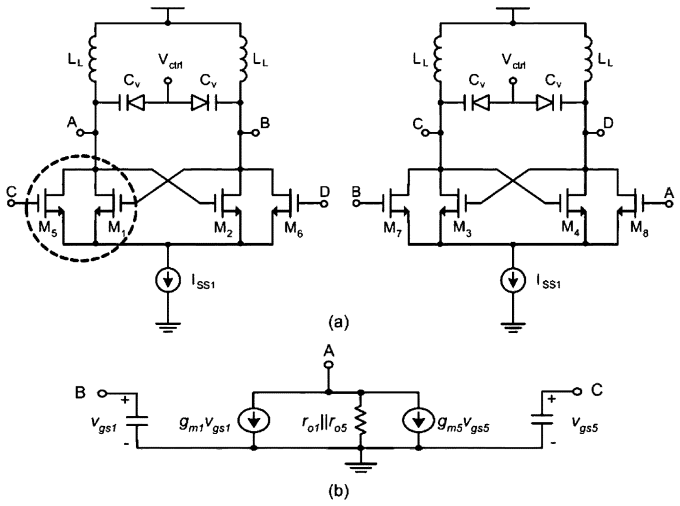

Fig. 1. (a) Conventional LC-QVCO schematic. (b) Small-signal equivalent circuit of the circled part.

II. New QVCO Topology

Fig. 2(a) shows the proposed QVCO topology. In Fig. 2, all transistors are assumed to be housed in separate wells, so that each transistor can be used as full four-terminal device. As can be seen from Fig. 2(a), compared to the topology shown in Fig. 1(a), the coupling transistors are removed and the two differential VCOs are coupled through the back-gates (or body terminals) of the core nMOS transistors. The resistors R_b in Fig. 2(a) are added for dc biasing of the body terminals and the capacitors C_b for ac coupling. As in Fig. 1(a), where the main and the coupling signals that come from nodes B and C, respectively, set the signal values at node A, in Fig. 2(a), the signals from nodes b and c set the signal value at node a.

Figs. 1(b) and 2(b) show the small-signal equivalent representation for the circled part of the circuit shown in Figs. 1(a) and 2(a), respectively. In Fig. 2(b), v_{gs9} and v_{bs9} are the corresponding signals of v_{gs1} and v_{gs5} in Fig. 1(a), and g_{m9} and g_{mb9} are the matching components of g_{m1} and g_{m5}, respectively. It can be seen that the two small-signal circuits shown in Figs. 1(b)

Manuscript received June 10, 2003; revised March 8, 2004. This work was supported by Digital Media Laboratory, which is funded by the Ministry of Information and Communications, Korea.

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Digital Object Identifier 10.1109/JSSC.2004.827798

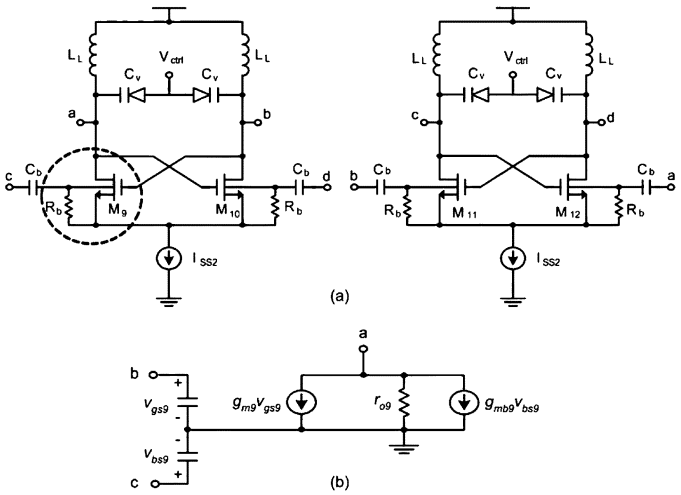

Fig. 2. (a) Proposed back-gate coupled LC-QVCO. (b) Small-signal equivalent circuit of the circled part.

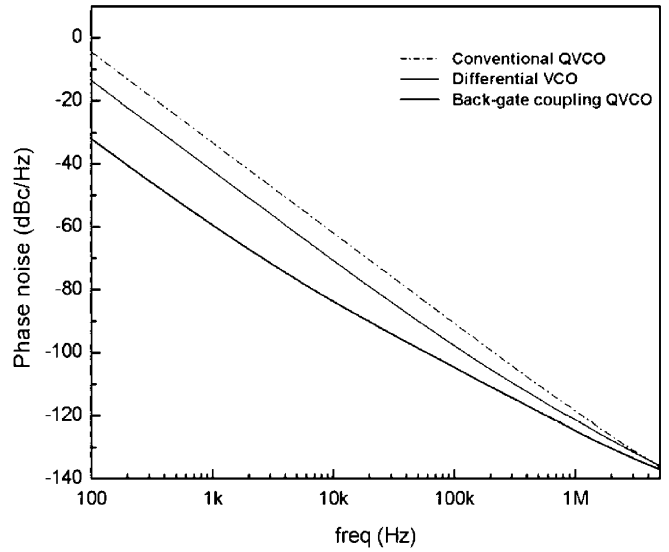

Fig. 3. Simulated phase noise performance of the conventional QVCO, back-gate coupled QVCO, and differential VCO at 1-GHz oscillation frequency.

and 2(b) are effectively the same and the back-gate in Fig. 2(b) replaces the coupling transistor M_5 of the conventional QVCO.

According to [6], the phase noise in the conventional QVCO shown in Fig. 1(a) is greatly degraded by the variations in the transconductance of the coupling transistors M_5–M_8 (G_{Mc}). The $1/f$ noise currents from the coupling transistors produce a slowly varying current offset which affects the current level flowing into the LC-tank. This offset current changes G_{Mc} and the coupling of both oscillators, leading to output frequency modulation and, therefore, the degradation in the phase noise. Furthermore, as reported in [4]–[6], the coupling transistors dissipate $30 \sim 100\%$ of the power dissipated in the core transistors, leading to a significant increase in overall power dissipation. Compared to that, in the QVCO topology proposed in this work, by utilizing the back-gate, the additional noise source as well as power dissipation can be avoided altogether. Note that although the transistor with back-gate coupling effectively works as two source-coupled transistors, the overall $1/f$ noise is expected to

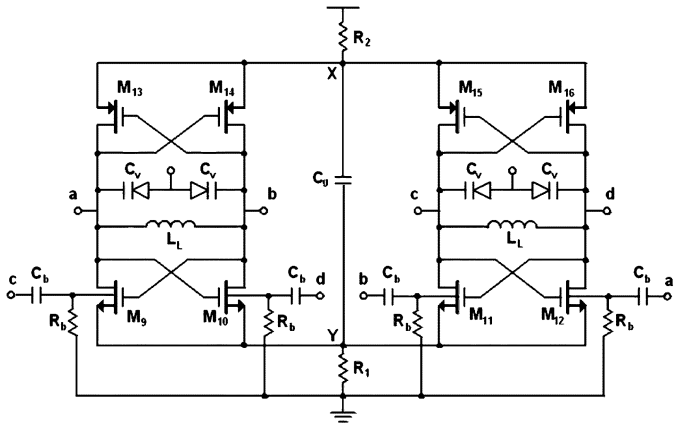

Fig. 4. Schematic of the fabricated back-gate coupled LC-QVCO.

be the same as that of the conventional single transistor, since the $1/f$ noise of the transistor originates from the same location. Therefore, it can be thought that the body-coupled transistor is added free of $1/f$ noise. The nMOS transistors for body-gate coupling in Fig. 2(a) can be replaced as pMOS transistors.

Fig. 3 compares the phase noise performance of the conventional and proposed LC-QVCO as well as the differential VCO from the simulations based on 0.18-μm CMOS technology. All three oscillators are designed to oscillate at 1 GHz. In Fig. 2, each constituting differential VCOs of all three circuits are biased to dissipate 3 mA from 1.8-V supply, and the coupling transistors in Fig. 1 (M_1–M_8) dissipate a total of 2 mA. Therefore, the total current dissipation for the differential VCO, proposed QVCO, and conventional QVCO are 3, 6, and 8 mA, respectively. With the conventional QVCO, the current ratio of 3:1 between the transistors that constitute the differential VCO (M_1–M_4) and the coupling (M_5–M_8) reported the best phase noise [5]. From Fig. 3, as expected, the conventional QVCO shows higher phase noise than that of the differential VCO, while the back-gate coupled QVCO not only shows significantly lower phase noise than that of the conventional QVCO, despite the lower power dissipation, but the proposed QVCO shows less phase noise than that of the differential VCO. From Fig. 3, the proposed QVCO shows improvement in phase noise by 26, 21, and 14 dB compared to the conventional QVCO, and 17, 13, and 7 dB compared to the differential VCO, at the frequency offset of 1, 10, and 100 kHz, respectively. The lower phase noise of the proposed QVCO compared to the differential VCO might be explained by the increase in the overall transconductance of the back-gate coupled transistors. In addition, considering the origin of $1/f$ noise in MOS transistor, the back-gate transistor adds negligible $1/f$ noise, as it involves no Si–SiO_2 interface.

III. QVCO Design and Experimental Results

Fig. 4 shows the implemented LC-QVCO schematic based on the newly proposed topology. In Fig. 4, the QVCO consists of two identical complementary differential VCOs coupled through the back-gates of nMOS transistors for the quadrature outputs. The complementary differential VCOs are chosen for better phase noise by improving the symmetry and transconductance [7]. Note that, in Fig. 4, the couplings can be applied to the

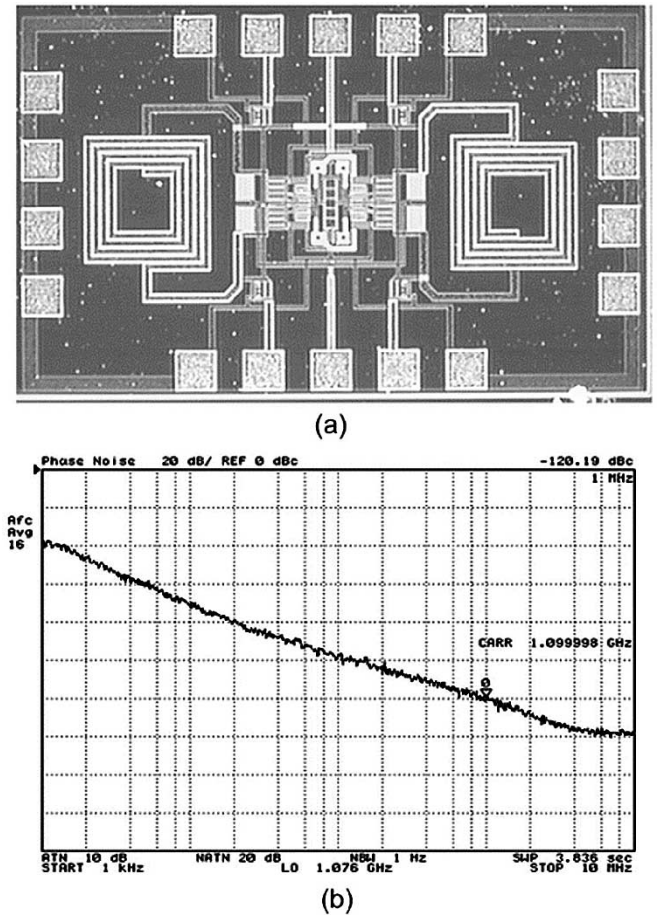

Fig. 5. (a) Die photograph. (b) Measured phase noise performance.

back-gates of pMOS transistors as well. The nMOS transistors are chosen with current design considering the higher amount of coupling due to the higher transcondcutance of nMOS transistors. In Fig. 4, the two resistors R_1 and R_2 are adopted as current sources in order to improve the symmetry of the complementary differential oscillators, and the resistor values are chosen for maximum current-limited operation [7]. The dual current sources R_1 and R_2 are also chosen to accommodate the coupling capacitor C_g. The capacitor C_g helps to suppress the injection of the high-frequency noise from the current sources into the oscillator core by canceling the large-amplitude harmonics generated at the common-source nodes of the oscillator core [8]. Due to the differential voltage swing of the even-order harmonics of each differential VCO core at nodes X and Y in Fig. 4, the addition of the on-chip coupling capacitor C_g provides an on-chip ac ground and cancels out harmonics leading to phase noise suppression. Compared to the previous work [8], where the current source is shunted by a capacitor terminated to the off-chip ground, the on-chip capacitor C_g can provide low-impedance ac ground up to very high frequency by its high resonance frequency and requires no additional bondpad.

The LC-QVCO topology shown in Fig. 4 is implemented in a standard triple-well 0.18-μm CMOS technology for 1-GHz-band operation. Fig. 5(a) shows the die photograph. As can be seen in Fig. 5(a), the implemented QVCO uses on-chip inductors, and on-chip accumulation-mode MOS varactors [9] are adopted for tuning. Fig. 5(b) shows a plot of the measured phase noise versus offset frequency at 1.1-GHz oscillation with output power of 2.5 dBm. As can be seen in Fig. 5(b), the measured phase noise at 1-MHz offset is -120 dBc/Hz while dissipating a total of only 3 mA for the whole QVCO from 1.8-V supply. Table I summarizes the measurement results at 1.1-GHz operation and Table II compares the performance with prior works. In Table II, though the one-to-one comparison with prior works might be improper, due to the differences in individual oscillator core optimization techniques and the tuning elements, this work shows a major advantage in power dissipation.

TABLE I
MEASURED PERFORMANCE OF THE FABRICATED LC-QVCO

Supply voltage	1.8 V
Supply current	3 mA
Output power	> 2.5 dBm
Oscillation frequency	1.1 GHz
Tuning range	1.047 ~ 1.39 GHz
Phase noise @ 1 MHz offset	- 120 dBc/Hz
Process	0.18-μm CMOS

TABLE II
COMPARISON OF THE PERFORMANCE WITH PRIOR WORKS

CMOS QVCO	Technology [μm]	Frequency [GHz]	Power [mW]	Phase Noise [dBc/Hz]	FOM [dBc]
[4]	1	0.9	30	-85 [@100k]	-149.31
[5]	0.25	1.8	20	-143 [@3M]	-185.55
[6]	0.35	1.8	50	-140 [@3M]	-178.57
[10]	0.25	1.57	30	-147 [@3M]	-186.59
[11]	0.18	6	6.8	-106 [@1M]	-173.24
This work	0.18 triple - well	1.1	5.4	-120 [@1M] -137 [@3M]	-173.50 -180.96

IV. CONCLUSION

A very low-power and low-phase-noise QVCO topology based on CMOS technology is proposed. In the proposed QVCO, the quadrature couplings are realized by utilizing the back-gates of the core transistors. The advantage of the proposed QVCO is analyzed in terms of phase noise and power dissipation. From the simulation, the advantages of the proposed QVCO are demonstrated in comparison with the conventional coupled-transistor-based QVCO and the differential VCO. A 1-GHz QVCO, adopting the newly proposed QVCO topology, is implemented in 0.18-μm triple-well CMOS technology where additional design techniques are applied to improve the symmetry of the complementary VCO and to suppress the tail current noise contribution. From the measurements, the implemented QVCO shows phase noise of -120 dBc/Hz at 1-MHz offset while dissipating only 3 mA for the whole QVCO from 1.8-V supply.

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