Low-voltage, high dB-linear, exponential V-V converter

Q.-H. Duong, V. Krizhanovskii, H.-C. Choi, S.-J. Yun, M.-S. Yang and S.-G. Lee

A new idea is proposed to make use of the disadvantages at low-voltage operations to widen the output dynamic range and the input swing of the exponential voltage-to-voltage circuit with differential input, at low-voltage low-power applications. The pseudo-exponential function is used to realise the exponential characteristic. Based on 0.25 μm CMOS technology, simulations show a 16 dB linear improvement of the output voltage range while dissipating less than 0.2 mW from 1.25 V supply voltage.

Introduction: CMOS devices have the important feature that they are easily scaled. Scaling down the transistor sizes enables integration of more circuit components in a single chip so that the circuit area, and thus its cost, will be reduced. However, scaling down also leads to MOS transistors with thinner gate oxides; and, to prevent the transistor from breakdown because of the higher electrical field across the thinner gate oxide and to ensure its reliability, the supply voltage has to be reduced. Lowering the supply voltage is also one of the most effective ways of reducing power consumption. However, many of the existing CMOS analogue building blocks, designed to operate with higher supply voltages, will lose a significant amount of operating range and need to be reconsidered. In this Letter, a new idea to solve this problem at low-voltage operations is proposed; moreover, this idea also improves the performance of the exponential voltage-to-voltage converter (EVVC), therefore high performance EVVC at low-voltage low-power application is achieved.
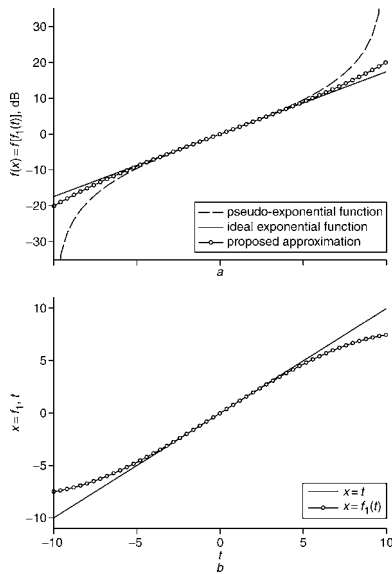

Fig. 1 *Various functions on dB scale, and variable x as linear and nonlinear functions of t*

a Functions on dB scale
b Variable x as linear and nonlinear functions of t

Proposed idea: EVVCs are usually implemented with bipolar or MOS transistors in weak inversion, because of their exponential *I–V* characteristics. However, bipolar transistors are not compatible with CMOS technology, and MOS transistors in weak inversion are limited to low-frequency applications because of their poor frequency response. Consequently, the 'pseudo-exponential' generators [1, 2] and the Taylor series approximation [3, 4] have been introduced as alternatives. The pseudo-exponential function is given as

$$f(x) = e^{2ax} = \frac{e^{ax}}{e^{-ax}} \simeq \frac{1+ax}{1-ax} \qquad (1)$$

where *a* and *x* are the coefficient and the independent variables, respectively. Equation (1) is valid for $|ax| \ll 1$. Using MATLAB to investigate (1), the results show 15 dB linear range with the linearity error $< \pm 0.5$ dB for $|x| < 0.42$ as shown in Fig. 1*a* by the dashed line,

which is drawn for the constant $a = 0.1$. Otherwise, the deviation of (1) from the ideal exponential function will increase drastically. As a result, the dB linear range as well as the input range is critically limited. In this Letter, the variable *x* is considered as a function of *t* as depicted in Fig. 1*b*, the *x* is relatively linear function of *t* for $|t| \ll 5$ (i.e $x = t$). In this region, from (1) the $f(x) = f(t)$ is closed to the ideal exponential function as depicted in Fig. 1*a* by the dashed and circle symbol lines. Otherwise, *x* is a nonlinear function of *t* as shown in Fig. 1*b* by the circle symbol line (let $x = f_1(t)$). Intuitively, from (1) one can see that the equation $f(x) = f[f_1(t)]$ as a function of *t* is shifted to the ideal exponential function as shown in Fig. 1*a* by the circle symbol line, leading to the improvement of both the dB linear output range and the input range. In this Letter, the variable *x* and *t* are chosen to be current and differential input voltage parameters, respectively. Hence, the output voltage $f(x)$ is a function of the differential input voltage *t*.

Low-voltage low-power EVVC design: Fig. 2 shows the schematic of the proposed EVVC that implements (1) and the proposed idea. As shown in Fig. 2, the voltage-to-current converter (VCC) is a differential amplifier with M_3 and M_4 as diode connected loads. Neglecting the second-order effects and assuming that all transistors are biased in the saturation region, the drain current of transistor $M_{1,2}$ is given as

$$I_{1,2} = \left(\frac{1}{2}\right)\left(\frac{\mu_n C_{ox} W}{L}\right)(V_{in\pm} + V_{cm} - V_p - V_{TH}) \qquad (2)$$

where V_{cm} and V_{TH} are, respectively, the common-mode input voltage and the threshold voltage of $M_{1,2}$. The V_{cm} is chosen to bias $M_{1,2}$ in the saturation region. The $I_{1,2}$ are, respectively, copied to M_5 and $M_{6,7}$ by a multiplication factor of a constant *k*. The two output currents *I* of the VCC as shown in Fig. 2 are given as $I = k(I_1 - I_2)$ From (2), *I* is calculated as

$$I = k(I_1 - I_2) = \beta(V_{in+} - V_{in-}) = \beta V_d \qquad (3)$$

where $\beta = k(\mu_n C_{ox} W/L)(V_{cm} - V_p - V_{TH})$ and $V_d = V_{in+}$ in V_{in-}. Equation (3) shows that the output current of the VCC, *I*, is linear function of V_d. The current *I* is, respectively, added and subtracted to the bias current I_0 to form two current signals, $(I + I_0)$ and $(I - I_0)$ as shown in Fig. 2. The current $(I + I_0)$ is copied to the drain current of the transistor M_{14}, while the current $(I - I_0)$ is fed to the drain of two diode connected transistors M_{11} and M_{12}. As in [2] the transistors M_{11} and M_{12} constitute the linear *I–V* converter, and the output voltage of this converter is given as [2]

$$V_{G,M_{11,12}} = \frac{V_{DD} - |V_{Tp}| + V_{Tn}}{2} - \frac{(I - I_0)}{K(V_{DD} - |V_{Tp}| - V_{Tn})} \qquad (4)$$

where $V_{G,M_{11,12}}$ is the output voltage of this converter which is also the gate voltage of transistor M_{15}. The transistor M_{15} is assumed to be in the triode region and acts as a voltage controlled resistor. For small drain-source voltage, the resistance exhibited by M_{15} is given as

$$R_{DS,M_{15}} \simeq \frac{1}{K_{M_{12}}(V_{G,M_{11,12}} - V_{TH})} \qquad (5)$$

Consequently, the current $(I + I_0)$ flowing through M_{15} will generate a drain-source voltage, $V_{DS,M_{15}} = R_{DS,M_{15}}(I + I_0)$, proportional to $(I + I_0)/(I - I_0)$. Hence, the following equation applies

$$V_{out} = V_{DS,M_{15}} \simeq M\frac{I + I_0}{I - I_0} \qquad (6)$$

where M is a constant. I_1 is a function of the input differential voltage $V_d = V_{in+} - V_{in-}$. Finally, from (6) the pseudo-exponential approximation of the proposed circuit shown in Fig. 2 is given as

$$V_{out} = M\frac{kV_d + I_0}{kV_d - I_0} = M\frac{kV_d/I_0 + 1}{kV_d/I_0 - 1} \qquad (7)$$

In (7), the output voltage V_{out} is obviously a pseudo-exponential function of the V_d, which is the same form of expression as in (1), where $a = k/I_0$.

The *I–V* performance of the VCC is shown in Fig. 3. When the supply voltage is reduced as shown in Fig. 3 by the solid line, as V_d increases to saturate either input transistors in the differential pair, the

linear relation of $I = \beta V_d$ no longer exists because of cutoff or weak inversion operation of either transistor. This results in a narrow window for differential-input voltage at low-voltage applications. Therefore, for the VCC to achieve large differential-input swing as shown in Fig. 3 by the dashed line, the supply voltage should be high; however, the power consumption is high as well. This issue is not compatible for low-voltage low-power applications. Fortunately, the idea in this Letter not only opens up a possibility to implement the I–V characteristic of the VCC at low-voltage applications but also extends the output range of the EVCC; hence, this idea is significant.
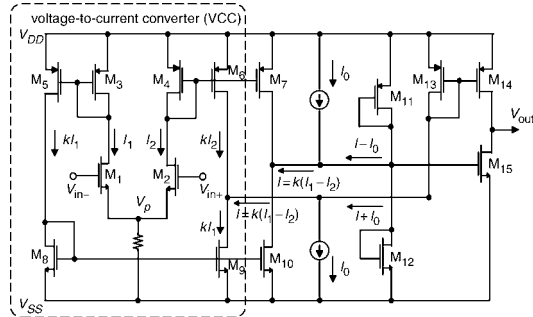

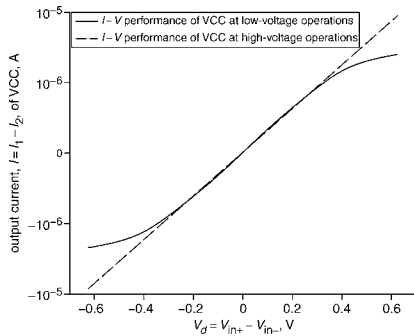**Fig. 2** *Proposed exponential voltage-to-voltage converter (EVVC)*

Fig. 3 *I–V performance of VCC shown in Fig. 2*

Simulation results: The feasibility of the proposed circuit was verified through simulation based on 0.25 μm CMOS technology. As discussed above, (1) is valid for $|x| \ll 1$, therefore (7) is also valid for $V_d \ll I_0/k$. For a given I–V characteristic of the VCC as shown in Fig. 3, I_0 and k are determined to satisfy the condition $|ax| \ll 1$, which means that $V_d \ll I_0/k$. Then, a 15 dB linear output voltage range with the error $< \pm 0.5$ dB can be obtained. When V_d increases beyond the linear region, the output current is a nonlinear function of V_d which helps to shift the approximation function close to the ideal exponential function as shown in Fig. 4 by the solid line. The performance of the proposed circuit is shown in Fig. 4, which shows 38 dB range, and 31 dB linear range with error $< \pm 0.5$ dB over large differential input voltage V_d from -0.625 to 0.58 V. The power consumption is < 0.2 mW from a 1.25 V supply voltage.
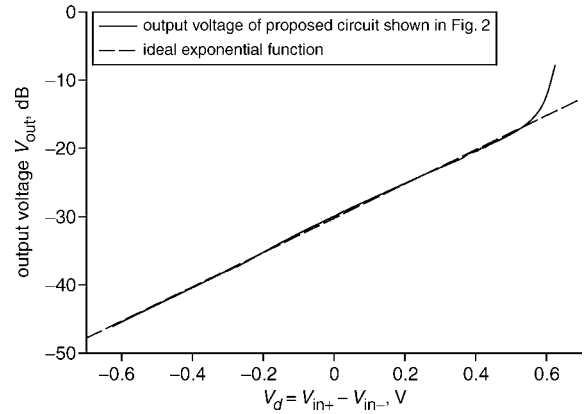

Fig. 4 *V-V performance of EVVC shown in Fig. 2*

By implementing circuits that also replicate (1), some of the previously reported EVCCs have been able to obtain 15 dB of amplitude variation with the error $< \pm 0.5$ dB [1, 2]. However, these circuits have single inputs, and the dB linear ranges are extremely limited. The circuit proposed can extend the dB linear range drastically. Moreover, the circuit provides rail-to-rail differential input, which is useful for the design of analogue and mixed-signal circuits such as log-domain filtering, AGC, etc.

Conclusions: We propose a new and compact EVVC that can operate at extremely low-voltage low-power applications and increase the output voltage range drastically (16 dB linear range improvement compared to traditional pseudo-exponential approximations [1, 2]). The proposed circuit offers significant performance advantages over previous works [1–4], such as high dB linear range, low-power (< 0.2 mW) and low-voltage (< 1.25 V) applications and differential input. The design details of the EVVC are described which could be used for very low-voltage and low-power VGA and AGC designs.

Q.-H. Duong, V. Krizhanovskii, H.-C. Choi, S.-J. Yun, M.-S. Yang and S.-G. Lee (*School of Engineering, RFME Lab, Information and Communications University, 119-Mujro, Daejeon 305-714, Republic of Korea*)

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