# THERMAL PARAMETER EXTRACTION FOR BIPOLAR CIRCUIT MODELLING

*Indexing terms: Modelling, Bipolar devices, Transistors, Semiconductor devices and materials*

A practical method is presented for extracting the thermal spreading resistance of BJTs, which is needed for accurate circuit simulation. The method uses the output resistance as the temperature sensitive parameter. Measurements can be made in the time or frequency domain.

*Introduction:* Thermal feedback from collector power to emitter temperature has been shown to significantly affect BJT performance.[1-4] Recently several workers[5,6] have demonstrated ways to model this thermal feedback in circuit simulation assuming that thermal model parameters are available. This Letter introduces a simple way to extract thermal parameters needed for such simulations.

BJT thermal behaviour is dominated by two components, characterised by the thermal spreading impedance and the chip/package thermal impedance. It is important to extract these components separately, as the package thermal impedance causes a coupling between transistors on the same chip, and thermal spreading impedance usually does not. Standard methods for extracting impedance are adapted for characterising power transistors.[7] They are poorly suited for measuring thermal spreading impedance, which becomes increasingly important with decreasing transistor size.

*Thermal impedance extraction method:* The standard electrical method for thermal impedance measurement is the 'emitter-only switching' method. In this technique, a large heating current is first applied to establish thermal equilibrium. This current is then turned off and the temperature is inferred from the resulting transient response of $V_{BE}$, measured at a small fixed emitter current. The initial response is controlled by both electrical and thermal spreading-impedance effects. This makes it difficult to determine the original temperature, and prevents accurate extraction of the thermal spreading resistance $R_{TH}$. The method is still useful, however, for finding package thermal impedance. For small transistors, the transient due to thermal spreading impedance is typically complete long before the thermal transient of the package begins. The transient of the package typically begins a few milliseconds after the power step and lasts for up to several minutes. The package thermal resistance can be found by dividing the total change in temperature after 1 ms by the size of the power step.

The following technique can be used to extract thermal spreading resistance. It is easy to show[1] that for small changes in the base and collector voltages, the change in $I_C$ can be written as

$$\Delta I_C = g_{21E}\,\Delta V_{BE} + g_{22E}\,\Delta V_{CE} + I_C D_C R_{TH}(I_C\,\Delta V_{CE} + V_{CE}\,\Delta I_C) \quad (1)$$

where $g_{21E}$ and $g_{22E}$ are common-emitter small-signal two-port parameters neglecting thermal effects, and $D_C$ is the fractional temperature coefficient of collector current ($D_C = I_C^{-1}\,\partial I_D/\partial T$). With $V_{BE}$ set to zero, eqn. 1 can be solved for $D_C R_{TH}$, which gives

$$D_C R_{TH} = \frac{\Delta I_C/I_C - \Delta V_{CE}/(V_A + V_{CE})}{I_C\,\Delta V_{CE} + V_{CE}\,\Delta I_C} \quad (2)$$

where $g_{22E}$ is expressed as $I_C/(V_A + V_{CE})$, where $V_A$ is the Early voltage. The extraction procedure is as follows. $V_{CE}$ is set to some value in the forward-active region. For a series of fixed values of $V_{BE}$, $V_{CE}$ is varied slightly and the resulting $\Delta I_C$ is measured. Because thermal effects are negligible for low currents, a constant value for $V_A$ can be extracted at low $V_{BE}$ values using

$$V_A \simeq (\Delta V_{CE}/\Delta I_C) I_C - V_{CE} \quad (3)$$

At higher currents, thermal effects become significant, and eqn. 2 can be used to extract the product $D_C R_{TH}$. For moderate currents, $D_C$ can be approximated as[3]

$$D_C = T^{-1}[V_T^{-1}(V_{GO} - V_{BE}) + \eta] \quad (4)$$

where $T$ is absolute temperature, $V_T$ is the thermal voltage, $V_{GO}$ for silicon is 1·205 V, and $\eta \simeq 2$. Eqn. 4 becomes inaccurate at very high currents, so it is important not to use such high currents in the extraction.

Note that output resistance should always be extracted with the base voltage fixed, not the base current. An equation comparable to eqn. 1 gives the change in base current as

$$\Delta I_B \simeq g_{11E}\,\Delta V_{BE} + g_{12E}\,\Delta V_{CE} + I_B D_B R_{TH}(I_C\,\Delta V_{CE} + V_{CE}\,\Delta I_C) \quad (5)$$

where $D_B$ is the fractional temperature coefficient of $I_B$. Because $g_{12E}$ is extremely small for narrow-base transistors, fixing $I_B$ and fixing $V_{BE}$ would be equivalent in the absence of thermal effects. In practice, however, with fixed $I_B$, $V_{BE}$ adjusts itself to compensate for temperature variations caused by a $V_{CE}$ change. This cancels most of the thermal effect on the output resistance. This effect is easily demonstrated by comparing output characteristics measured with fixed $I_B$ and with fixed $V_{BE}$. At high currents, the fixed $V_{BE}$ curves generally show much greater slopes.

It is important to carefully consider the timing of these measurements to avoid confusing thermal spreading and package thermal impedances. An HP 4145 semiconductor parameter analyser set to its minimum integration time requires at least 20 ms to measure a pair of ($V_{CE}$, $I_C$) data points, during which time substantial change in package temperature can occur. Longer delays between data points lead to larger errors. For this reason fast equipment is needed to extract thermal spreading resistance alone. A pulse generator, a current-to-voltage convertor and an oscilloscope are generally adequate.

A method which avoids this source of error involves measuring the output admittance $Y_{22}$ using an impedance analyser. As previously noted, for typical small transistors there is a period after a power step during which the thermal step response is constant for some time. This implies that there is also a range of frequencies over which the thermal frequency response is constant. In the middle of this frequency range $Y_{22}$ is also constant for a given current. Its real part can be denoted $g_{22}$. At low currents, thermal effects are negligible and $g_{22} = g_{22E} = I_C/(V_A + V_{CE})$, which can be used to find $V_A$. With increasing current, $g_{22}$ rises above $I_C/(V_A + V_{CE})$, and $R_{TH}$ can be extracted using

$$R_{TH} = \frac{1}{D_C}\,\frac{g_{22}/I_C - 1/(V_A + V_{CE})}{I_C - g_{22} V_{CE}} \quad (6)$$

This method generally gives results consistent with those found with the previous method.

*Extraction results:* Measured thermal spreading resistance values were used with eqns. 1 and 5 to predict BJT small-signal behaviour. Values for $D_C$ and $D_B$ were determined using SPICE. Fig. 1 shows measured and simulated variation of normalised output resistance $V'_A = r_0 I_C - V_{CE}$ with $I_C$. The transistor had an emitter area of $23 \times 23\,\mu m^2$, a base width of 1·0 $\mu$m, and epitaxial-layer doping of $10^{15}\,cm^{-3}$. The measured thermal spreading resistance $R_{TH}$ was 70 K/W. The device was packaged in a 14 pin plastic DIP whose chip-to-ambient thermal resistance was 110 K/W. The measurements and the simulations were both arranged to include only the thermal spreading resistance. Fig. 2 shows measured and simulated variation of $g_{12}$ for the same transistor. In this case, an HP 4145 parameter analyser set to its maximum integration time was used to make the measurement. As discussed previously, this causes the package thermal impedance to contribute a component to the effective value of $R_{TH}$. $R_{TH}$ was raised to 90 K/W in the simulation to account for this effect.

The measurements and simulations in both Figures agree well over many decades of current. The differences at high

currents could be due to effects of parasitic emitter resistance or errors in the models for $D_C$ and $D_B$ at these current levels.

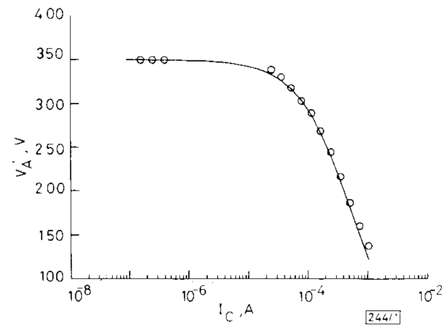


**Fig. 1** *Measured and simulated normalised output resistance $V_A = I_C/g_{22} - V_{CE}$ for 23 × 23 μm² BJT*

$R_{TH} = 70$ K/W
○ measurement
——— simulation

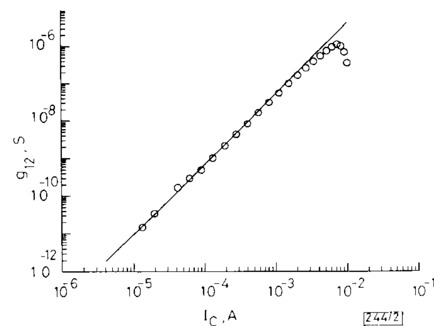


**Fig. 2** *Measured and simulated reverse transfer conductance $g_{12}$ for 23 × 23 μm² BJT*

Simulation used $R_{TH} = 90$ K/W to account for package thermal impedance affecting measurement
○ measurement
——— simulation

Note that SPICE models predict a constant value (VAF) for normalised output resistance and zero or very small negative value for $g_{12}$. The much larger positive value for $g_{12}$ seen here is important because it makes the input impedance depend strongly on loading conditions at the opposite port.

Similar agreements between measured and simulated small-signal parameters have been seen with many other transistors. Of special interest is the high thermal spreading resistance seen with dielectrically isolated BJTs. Such transistors are isolated from the silicon substrate by a layer of silicon dioxide, whose thermal conductivity is only 1% of that for silicon. The $R_{TH}$ of a 23 × 23 μm² dielectrically isolated transistor was found to be 280 K/W, four times that of the similar-size junction-isolated transistor previously described.

*Conclusion:* Modelling of thermal spreading impedance is expected to become increasingly important in circuit and device simulation as transistor geometries are scaled down and current densities rise. This Letter presents a practical way to extract thermal spreading resistance of BJTs separately from package thermal impedance. This technique will be especially useful for modelling of devices whose unusual geometries or structures (such as dielectric isolation) make analytical modelling of thermal impedance impractical.

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## VERTICALLY COMPACT 15 GHz GaAs/AlGaAs MULTIPLE QUANTUM WELL LASER GROWN BY MOLECULAR BEAM EPITAXY

*Indexing terms: Semiconductor lasers, Lasers*

A GaAs/$Al_xGa_{1-x}As$ multiple quantum well laser with an electrical modulation bandwidth exceeding 15 GHz has been fabricated. Optimised design of the waveguide, including development of high Al mole fraction ($x = 0{\cdot}8$) cladding layers, together with a coplanar electrode geometry, has resulted in a vertically compact laser structure suitable for integration.

The monolithic integration of high-speed heterostructure lasers and fast photodetectors with GaAs-based driver and receiver electronics is seen as a promising technology for short range data transmission. The design and performance requirements of the lasers include a vertically compact design and a large modulation bandwidth. To date, metal organic chemical vapour deposition (MOCVD)-grown GaAs/$Al_xGa_{1-x}As$ multiple quantum well (MQW) lasers with $Al_{0.55}Ga_{0.45}As$ cladding layers have been reported with 3 dB (optical) modulation bandwidths of up to 14 GHz.[1] This work demonstrates molecular beam epitaxy (MBE)-grown GaAs/AlGaAs MQW lasers with 3 dB electrical modulation bandwidths up to 15·1 GHz (16·7 GHz 3 dB optical bandwidth); electrical modulation bandwidth is a more common figure of merit for transmission systems. The structure has been optimised for both high speed and minimal total epilayer thickness, easing future monolithic integration with electronic circuitry.

The key to achieving this level of performance was the use of $Al_xGa_{1-x}As$ cladding layers with $x = 0{\cdot}8$. Employing such a high Al mole fraction allowed an increase of confinement factor Γ, leading both to an increase in resonance frequency and a substantial decrease in core and cladding layer thicknesses. As may be seen from the theoretically predicted variation of the confinement factor Γ with core width presented in Fig. 1, increasing the effective aluminium mole fraction from