A Low-Phase Noise LC-QVCO in CMOS Technology

Hyoung Chul Choi, So Bong Shin, and Sang-Gug Lee

***Abstract*—This letter presents a source-injection parallel coupled (SIPC) quadrature voltage-controlled oscillator (QVCO) topology. In the proposed SIPC-QVCO, compare to the conventional parallel-coupled LC-QVCO (P-QVCO), the coupling transistors are configured in a way so that the $1/f$ noise, contributed by the coupling transistors at the output, can be avoided. The newly proposed SIPC-QVCO and conventional P-QVCO are fabricated based on 0.25 μm CMOS technology. The phase noise of SIPC-QVCO measured at 1.5 GHz shows more than 10 dB improvement than that of the conventional P-QVCO over the offset frequency range of 10 K $\sim$ 1 MHz while dissipating the same amount of power.**

***Index Terms*—$1/f$ noise up-conversion, complementary metal oxide semiconductor (CMOS), phase noise, quadrature voltage-controlled oscillator (QVCO), RF, source-injection parallel coupled quadrature VCO (SIPC-QVCO).**

I. Introduction

THE QUADRATURE LO signal is a key element in many of the direct conversion transceivers which tend to dominate today's wireless communication technology. Since the introduction of the parallel-coupled LC-quadrature voltage-controlled oscillator (QVCO) (P-QVCO) topology, which was proposed by Rofougaran [1], it has become one of the most commonly used topology for the quadrature signal generation. Recently, Andreani [2] reported a series-coupled LC-QVCO topology (S-QVCO) that exhibits improvement in phase noise compare to the P-QVCO. However, the S-QVCO has disadvantage in the low supply voltage application, which is one of the major trends in concurrent technologies, due to the stack of the coupling transistors in series with the cross-coupled transistors of the differential VCO. In this letter, a source-injection parallel-coupled LC-QVCO (SIPC-QVCO) topology is proposed as a low voltage and low phase noise QVCO.

II. Design of the QVCO

A. SIPC-QVCO Topology Description

Fig. 1 shows the schematic of the proposed SIPC-QVCO topology. As shown in Fig. 1, the SIPC-QVCO consists of two LC-tuned differential VCOs and four coupling transistors. Note that, contrary to the conventional P-QVCO, the drain nodes of the coupling transistors ($M_5 \sim M_8$) are connected directly to the supply voltage ($V_{\rm DD}$). In P-QVCO, the drain nodes of coupling transistors are tied to the LC-tank.

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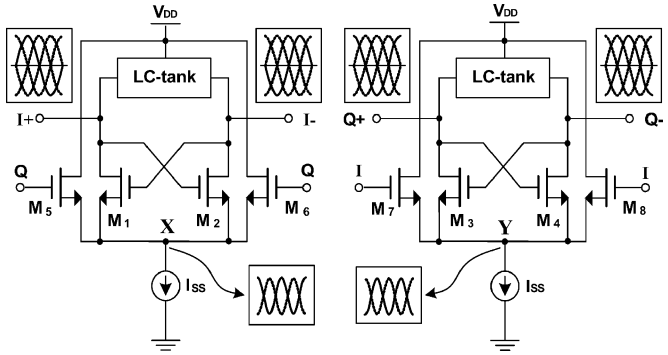

Fig. 1. Proposed SIPC-QVCO schematic.

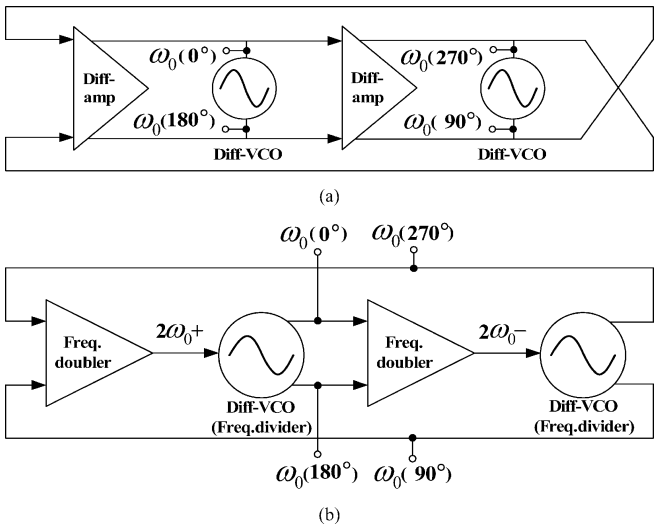

Fig. 2. Block diagram of (a) the conventional P-QVCO and (b) SIPC-QVCO.

B. Mechanism of Quadrature Signal Generation

The schematic of the SIPC-QVCO might seem like a minor modification from the conventional P-QVCO. However, the mechanism for quadrature signal generation is fundamentally modified. Fig. 2(a) and (b) represent the P-QVCO and SIPC-QVCO as a combination of functional block diagrams. As can be seen in Fig. 2(a), the quadrature output signals in P-QVCO are generated by the combination of two differential-VCOs and the cascade of two differential amplifiers (implemented as coupling transistors) with one of them in cross-connection. In Fig. 2(b), the simplified block diagram of the SIPC-QVCO is constructed as an alternating combination of two differential-VCOs and two frequency-doublers. The cross-coupled differential-VCOs in Fig. 2(b) operate as frequency divider for the signals injected at the common source

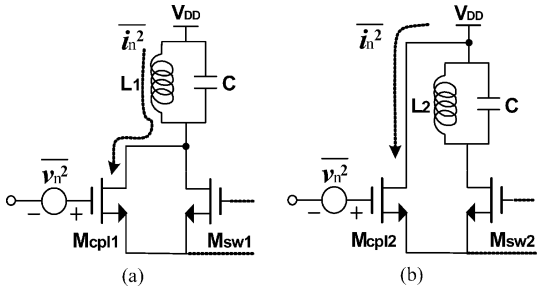

Fig. 3. Switching and coupling transistors and the LC-tanks for (a) the conventional P-QVCO and (b) the SIPC-QVCO.

nodes (X, Y Fig. 1) to the outputs [3]. The coupling transistor pairs M_5/M_6 and M_7/M_8 are configured as differential voltage buffer, but operate as frequency doubler at the output nodes X and Y with large input voltage swing. As shown in Figs. 1 and 2(b), through the frequency division and doubling procedure, a differential signal at the frequency of $2\omega_{\rm o}$ is generated at the common-source nodes X and Y of the two differential-VCOs. As described in [4], if two oscillators are injected by 2-s harmonics with a phase shift of 180°, their fundamental output will be in quadrature. In the SIPC-QVCO, the differential $2\omega_{\rm o}$ signals applied at the common-source nodes of the two differential-VCOs lead to interlocked quadrature signals with frequency of $\omega_{\rm o}$ at the outputs.

III. Phase Noise Analysis and Measurement Results

A. Phase Noise Analysis

To understand the advantage of the SIPC-QVCO in phase noise, Fig. 3 compares some parts SIPC-QVCO with P-QVCO : the switching and coupling transistors and the LC-tanks. In Fig. 3 $\overline{v_n^2}$ represents the low frequency $1/f$ noise of the coupling transistors modeled as a voltage source in series with the gate [5] and $\overline{i_n^2}$ represents the resulting noise current in the drain. In the case of conventional P-QVCO shown in Fig. 3(a), when the coupling transistor $M_{\rm cpl1}$ is in saturation, the resulting $1/f$ noise current $\overline{i_n^2}$ flows through the inductor L_1. Since the inductor impedance at low frequencies is small, the voltage drop across the LC-tank by $\overline{i_n^2}$ is insignificant. However, when the coupling transistor turns off, the abrupt change in the noise current leads to a voltage induction across the inductor L_1, in proportion to the value of L_1 and the time derivative, which could be a significant amount. Therefore, the switching operation of the coupling transistors effectively up-converts the $1/f$ noise to the frequency of oscillation leading to phase noise degradation. This is the main reason for the degradation of the inferior phase noise performance in P-QVCO compare to that of the core differential-VCO.

In comparison, with the SIPC-QVCO, the $1/f$ noise of the coupling transistor contributes no voltage induction across the LC-tank since the drain of the coupling transistors are directly connected to the supply voltage as shown in Fig. 3(b).

Note that the separation of the coupling transistors from the LC-tuning circuits helps to obtain wider tuning range as parasitic capacitances of the coupling transistors are separated [6].

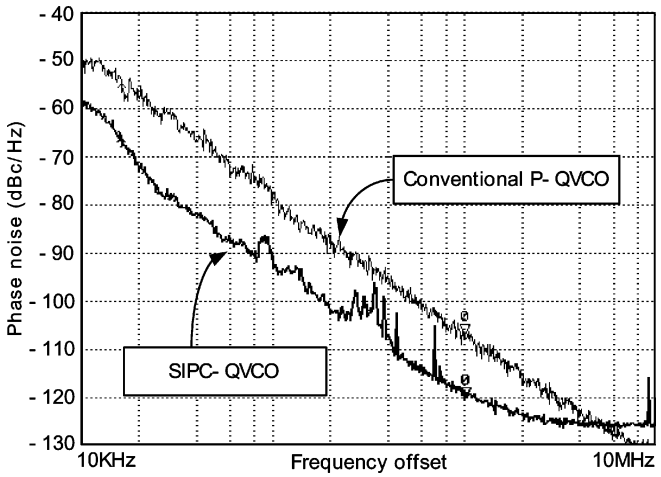

Fig. 4. Measured phase noise performances of the P- and SIPC-QVCOs.

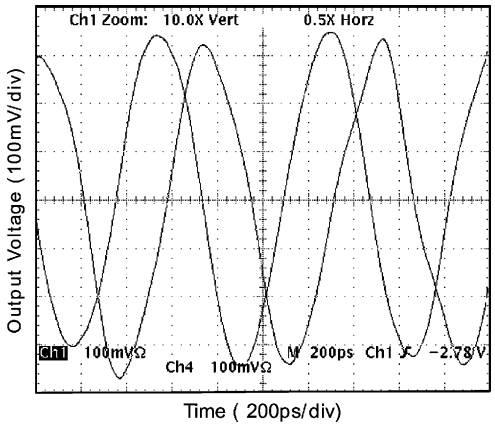

Fig. 5. Measured time-domain outputs of SIPC-QVCO.

B. Measurement Results

The proposed SIPC-QVCO and the conventional P-QVCO have been implemented with a 0.25 μm CMOS technology. For the fair comparison, both QVCOs adopted same active and passive component sizes and biased to dissipate the same total dc current of 16 mA from 1.8-V supply. Both QVCOs are measured at the same frequency of 1.5 GHz by the small adjustments in the control voltage of the varactor. Fig. 4 compares the phase noise performance of the two QVCOs. As can be seen in Fig. 4, over the offset frequency ranges of 10 K $\sim$ 1 MHz, SIPC-QVCO shows more than 10-dB superior phase noise performance compare to that of the conventional P-QVCO. The measured phase noise of the two QVCOs shows $3 \sim 5$ dB higher values compare to what was predicted by the simulation [7]. However, the amount of improvement in the measured phase noise of the SIPC-QVCO agrees with the simulation. The measured output power level of each quadrature signal was 0 dBm. Fig. 5 shows the measured time domain I+ and Q+ signal operating at 1.4 GHz. Fig. 6 shows the microphotograph of the fabricated SIPC-QVCO chip.

IV. Conclusion

A new QVCO topology has been proposed. In the proposed QVCO, the contribution of the $1/f$ noise induced by the cou-

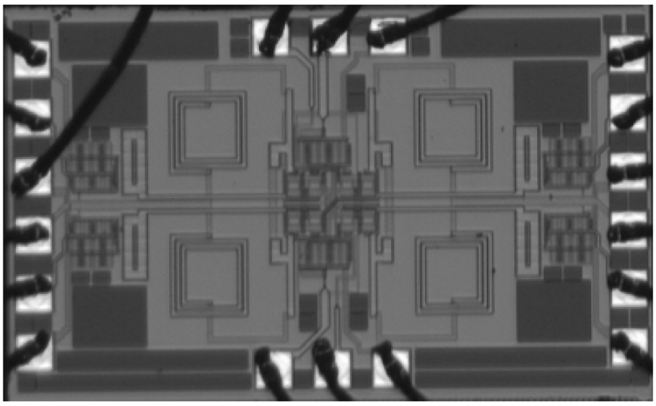

Fig. 6. Die microphotograph of the SIPC-QVCO.

pling transistors is removed from the output by diverting the drain connections of the coupling transistors to an ac ground. The operational principle of the proposed SIPC-QVCO is provided. A new explanation for the phase noise degradation by the $1/f$ noise of the switching and coupling transistors, in the conventional P-QVCO, is introduced. The improvement in the phase noise of the proposed SIPC-QVOC is explained by the same principle. The proposed SIPC-QVCO and the conventional P-QVCO have been implemented with a 0.25 μm CMOS technology. The phase noise of SIPC-QVCO measured at 1.5 GHz shows more than 10 dB improvement than that of the conventional P-QVCO over the offset frequency range of 10 K $\sim$ 1 MHz while dissipating the same amount of power. The improvement in phase noise agrees with simulation results.

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