An Inductance Enhancement Technique and Its Application to a Shunt-Peaked 2.5 Gb/s Transimpedance Amplifier Design

Yong-Hun Oh and Sang-Gug Lee

***Abstract*—This brief presents a bandwidth enhancement technique that is applicable to gigahertz-range broadband circuits. Using the inductance enhancement technique proposed in this brief, a 2.5-Gb/s transimpedance amplifier (TIA) has been implemented based on a 0.35-μm CMOS technology. With the input noise reduction, the TIA with the proposed active inductor loads improves the overall system performances including more that 90% increase in bandwidth. Measurements show the bandwidth of 1.73 GHz, transimpedance gain of 68 dBΩ, and the averaged input referred noise current of 3.3 pA$/\sqrt{\text{Hz}}$, respectively, while dissipating 50 mW of dc power.**

***Index Terms*—Active inductors, bandwidth extension, shunt-peaking, transimpedance amplifier (TIA).**

I. Introduction

With the explosive growth in the commercial wireless telecommunication market, silicon technology is actively used as it can satisfy the demands for low-cost and high integration [1]. Thanks to the continuous scaling of MOS transistors, the standard CMOS became a feasible technology for gigahertz range analog applications that were traditionally dominated by the more expensive technologies such as Si/SiGe bipolar and BiCMOS or the GaAs technologies. Still, the design of high-speed CMOS circuits involves many difficulties to overcome. For applications like high data rate optoelectronic integrated circuits (OEICs), the amplifiers tend to require wideband characteristics with high amount of gain. However, the poor transconductance of the MOS transistors mandates higher amount of load resistor with broadband amplifier design while the large load resistor leads to poor bandwidth.

Many efforts to obtain the increased bandwidth were introduced [2]. One of the commonly used techniques to increase the bandwidth is the inductive shunt peaking. This technique can simply be implemented using an inductor in series with load resistor to the common-source or cascode amplifier. Typically for a given technology, obtaining wider bandwidth tends to require higher power dissipation. An attractive feature of shunt peaking technique is that the bandwidth enhancement comes without additional power dissipation. However, as will be discussed in more detail in Section II, the conventional inductive shunt peaking technique is not very efficient under high value load resistance or low frequency applications (1–2 GHz range) as the amount of the required inductance is unrealistically large. To solve this limitation, in this brief, a variation of the shunt peaking technique is proposed.

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II. Broadband Amplifier Design

To extend the bandwidth of an amplifier, it is important to identify the key component that is responsible for the bandwidth limitation. In order to have a wideband characteristic, an amplifier should have no low frequency pole along the signal path. In addition to this time constant approach, for the given amplifier in order to improve the bandwidth, the inductive shunt peaking technique is generally applied, which is well explained elsewhere [2]. However, in order to identify the issues in applying the inductive shunt peaking technique and propose its alternative, a part of the work done by [2] will be repeated below. In the common-source amplifier, we assume that a single dominant pole composed of the load resistor R_L and the parasitic load capacitance (call it C_{eff}) determines the frequency response of the amplifier. As shown in (1), with the simple shunt-peaked common-source amplifier, Mohan [2] summarized the relationship between the amount of peaking, expressed by m, and the required inductance L

$$m = \frac{\frac{L}{R_L}}{R_L C_{\text{eff}}}. \tag{1}$$

Note that the factor m in (1) includes the information about the original bandwidth without the inductive peaking $R_L C_{\text{eff}}$. For the given load resistor R_L and the amount of peaking, the wider the original bandwidth (or the smaller $R_L C_{\text{eff}}$) the smaller necessary peaking inductance. Extending the discussion to amplifiers with the bandwidth of 1–2-GHz range, the necessary inductance has to be very large unless C_{eff} is very large and/or R_L is very small. However, considering the gain requirement, R_L is expected to be large due to the poor transconductance of the CMOS technology. Furthermore, large C_{eff} in wideband amplifier doesn't seem like a reasonable assumption, which is typically the case. As an example, with $C_{\text{eff}} = 0.2$ pF and $R_L = 1$ kΩ, the original -3-dB bandwidth is approximately 800 MHz. In this case, the shunt peaking with optimum amount of group delay ($m = 0.32$) can extend the bandwidth to 1.3 GHz. However, the required inductance from (1) has to be 64 nH. This size inductor is generally impractical as an on-chip implementation

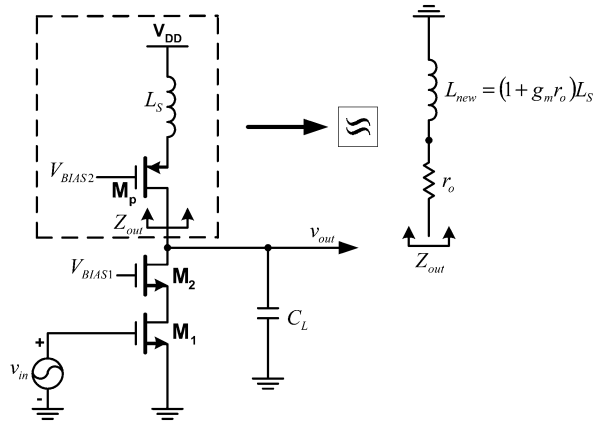

Fig. 1. Shunt peaked cascode amplifier with the proposed inductor load and its small-signal equivalent representation.

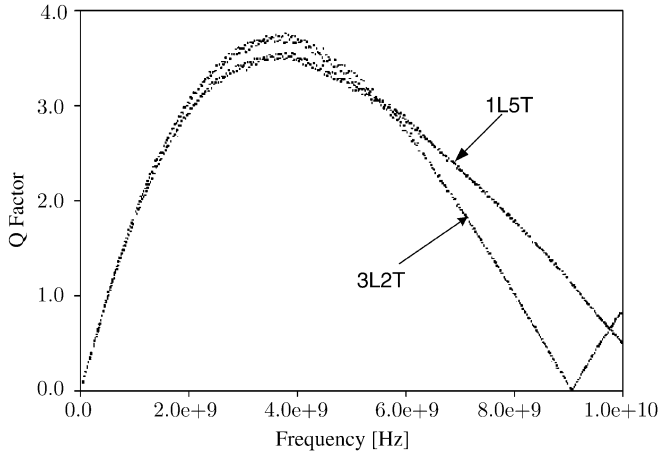

Fig. 2. Measured quality factor versus frequency of a single-level five-turn (2.6 nH) and a triple-level two-turn (3.3 nH) inductor.

due to the low self-resonance frequency. Above discussion tells us that the conventional inductive shunt peaking technique tends to be ineffective below 5 GHz unless R_L is small. In Section III, a variation of shunt-peaking adapting inductance amplification technique is proposed that can make the conventional shunt peaking technique effective at frequencies below 5 GHz.

III. Bandwidth Extension With Inductance Enhancements

Fig. 1 shows a variation of the shunt-peaking topology using a current-source with inductive source degeneration. By applying the elementary level circuit analysis technique, the output impedance of the current-source Z_{out} is given by

$$Z_{\text{out}}(s) = \frac{v_x}{i_x} = r_o + j2\pi f L_s (1 + G_m r_o) \tag{2}$$

where v_x and i_x are the test voltage and current, r_o the load resistance of transistor M_p, and G_m the overall transconductance of the cascode amplifier stage, respectively. Even though it is no surprise that the degeneration boosts the output impedance of a current source, it can be very interesting when we consider (2) as a load impedance of the shunt-peaked amplifier composed of inductor $(L_{\text{new}} = L_s(1 + G_m r_o))$ in series with load resistor (r_o), as shown in Fig. 1.

In a conventional shunt peaked cascode amplifier with a resistive load, the maximum value of output resistor is being limited by the voltage drop across the resistor. In Fig. 1, however, by using the active load, the suggested topology can provide a higher voltage gain. As discussed earlier, for wideband application higher load resistance mandates larger inductance, but the proposed topology solves this issue by the inductance amplification as explained above.

Note that in Fig. 1, it is expected that the parasitic gate–source capacitance of M_p leads to resonance. More accurately, including the gate–source capacitance C_{gs} of the active load, (2) can be expressed as

$$Z_{\text{out}}(s) = \frac{v_x}{i_x} = r_o + \frac{1 + G_m r_o}{1 - (2\pi f)^2 C_{\text{gs}} L_S} j2\pi f L_S. \tag{3}$$

Equation (3) can be approximated to (2) when $f^2 \ll 1/4\pi^2 C_{\text{gs}} L_S$. Therefore, the proposed topology should be used with care so that the parasitic capacitance does not turn the load impedance into capacitive value at the frequency of interest. Now, by applying (2) to (1), the relationship between the amount of peaking and required inductance of the shunt peaked amplifier can be represented as

$$m = \frac{\frac{L_{\text{new}}}{r_o}}{r_o C_L} = \frac{\frac{(1+G_m r_o) L_S}{r_o}}{r_o C_L} \tag{4}$$

where L_{new} represents the effective inductance of the active load given by $(1 + G_m r_o) L_S$. Comparing (4) with (1), for the same amount of peaking and assuming r_o and C_L are equal to R_L and C_{eff}, respectively, a much smaller sized inductor L_S is required with shunt peaked amplifier shown in Fig. 1 in comparison with the conventional shunt-peaked amplifier.

A. On-Chip Inductor Design

On-chip spiral inductors are an important performance-limiting component in monolithic gigahertz RF circuits such as voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), and passive filters. Countless numbers of research articles have been reported that introduces various techniques to improve the quality factor. However, with the shunt peaking application, the quality factor is not the primary issue as the inductor will be in series with the load resistor anyway. It is the area efficiency that matters more. As a monolithically implementable structure, the multilevel spiral structure is an efficient technique to improve the area efficiency [3], [4]. Both of the works, [3], [4], are effectively the same as far as the obtainable amount of inductance for the given number of metal-levels and turns. In this work, however, the implemented on-chip spiral inductor is designed according to Merrill's approach [3] in order to get a much higher self-resonance frequency. This is confirmed by [5], and based on these insights many 3-level square spiral inductors have been fabricated and evaluated.

Fig. 2 compares the quality factor of a conventional single-level 5-turn (2.6 nH) and a three-level two-turn (3.3 nH) inductors as a function of frequency. As can be seen from Fig. 2, the measured quality factor and resonant frequency of these two inductors are not much different, yet the multilevel inductor occupies only 1/3 of the area of single-level inductor, with a big area advantage.

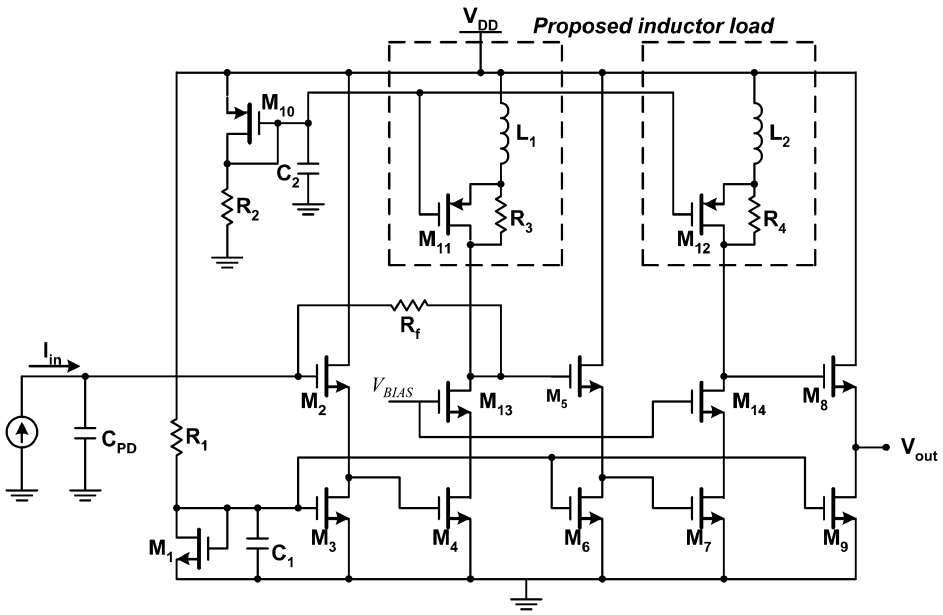

Fig. 3. Simplified schematic of the TIA designed for 2.5-Gb/s application.

IV. Transimpedance Amplifier Design and Measurement Results

The TIA is one of the key components in optical receiver dominating the gain, bandwidth, and noise performances. Fig. 3 shows the simplified schematic of the TIA designed for 2.5 Gb/s application. The TIA in Fig. 3 basically adopts the broadband cascode topology except the proposed inductance enhancement shunt peaking as loads.

In Fig. 3, the 500-Ω resistors, R_3 and R_4, are added to reduce the output resistance of the current source and control the amount of inductance amplification, as well as stabilizing the dc drain voltages of transistor M_{13} and M_{14}. The resistor $R_f(2\ \mathrm{k}\Omega)$ is the shunt feedback resistor that makes transimpedance and reduces the input impedance of the amplifier. The last buffer, composed of M_8 and M_9, is designed to provide 50 Ω output impedance matching. The capacitors C_1 and C_2 provide ac ground path to the gate nodes of the current sources and active loads, as well as reducing the inter-stage coupling and increasing output impedance of the current source at high frequencies. The rests are the biasing circuits. The inductors L_1 and L_2 are the 3-level, 4-turn square spiral inductors that provide 15.3 nH with 10-μm width and 1-μm spacing while occupying $136 \times 136\ \mu\mathrm{m}^2$. For the simulation, as shown in Fig. 3, the photodiode is modeled by a simple current source in parallel with capacitance. Each part of the cascode stage and source follower as a buffer has been designed to have 20-dB and -2-dB gain, respectively.

Fig. 4 shows the simulated transimpedance versus frequency for photodiode capacitances (C_{PD}) varying from 600 fF to 1.2 pF. As can be seen, the 3-dB bandwidth is above 1.5 GHz assuming maximum photodiode capacitance $(C_{\mathrm{PD}} = 1.2\ \mathrm{pF})$. And it is above 1.9 GHz with a typical value of photodiode capacitance $(C_{\mathrm{PD}} = 600\ \mathrm{fF})$ for a 2.5-Gb/s application. Based on the 0.35-μm CMOS technology under the same amount of gain, the common-source topology with resistive load has the

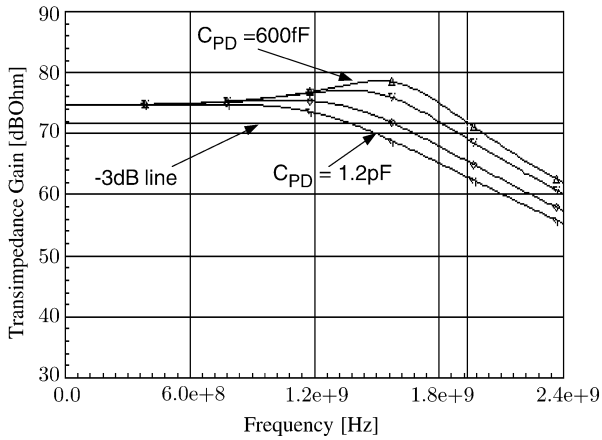

Fig. 4. Simulated transimpednace versus frequency for variable photodiode capacitances from 600 fF to 1.2 pF with 200 fF steps.

bandwidth of at most 650 MHz and cascode topology extends it near to 1 GHz. However, in this condition, applying conventional shunt-peaking with 15-nH inductor is no more effect on the bandwidth extension. As a result, the overall bandwidth of the TIA with the proposed inductor loads is extended even more than 90%.

In order to evaluate the performances of the TIA as shown in Fig. 3, the TIA has been implemented with 0.35-μm CMOS technology and measured with the method introduced by Razavi [6]. The chip microphotograph of the fabricated TIA is shown in Fig. 5. The overall chip area is 0.6 mm^2 and it dissipates about 50 mW with a 3.3-V of supply. As can be seen from Fig. 5, the effective chip area could be reduced significantly thanks to the proposed inductance enhancement shunt-peaking and multilevel implementation of the on-chip spiral inductors.

Fig. 6 shows the measured transimpedance gain versus frequency response of the TIA. As can be seen, the TIA shows 68 dBΩ of transimpedance gain with 1.73 GHz of 3-dB bandwidth. Fig. 7 shows the output impedance as a function of fre-

TABLE I
PERFORMANCE COMPARISON OF SEVERAL TIAS

Specifications	This work	Design in [2]	Design in [7]
Data rate	2.5 Gb/s	2.125 Gb/s	2.4 Gb/s
Transimpedance gain	68 dBΩ	64.1 dBΩ	59 dBΩ
Bandwidth	1.73 GHz @ 0.6 pF	1.2 GHz @ 0.6 pF	1.9 GHz @ 0.3 pF
Spectral current noise	3.3 pA/√Hz	0.6 μA (Sim.)	9.75 pA/√Hz
Output matching	Less than –15 dB	–	–
Power dissipation	~ 50 mW	115 mW	104 mW
Chip size	0.6 mm^2	0.6 mm^2	–
Technology	0.35 μm CMOS	0.5 μm CMOS	0.15 μm CMOS

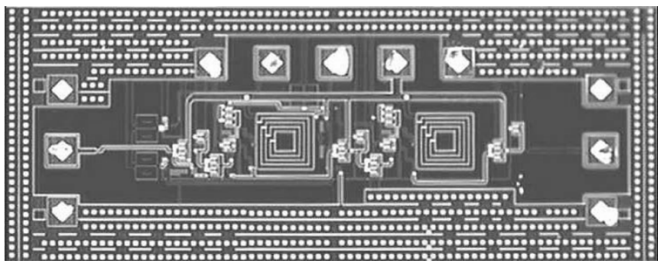

Fig. 5. Microphotograph of the fabricated TIA chip.

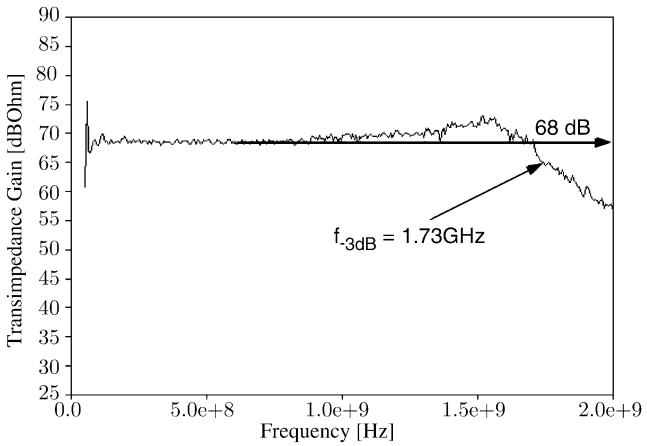

Fig. 6. Measured transimpedance gain versus frequency of the TIA.

quency where more than 15 dB return loss is obtained up to the 3-dB frequency of the designed TIA.

As shown in Fig. 8, the averaged spectral noise current density of the implemented TIA is about 3.3 pA/$\sqrt{}$Hz for the frequency up to 1.8 GHz. As can be seen in Fig. 8, the input referred noise current density seems to be relatively flat over frequency. This is another advantage of the proposed active inductor load. The additional inductor load proposed in this work can be reduce the noise contribution generated by the load transistor at high frequency without reducing the dc current in the input transistor. The input-referred noise spectral density of the proposed active inductor load can be represented by

$$\overline{i_L^2} = 4kT\gamma g_{mp}\frac{1}{\sqrt{1+(g_{mp}2\pi f L_S)^2}} \tag{5}$$

where g_{mp} is the transconductance of the current source transistor M_p shown in Fig. 1. Finally, Table I summarizes the overall performances of this work and compares the performance of several TIA's reported in References with this work.

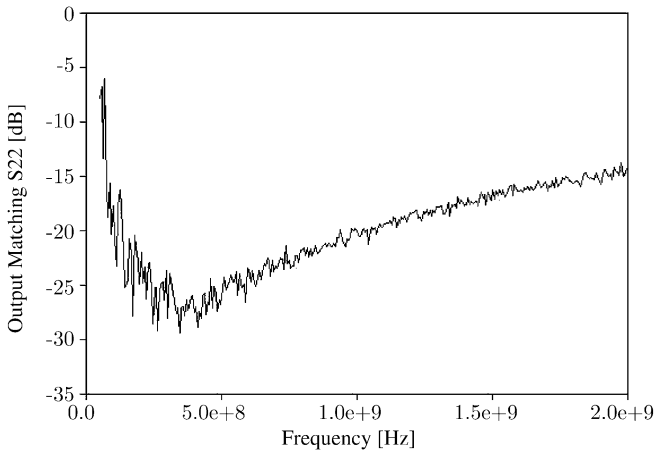

Fig. 7. Measured output impedance versus frequency of the TIA.

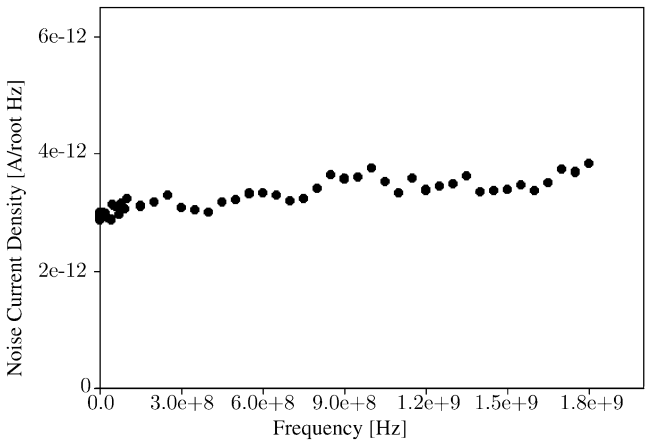

Fig. 8. Measured input referred noise current density versus frequency.

V. SUMMARY

This brief presents a novel shunt peaking technique that is applicable broadband amplifiers with the bandwidth of 1–2-GHz range. Using the inductance enhancement technique, while applying the well-known inductive shunt peaking, the bandwidth of the broadband amplifiers can be extended with much smaller amount of inductances by the inductance amplification principle. The proposed active inductor load, in this brief, allows amplifiers with high yet flexible gain and wide bandwidth at the same time. Another added advantage of the proposed inductor load is to result in a reduction in the noise generated by the input stage of the amplifier.

In order to confirm the bandwidth extension effects on a circuit with the proposed inductor load, a 2.5 Gb/s transimpedance amplifier (TIA) has been implemented based on 0.35-μm CMOS technology. The overall bandwidth of the TIA with the proposed inductor loads is improved more than 90% compared with that of conventional shunt-peaked TIA. The measured transimpedance gain, bandwidth, input referred noise current, and the output matching are 68 dBΩ, 1.73 GHz, 3.3 pA$/\sqrt{\text{Hz}}$, and greater than 15 dB, respectively, while dissipating 50 mW of dc power from a 3.3-V supply.

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