# Image-Rejection CMOS Low-Noise Amplifier Design Optimization Techniques

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***Abstract*—This paper reviews and analyzes two reported image-rejection (IR) low-noise amplifier (LNA) design techniques based on CMOS technology, i.e., the second-order active notch filer and third-order passive notch filter. The analyses and discussions are based on the quality factor of filters and the ability of the frequency control. As the solution to deal with the suitable on-chip filter, this paper proposes a new notch-filter topology that can overcome the limitations of the two previous reported studies. In addition, the LNA design method satisfying the power-cons-trained simultaneous noise and input matching, as well as the linearity optimization conditions is introduced. By using the proposed notch filter and proposed design methodology, an IR LNA used in the superheterodyne architecture is implemented. The proposed IR LNA, designed based on 0.18-$\mu$m CMOS technology with total current dissipation of 4 mA under 3-V supply voltage, is optimized for a 5.25-GHz wireless local area network with IF frequency of 500-MHz applications. The measurement results show 20.5-dB power gain, lower than 1.5-dB noise figure, −5-dBm input-referred third-order intercept point and an IR of 26 dB.**

***Index Terms*—CMOS, image-rejection (IR) technique, low-noise amplifier (LNA), noise optimization, RF, wireless local area network (WLAN).**

## I. Introduction

GENERALLY, superheterodyne architecture is the most widely used for stage-of-the-art receivers in modern handsets since it is capable of providing high and stable performance in mobile communications [1]–[3]. In the superheterodyne receivers, proper filtering of image signals is mandatory, and this filtering is done by external passive components such as surface-acoustic wave (SAW) filters. These external filters are large and expensive, but unavoidable in superheterodyne architectures. Consequently, they are the major impediment to increase the level of integration of wireless radio since they cannot be easily implemented monolithically. To overcome the problems from those external filters, image-rejection (IR) mixers using phase cancellation are developed [4]–[8]. However, due to the gain and phase mismatches, IR ratios for 5-GHz-band receivers generally lie within the range of 25–35 dB [3]. Therefore, an extra 50-dB IR should be provided to meet the specification of a superheterodyne receiver, which typically requires 80 dB of IR. To address this need, some of the recent research has focused on the development of monolithic IR using a notch filter [9]–[14]. In this technique, a notch located at the image frequency is used to reject image signals rather than bandpass filtering. By combining an on-chip IR filter with an integrated image reject mixer, 79 dB of on-chip IR could be obtained [14].

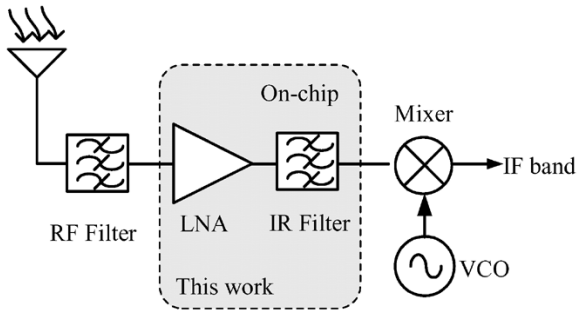


Fig. 1. Typical superheterodyne receiver.

In this paper, two previously reported IR low-noise amplifier (LNA) design techniques are reviewed and analyzed. The analyses and discussions are based on the quality factor and the ability to control frequencies at both image and wanted signals. As a solution to overcome the limitations of two previously reported works, this paper proposes a new notch-filter topology—the third-order active notch filter. In other words, the proposed topology can not only control both the image signal and wanted signal, but can also obtain a high-quality factor regarding the low-quality factor of an on-chip inductor.

In addition, this paper shows the guideline as to how to design an LNA that achieves power-constrained simultaneous noise and input matching, as well as satisfies the linearization condition. By combining a low-noise high-gain LNA designed by the proposed optimization technique with the proposed notch filter, an IR LNA, shown in Fig. 1, is implemented. The proposed IR LNA is optimized for superheterodyne applications having 5.25 GHz with IF frequency of 500 MHz. The measurement results show the power gain of 20.5 dB, lower than 1.5-dB noise figure (NF), and an IR of 26 dB. Measured two-tone test results show −5 and −8 dBm of the input-referred third-order intercept point (IIP3) in the cases of using and not using the notch filter, respectively. The circuits dissipate a dc current of 4 mA under a supply voltage of 3 V. Section II summarizes the reported analysis details of two reported IR design techniques

Manuscript received April 21, 2004.

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Digital Object Identifier 10.1109/TMTT.2004.840744

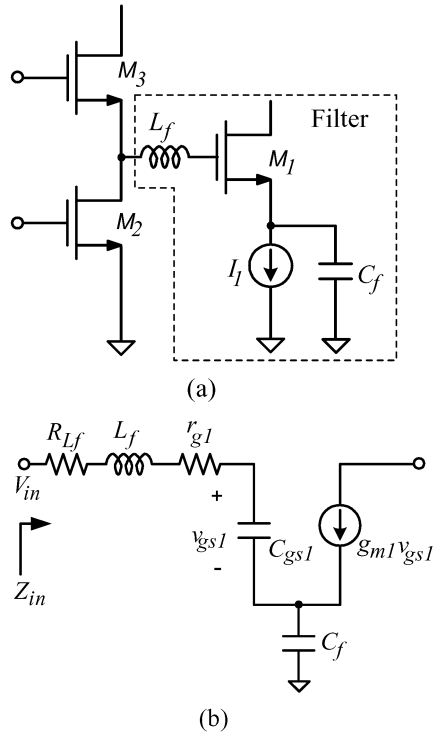


Fig. 2. (a) Schematic of the IR LNA with second-order active notch filter. (b) The filter's small-signal equivalent circuit only.

along with the proposed filter topology. Sections III and IV describe the design and measurement details of the proposed IR LNA. Section IV concludes this study.

## II. IR Design Techniques

### A. Second-Order Active Notch-Filter Technique

The on-chip IR LNA with the second-order active filter was first introduced in [9]. This active notch filter is based on a series resonator, whose resonant frequency is tuned to the image frequency. Fig. 2(a) shows the cascode LNA with the second-order active filter is attached, and Fig. 2(b) shows only the small-signal equivalent circuit of the filter.

From Fig. 2(b), the impedance looking into the gate of $M_1$ is given by

$$Z_{\text{in}} = j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{\text{gs1}}} + \frac{1}{C_f}\right) - \frac{g_{m1}}{\omega^2 C_{\text{gs1}} C_f} + R_{Lf} + r_{g1} \tag{1}$$

where $C_{\text{gs1}}$ is the gate–source capacitor $g_{m1}$ transconductance, $r_{g1}$ is the series gate resistance of $M_1$, and $R_{Lf}$ is the series resistance of on-chip inductor $L_f$.

Note that the negative term on the right-hand side of (1) represents the negative resistance (proportional to $g_{m1}$) seen at the gate of transistor $M_1$. Thus, by adjusting $g_{m1}$, i.e., the bias current $I_1$, sufficient negative resistance can be generated to cancel out $R_{Lf}$ and $r_{g1}$. This results in a dramatic increase in the quality factor $Q$ of the filter to very high values [9]. Therefore, the quality factor of the on-chip integrated inductor plays a minor role in the quality factor of the filter, which is given by

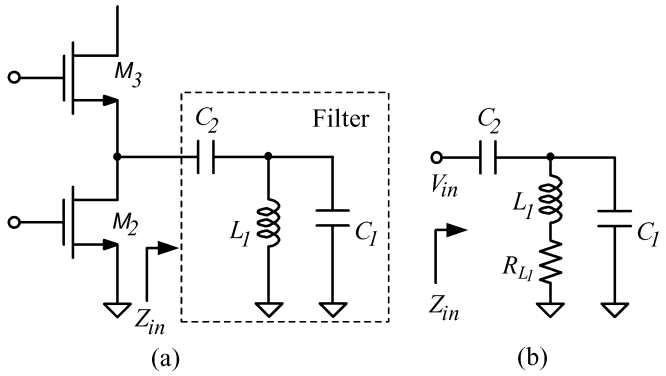


Fig. 3. (a) Schematic of the IR LNA with the third-order passive notch filter. (b) The filter's equivalent circuit including the series resistance of the on-chip inductor only.

$$Q = \frac{\left(\dfrac{L_f}{C_{\text{gs1}}} + C_f\right)^{1/2}}{R - \left(g_m/\omega^2 C_{\text{gs1}} C_f\right)} \tag{2}$$

where $R = R_{Lf} + r_{g1}$ represents the total resistance.

The frequency of resonance $f_o$ for the filter can be derived as

$$f_o = \frac{1}{2\pi\sqrt{L\left(\dfrac{C_{\text{gs1}} C_f}{C_{\text{gs1}} + C_f}\right)}}. \tag{3}$$

At this frequency, $Z_{\text{in}}$ is minimum, with the value depending on the quality factor of the filter. However, this notch filer can work negatively to the wanted signal. That means, at the wanted frequency, the input impedance of the second-order active notch filter might be lower than the case without the filter. Therefore, it is possible that there is some amount of wanted signal that can be lost to the ground. Consequently, the power gain of the amplifier can be degraded, while the NF can be increased due to the signal loss to the ground.

### B. Third-Order Passive Notch-Filter Technique

The cascode LNA with the third-order passive notch filter noted in Fig. 3(a) is introduced in [10] as the solution to control both the image and wanted signal. From Fig. 3(a), the input impedance of the filter is given by

$$Z_{\text{in}} = \frac{L_1 \cdot (C_1 + C_2)\, s^2 + 1}{C_1 C_2 \cdot L_1 \cdot s^3 + C_2 \cdot s}. \tag{4}$$

The image and wanted signals are located at

$$f_{\text{im}} = \pm\frac{1}{2\pi\sqrt{L_1 \cdot (C_1 + C_2)}} \tag{5}$$

$$f_{\text{wanted}} = \pm\frac{1}{2\pi\sqrt{L_1 \cdot C_1}}. \tag{6}$$

The filter can provide low impedance at the image frequency and high impedance at the wanted frequency. This filter is designed not only to reject the image signal, but also to remove

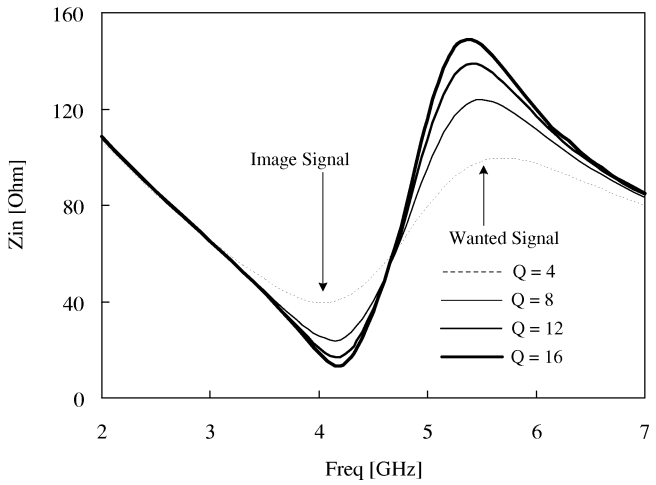


Fig. 4. Filter characteristic for various $Q$ factor values of an on-chip inductor.

the effect of the parasitic capacitance in the signal path of cascode amplifier. Thus, by providing high and low impedance at the wanted and image signals, the filter archives IR and good noise performance at the same time. However, the major drawback of this filer comes from the quality of the on-chip inductor that affects the overall quality factor of the filter.

In typical CMOS technology, the quality factor of the on-chip inductor is dominated by the series resistance. By neglecting all the parasitic components, except the series resistance of the on-chip inductor, the equivalent circuit of only the filter can now be represented as shown in Fig. 3(b), where $R_{L1}$ is the series resistance of $L_1$. Also assume that only the quality factor of the filter at the image frequency is of most interest at this moment; the quality factor of filter is given by

$$Q = \frac{\left(\dfrac{L_1}{C_1 + C_2}\right)^{1/2}}{R_{L1}}. \tag{7}$$

As can be seen in (7), the quality factor of the filter is limited by the parasitic series resistance of $L_1$. Since, in CMOS technology, the on-chip inductor tends to have high resistance, so does the quality factor of the filter. Fig. 4 shows the filter characteristic as a function of frequency with various values of the inductor's quality. In this simulation, the on-chip inductor is modeled as introduced in [15]. From Fig. 4, it can be seen that the filter characteristics significantly depends on the quality factor of the on-chip inductor. Therefore, in order to design a filter with a high quality factor, an off-chip inductor is needed. However, using an off-chip inductor will violate the idea of an on-chip integrated IR filter.

### C. Proposed Third-Order Active Notch Filter

To overcome the limitations of [9] and [10], in this paper, a third-order active notch filter is introduced, as shown in Fig. 5(a). As can be seen from the small-signal equivalent circuit shown in Fig. 5(b), the input impedance $Z_{\rm in}$ of the proposed active filter can be expressed as

$$Z_{\rm in} = \frac{1}{j\omega C_{tt}} // Z_1 \tag{8}$$

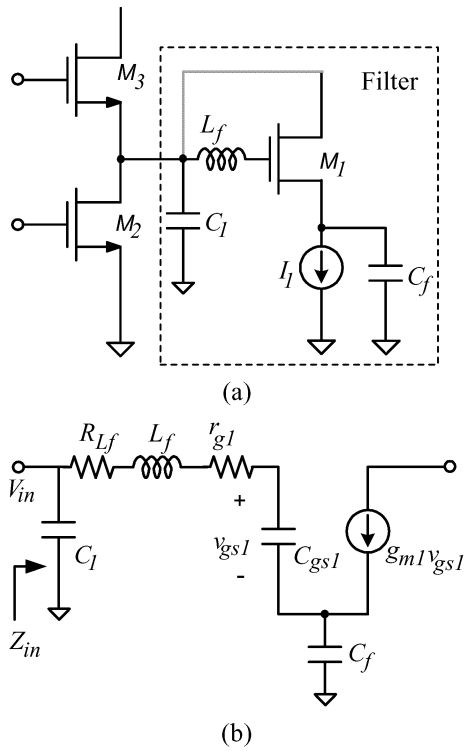


Fig. 5. (a) Schematic of cascode IR LNA with the proposed third-order active notch filter. (b) The filter's small-signal equivalent circuit only.

where

$$Z_1 = j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{\rm gs1}} + \frac{1}{C_f}\right) - \frac{g_{m1}}{\omega^2 C_{\rm gs1} C_f} + R_{Lf} + r_{g1} \tag{9}$$

and $C_{tt} = C_1 + C_{\rm gs1}$.

Note that the negative term in the right-hand side of (9) represents the negative resistance (proportional to $g_{m1}$) seen at the gate of transistor $M_1$. Like the first filter topology shown in Fig. 2(a), by adjusting $g_{m1}$ by varying the bias current $I_1$, sufficient negative resistance can be generated to cancel $R_{Lf}$ and $r_{g1}$. Therefore, the quality factor of this filter is almost unaffected by the quality factor of an on-chip inductor.

Assuming that all the parasitic components are cancelled, the input impedance of the filter is now re-expressed as

$$Z_{\rm in} = \frac{s^2 L_f C_{\rm eq} + 1}{s\left(s^2 C_{tt} L_f C_{\rm eq} + C_{tt} + C_{\rm eq}\right)} \tag{10}$$

where

$$\frac{1}{C_{\rm eq}} = \frac{1}{C_{\rm gs1}} + \frac{1}{C_f}. \tag{11}$$

From (11), the image and wanted signals are located at

$$f_{\rm im} = \frac{1}{2\pi\sqrt{L_f C_{\rm eq}}} \tag{12}$$

$$f_{\rm wanted} = \frac{1}{2\pi\sqrt{\dfrac{1}{L_f}\left(\dfrac{1}{C_{tt}} + \dfrac{1}{C_{\rm eq}}\right)}}. \tag{13}$$

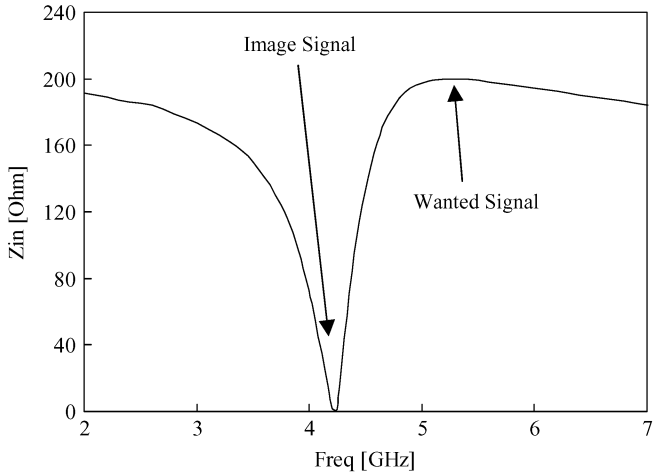


Fig. 6. Filter characteristic of the proposed notch filter.

At the image frequency, the impedance $Z_{\rm in}$ looking into the filter can be reduced to zero such that the entire image signal will be extracted from the original path, whereas at the wanted frequency, the input impedance of the proposed filter $Z_{\rm in}$ is maximized. Therefore, the loss of the wanted signal can be avoided. The ability of IR depends on the difference of impedance between the filter and the original LNA at the image frequency. The larger the difference is, the higher the IR can be obtained. To increase this difference, a feedback connection from the drain of the transistor to the input of the inductor has been added [9], as denoted by the dark line in Fig. 5(a). Now, the input impedance will be decreased by the factor of $(1+g_m/\omega C_{\rm gs1})$ such that the impedance difference becomes less dependent on the negative term in (9). This means that with a relatively low $Q$ filter implemented in the signal path of a typical cascode LNA it is possible to realize a very deep notch with a very high $Q$ provided that the bandpass filter has a large impedance difference.

Fig. 6 shows the filter characteristic as a function of frequency. This design is optimized for a 5.25-GHz wireless local area network (WLAN) and a local oscillator (LO) of 4.75 GHz for 500-MHz IF wireless receivers. Hence, the image signal is located at 4.25 GHz. As can be seen from Fig. 6, the impedance at 4.25 GHz is very low, while the impedance at the wanted signal has a peak value. However, the impedance at the image signal has a narrow valley; therefore, for the correct image cancellation, the zero must occur at the correct frequency. On the other hand, the peak is a wider valley and the exact location of the pole is less important.

## III. IR-LNA Design

In this design, the proposed IR LNA is implemented by applying a two-stage current reuse LNA [16] with the proposed third-order active notch filter shown in Fig. 5. A complete schematic of the IR LNA is shown in Fig. 7. The first stage is a common source inductive degeneration topology. In this stage, an extra capacitor $C_{\rm ex}$ is used together with $L_s$ and $L_g$ so as to obtain power-constrained simultaneous noise and input matching [17], [18]. The second stage uses a cascode configuration, which consists of the transistors $M_2$ and $M_3$. $C_c$ is the ac-coupling capacitor and $C_p$ is the bypass capacitor. In

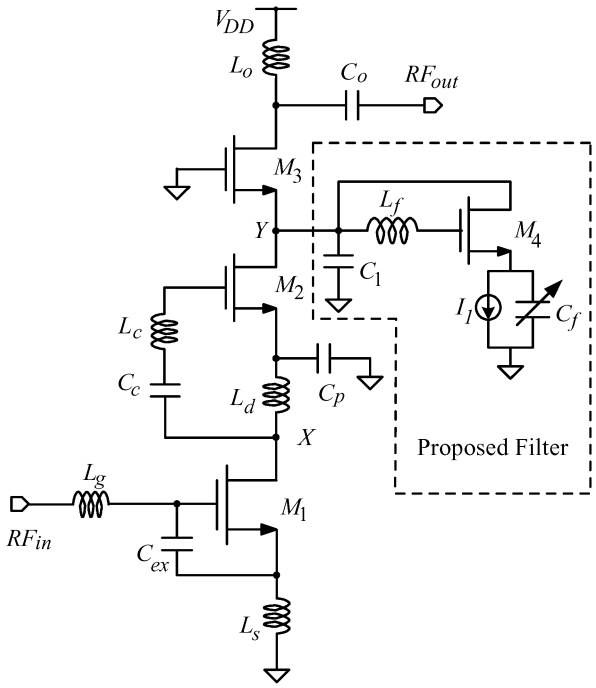


Fig. 7. Schematic of the proposed IR LNA.

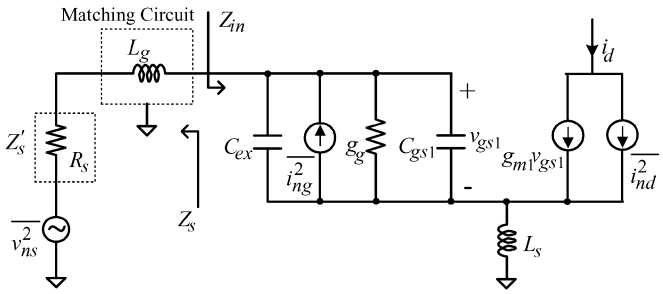


Fig. 8. Small-signal equivalent circuit of the input stage of the IR LNA in Fig. 7 for noise analysis.

this design, an inter-stages inductor $L_c$ is included to resonate with an input capacitor of the second stage $C_{\rm in2}$ (approximately equal to the gate–source capacitor of $M_2$) to improve the gain and NF of the amplifier. A simple $L_o - C_o$ network is used to match the output of the LNA.

### A. Input Stage Noise Optimization

Typically, the noise performance of an LNA is dominated to the input stage. Thereby, in order to simplify the analysis, in this study, only the input stage noise analysis is considered. From this assumption, the simplified small-signal input-stage's equivalent circuit of the proposed LNA, shown in Fig. 7, is predicted as Fig. 8 for the noise analysis. In Fig. 8, the effects of the parasitic resistances of the gate, body, source, drain terminals, and the gate–drain capacitance of $M_1$ on the noise and frequency response are also assumed to be neglected.

Readers may refer to [17] and [18] for further detail of noise analysis. However, in this study, in order to have an overall perspective understanding of the design methodology for the noise and linearity optimization technique, some of the noise parameter expressions called the noise factor, minimum NF,

optimum noise impedance, and noise resistance are rewritten as (14)–(17), shown at the bottom of this page, where

$$g_g = \frac{\omega^2 C_{\rm gs1}^2}{5g_{d0}} \quad \delta_{\rm eff} = \delta \cdot \left(\frac{C_{\rm gs1}^2}{C_t^2}\right) \quad C_t = C_{\rm gs1} + C_{\rm ex}.$$

From Fig. 8, the input impedance of the LNA is given by

$$Z_{\rm in} = sL_s + \frac{1}{sC_t} + \frac{g_{m1}L_s}{C_t}. \tag{18}$$

The condition that allows the simultaneous noise and input matching is now

$$Z_{\rm opt} = Z_{\rm in}^*. \tag{19}$$

From (16) and (18), (19) can be satisfied when the following conditions are met:

$$\frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{\rm gs1}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\rm gs1}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} = {\rm Re}[Z_s] \tag{20}$$

$$\frac{j\left(\dfrac{C_t}{C_{\rm gs1}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\rm gs1}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\rm gs1}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s = {\rm Im}[Z_s] \tag{21}$$

$$\frac{g_{m1}L_s}{C_t} = {\rm Re}[Z_s] \tag{22}$$

$$sL_s + \frac{1}{sC_t} = -{\rm Im}[Z_s]. \tag{23}$$

As can be seen in (18), the source degeneration generates a real part at the input impedance. This is important because there is no real component in the input impedance without degeneration, while there is one in the optimum noise impedance. Therefore, $L_s$ helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, from (18), the imaginary part of $Z_{\rm in}$ is changed by $sL_s$, and this is followed by nearly the same change in $Z_{\rm opt}$ in (16), especially with advanced technology, as discussed in [18]. Therefore, (23) can be dropped, which means that, for a given value of $L_s$, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign. Now, the design parameters that satisfy (20)–(22) are $V_{\rm GS}, W_1$ (or $C_{\rm gs1}$), $L_s$, and $C_{\rm ex}$. Since there are three equations and four unknowns, (20)–(22) can be solved for an arbitrary value of $Z_s$ by fixing the value of one of the design parameters, which is possibly the power dissipation or $V_{\rm GS}$. In other words, this LNA design optimization technique allows designing simultaneous noise and input matching at any given amount of power dissipation.

### *B. Linearity Analysis*

In RF circuit design, the linearity is another important parameter that needs to be considered. Since the LNA is the first block in the typical receiver system, the linearity of the LNA is commonly estimated by the third-order intermodulation (IM3) product. Two signals of adjacent channels $A\sin\omega_1$ and $A\sin\omega_2$ will generate products IM3 such as $A\sin(2\omega_1-\omega_2)$ and $A\sin(2\omega_2-\omega_1)$ at the output of the nonlinear circuit. Normally, IM3 is calculated as the ratio of the IM3 and response magnitude of the fundamental frequency, which is given by [2]

$${\rm IM3} = \frac{3}{4}A^2\left|\frac{A_3(2\omega_1-\omega_2)}{A_1(\omega)}\right| \tag{24}$$

where $A_1$ and $A_3$ are the first- and third-order coefficient of Volterra series.

As mentioned above, the proposed IR LNA consists of two amplifier stages. According to [2], the linearity of the second

$$F = 1 + \frac{1}{g_{m1}^2 R_s}\left\{\gamma g_{d0}\cdot\left\{\begin{array}{c}\left[1+s^2C_t(L_g+L_s)\left(1+|c|\alpha\sqrt{\dfrac{\delta_{\rm eff}}{5\gamma}}\right)\right]^2 \\ -(sC_tR_s)^2\left(1+|c|\alpha\sqrt{\dfrac{\delta_{\rm eff}}{5\gamma}}\right)^2 \\ -\dfrac{\alpha\delta_{\rm eff}}{5}\left(1-|c|^2\right)g_{m1}(sC_t)^2\left(R_s^2 - sL_g^2\right)\end{array}\right\}\right\} \tag{14}$$

$$F_{\rm min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)} \tag{15}$$

$$Z_{\rm opt} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma\left(1-|c|^2\right)}} + j\left(\dfrac{C_t}{C_{\rm gs1}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\rm gs1}\left\{\dfrac{\alpha^2\delta}{5\gamma\left(1-|c|^2\right)} + \left(\dfrac{C_t}{C_{\rm gs1}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{16}$$

$$R_n = \frac{\gamma}{\alpha}\cdot\frac{1}{g_{m1}} \tag{17}$$

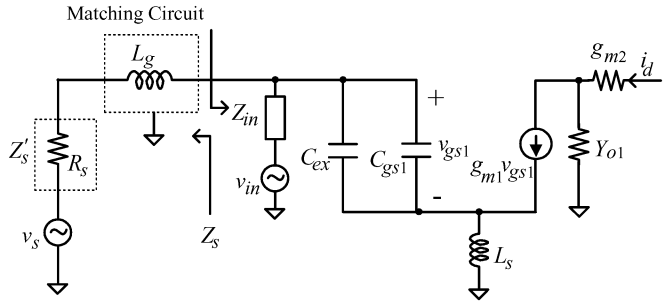


Fig. 9. Circuit model for linearity analysis.

stage plays an important role and it cannot be neglected when the linearity is considered. Thereby, for the linearity analysis purpose, the equivalent small-signal circuit of the LNA in Fig. 7 can be predicted as Fig. 9, where the second stage is considered and modeled by the series transconductance $g_{m2}$. Assume that, in this case, the effects of $C_{\rm gs2}$ and $C_{\rm gd1}$ are neglected. In Fig. 9, the output admittance seen at the drain of $M_1$ and $Y_{o1}$ is added in the model with the purpose of identifying the output contribution. The magnitude of $\mathrm{IM}_3$ at $(2\omega_1 - \omega_2)$ can be derived from the Volterra-series analysis [18] as follows:

$$|\mathrm{IM}_3| = \frac{A^2}{2}\left|\frac{A_1^3(s)}{g_{m1}^3}\right| |a_1(s)| \left|3g_3 - 2g_2^2 B\right| \tag{25}$$

where

$$A_1(s) = \frac{g_{m1}}{a_1(s) + g_{m1}a_2(s)} \tag{26}$$

$$a_1(s) = sC_t(Z_{\rm in} + sL_s) + 1 \tag{27}$$

$$a_2(s) = sL_s\left(1 + \frac{Y_{o1}}{g_{m2}}\right) \tag{28}$$

$$B = 2\Delta s L_s(\Delta s)a_2(\Delta_s)A_1(\Delta s) + 2sL_s(2s)a_2(2s)A_1(2s) \tag{29}$$

$$g_2 = \frac{4K\mu_0 L^2 v_{\rm sat}^2}{\left[(V_{\rm gs} - V_t)\mu_1 + 2Lv_{\rm sat}\right]^3} \tag{30}$$

$$g_3 = \frac{4K\mu_0 L^2 v_{\rm sat}^2}{\left[(V_{\rm gs} - V_t)\mu_1 + 2Lv_{\rm sat}\right]^4} \tag{30}$$

$$\Delta s = s_1 - s_2. \tag{31}$$

Here, $g_2$ and $g_3$ are the second- and third-degree coefficients of the transistor nonlinear Taylor expansion. The $B$ coefficient is the second-order interaction of the products $2\omega, \omega_1 - \omega_2$, and $\omega_2 - \omega_1$. $A_1(s)$ is the transconductance of the circuit. Substituting (26) into (25), it shows that $|\mathrm{IM3}|$ reversely depend on the term

$$\left[sC_tR_{\rm in} + sL_sg_{m1}\left(1 + \frac{Y_{o1}}{g_{m2}}\right)\right]^3. \tag{32}$$

As can be seen in (25), the linearity can be improved by using different ways such as the reduction of $a_1(s), g_3$ or with the increase (30). From (27), with inductive degeneration, the $s^2C_tL_s$ term will cancel the "1" term and, as a result, $a_1(s)$ is reduced. This indicates that the inductive degeneration topology helps to improve $|\mathrm{IM3}|$ compared to the resistive and capacitive degeneration topology since such cancellation does not exist. As can be seen from (30) and (31), the effect of $g_3$ and $g_2$ coefficients in $|\mathrm{IM3}|$ is inversely dependent on the bias $(V_{\rm GS} - V_t)$, indicating that the linearity can be improved by increasing the gate–source voltage. However, increasing the gate–source voltage will increase the power dissipation. With large $Y_{o1}$ and $g_{m1}$ values and small $g_{m2}$ value, (32) is increased such that linearity will be increased. For the same reason, with any increase in $C_t$, preserving the simultaneous noise and input matching conditions also improves the linearity. Note that if $C_{\rm ex}$ is not used, the higher $C_t$, the higher the gate–source capacitance $C_{\rm gs1}$ is. The gate–source capacitance can be increased with an increase of the transistor size. However, at a given bias condition, increasing the transistor size results in the more current dissipation. Therefore, $C_{\rm ex}$ not only helps to archive matching conditions in both input impedance and noise at a given amount of power consumption, but also helps to improve the linearity.

### C. Input Stage Design Methodology

Here, the overall consideration for the input stage of LNA design to obtain power-constrained simultaneous noise and input matching, as well as satisfy the linearization condition, is described. The qualitative description of the proposed design process would be as follows.

- First, choose the dc bias $V_{\rm GS}$, for example, the bias point that provides minimum $F_{\rm min}$.
- Second, choose the transistor size $W$ based on the power constraint $P_D$.
- Third, choose the additional capacitance $C_{\rm ex}$, as well as the degeneration inductance, $L_s$ to satisfy (20), (22), and $s^2C_tL_s = -1$ conditions (as mentioned above, to improve the linearity of the LNA, the condition $s^2C_tL_s = -1$ need to be satisfied). With the given $L_s$, the condition $\mathrm{Im}[Z_{\rm in}^*] = \mathrm{Im}[Z_{\rm opt}]$ is automatically satisfied. At this point, simultaneous noise and input matching is achieved.
- As the final phase, if there exists any mismatch between $Z_{\rm in}$ and $Z_s'$, as shown in Fig. 8, an impedance-matching circuit can be added.

This design optimization technique suggest that, by using an extra capacitor $C_{\rm ex}$, in principle, the LNA can be designed to achieve power-constrained simultaneous noise and input matching, as well as satisfy the linearization condition at a given amount of power consumption. However, the limitations of this are high $R_n$ and low effective cutoff frequency. High $R_n$ can be a serious limitation for the practical high-yield LNA design.

### D. Inter-Stage Series Resonant Technique

Fig. 10(a) shows the small-signal equivalent circuit from the drain node of $M_1$ to that of $M_2$ of the LNA shown in Fig. 7. In this figure, $Z_{\rm sub}$ and $Z_{L1}$ represent parasitic impedance to the ground through the silicon substrate and the load impedance of the first stage, respectively. $R_{\rm in2}$ and $C_{\rm in2}$ are the real part of the input impedance and equivalent input capacitance of the second stage seen from node $X$, respectively. If $R_{\rm in2}$ is much

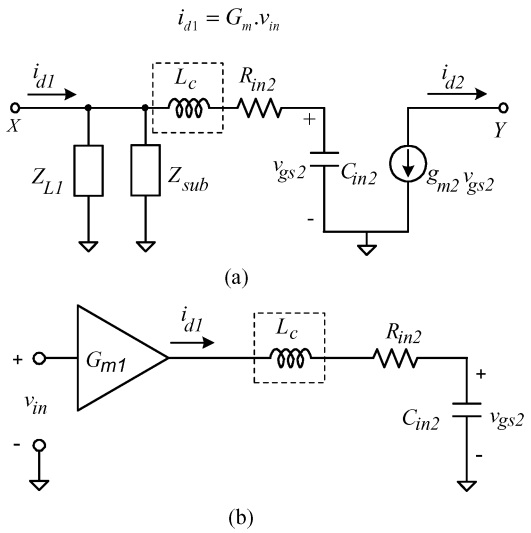


Fig. 10. Small-signal equivalent circuit of the IR LNA. (a) The small-signal equivalent circuit from node $X$ to $Y$ to evaluate the effect of the inter-stage series resonant technique and (b) to evaluate the effect of the quality factor of the inter-stage series on the performances of the IR LNA.

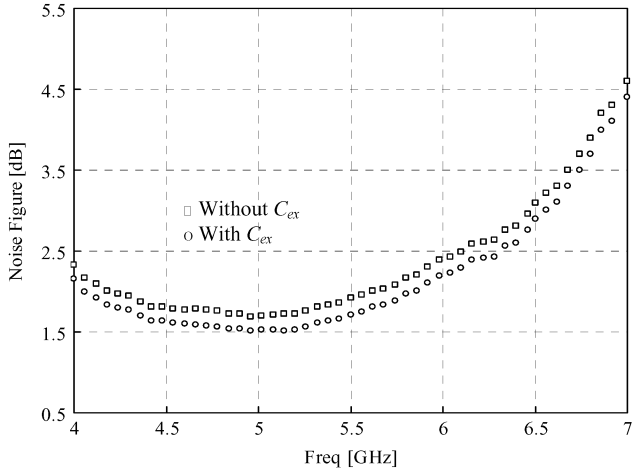


Fig. 11. Measured NF of a simple cascode LNA: with and without $C_{\rm ex}$.

smaller than $|Z_{L1}//Z_{\rm sub}|$, then the series resonant network $L_c-C_{\rm in2}$ will provide low impedance at node $X$. Under the series resonance, and assume that $C_{\rm in2}$ is approximately equal to $C_{\rm gs2}$, the current gain from the drain of $M_1$ to that of $M_2$ can be given by

$$\begin{aligned}\frac{i_{d2}}{i_{d1}} &= \frac{g_{m2}}{sC_{\rm in2}} \frac{sL_d//Z_{\rm sub}}{sL_d//Z_{\rm sub} + sL_g + 1/sC_{\rm in1}} \\ &\approx \frac{g_{m2}}{sC_{\rm gs2}} \\ &= \frac{\omega_T}{\omega} \end{aligned} \tag{33}$$

where $i_{d1}, i_{d2}$ are, respectively, the currents of $M_1$ and $M_2$; $C_{\rm gs2}$ and $g_{m2}$ are the gate–source capacitor and transconductance of $M_2$, respectively, $\omega_T$ represents the cutoff frequency of $M_2$, and $\omega_o$ represents the operating frequency. Note that (33) is valid regardless of the size of transistor $M_2$ and the value of $R_{\rm in2}$, as long as $R_{\rm in2} \ll |Z_{L1}//Z_{\rm sub}|$. In (33), with the given 0.18-$\mu$ m CMOS technology, the proposed series resonant technique can provide a current gain of over ten. In addition, due to the small impedance presented at node $X$, the proposed topology can avoid the signal loss through substrate. Besides, the low impedance at node $X$ also reduces voltage gain of the first stage so that the Miller effect on $M_1$ is reduced.

In Fig. 10(a), the effect of the quality factor of the inter-stage series resonant network on the performances of the LNA is one of the important factors that needs to be considered. From Fig. 10(a), the quality factor of the resonance network $Q_{\rm rs}$ can be calculated by

$$Q_{\rm rs} = \frac{\sqrt{L_c C_{\rm in2}}}{R_{\rm in}} \tag{34}$$

$$R_{\rm in} = \frac{g_{m2} C_{\rm gs2}}{L_3} + R_{Lc} \tag{35}$$

where $R_{Lc}$ is the parasitic series resistance of $L_c$. As can be seen in (34) and (35), $Q_{\rm rs}$ can significantly depend on $R_{Lc}$. The effect of $R_{Lc}$ on the performances of the LNA can be summarized as follows. First, the series resonant condition will provide low impedance at node $X$ such that the current gain from node $X$ to node $Y$ does not depend on $R_{Lc}$. Second, the voltage gain $A_v$ from the gate of $M_1$ to that of $M_2$ can be calculated based on the equivalent circuit shown in Fig. 10(b). From Fig. 10(b), the output current of the first stage can be given by

$$i_{d1} = G_m \cdot v_{\rm in}. \tag{36}$$

The voltage at the input of the second stage is

$$v_{\rm gs2} = i_{d1} \cdot \frac{1}{sC_{\rm in2}} = \frac{1}{sC_{\rm in2}} \cdot G_m \cdot v_{\rm in}. \tag{37}$$

Therefore, the voltage gain $A_v$ can be expressed as

$$A_v = \frac{v_{\rm gs2}}{v_{\rm in}} = G_m \cdot \frac{1}{sC_{\rm in2}}. \tag{38}$$

From (38), the voltage gain $A_v$ is independent of $R_{\rm in}$, thereby $R_{Lc}$ does not affect the voltage gain of the amplifier. Therefore, in this design, $L_c$ is implemented as on-chip.

## IV. Measurement Results

In this design, considering the power gain and linearity of circuit, the current dissipation is fixed to be 4 mA. To demonstrate the effect of $C_{\rm ex}$ on the noise performance of the LNA, two simple cascode LNA versions are fabricated: one uses an extra capacitor, while the other does not. The measured NF results are shown in Fig. 11. As can be seen from Fig. 11, the one with $C_{\rm ex}$ has a lower NF compared to that with without $C_{\rm ex}$. The improvement in the NF effect can be understood as the mismatch between $\mathrm{Re}[Z_{\rm opt}]$ and $\mathrm{Re}[Z_s]$.

To demonstrate the effect of the proposed notch filter on the performances of the LNA, two versions of the LNA are designed. Version 1 is an LNA without the proposed notch filter, and version 2 includes the proposed third-order notch filter. Fig. 12 shows the measurement results of the NF versus the

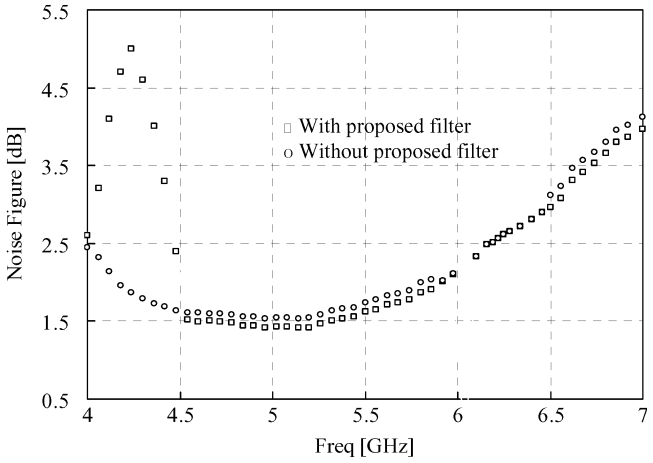


Fig. 12. Measured NF of LNAs.

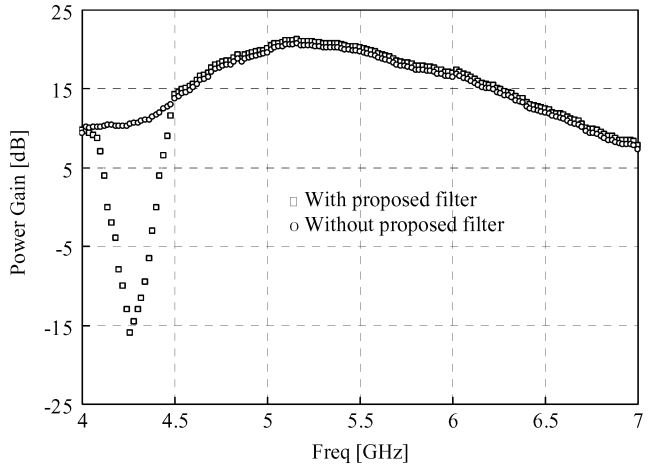


Fig. 13. Measured power gain of LNAs.

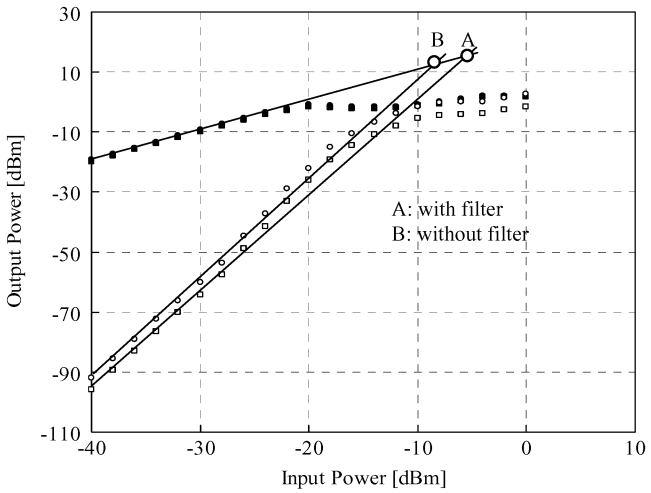


Fig. 14. Measured IIP3 of LNAs.

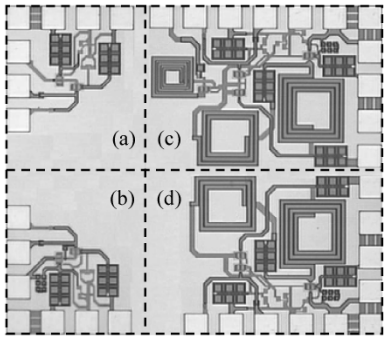


Fig. 15. Microphotograph of the LNAs. (a) Simple cascode without $C_{ex}$, (b) with $C_{ex}$, (c) current reused with the proposed filter, and (d) without the proposed filter.

TABLE I
SUMMARY OF THE MEASURED IR-LNA PERFORMANCES

| Parameters | Without filter | With filter |
|---|---|---|
| Operating frequency [GHz] | 5.25 | 5.25 |
| Image frequency [GHz] | - | 4.25 |
| $S_{11}/S_{22}$ [dB | -19/-20 | -18/-20 |
| NF [dB] | 1.5 | < 1.5 |
| Power gain [dB] | 20 | 20.5 |
| IIP3 [dBm] | -8 | -5 |
| Input P 1dB | -19 | -16 |
| Image rejection ratio | - | -20 |
| Power consumption [mW] | 11.7 | 12 |
| Technology [μm] | CMOS 0.18 | |

frequency of the LNAs. As can be seen from Fig. 12, version 2 presents a high NF near the image frequency that can be understood as the signal loss through the notch filter. However, as the frequency approaches 5.25 GHz, the NF reduces below that of version 1. Fig. 13 shows the power gain of the two LNAs. From Fig. 13, by using the proposed filter, the IR LNA provides approximately 26 dB of overall IR. At 5.25 GHz, the power gain of the version 2 is higher than that for version 1. The improvements in NF and power gain at the operating frequency are 0.1 and 0.5 dB, respectively, which are explained as the resonant effect between $L_f$ and the parasitic capacitance at node $Y$ [10]. From measured results, the values of $S_{11}/S_{22}$ of two LNAs, with and without a filter, are $-18$ dB/$-20$ dB and $-19$ dB/$-20$ dB, respectively.

The measured IIP3 results of the LNAs are shown in Fig. 14. Two tones were applied with equal power levels at 5.25 and 5.255 GHz. The measured results indicate $-5$-dBm and $-8$-dBm IIP3 for the case of using and not using the notch filter. The effect of the linearity improvement is not clear at this point; however, this result is confirmed by measurement. The photographs of LNAs are shown in Fig. 15. The chip area of versions 1 and 2 are 0.4 and 0.5 mm, respectively. The measured performances of LNAs are summarized in Table I.

## V. CONCLUSION

The rejection of image signals is the main problem in the superheterodyne architecture. To eliminate the use of an off-chip SAW filter, the on-chip IR techniques have been developed. Among them, the IR notch filter appears to be the proper solution for an on-chip integrated image receiver. This paper introduces the third-order active notch filter as the satisfactory factor. The proposed notch filter can control not only the wanted signal, but also the image one. It can also provide a high-value quality factor regardless of the quality factor of the on-chip inductor. In addition, the method to design an

LNA satisfying the power-constrained simultaneous noise and input matching, as well as linearity optimization conditions is introduced. The IR LNA, implemented by integrating a high-gain LNA with the proposed third-order active notch filter, shows some improvement in the NF and power gain thanks to the resonant effect between the inductor used in the notch-filter topology and the parasitic capacitor at the signal path at the middle node of the cascode topology. In addition, this paper introduces the LNA design methodology, which obtains noise matching and power matching, as well as linearity optimization at a given amount of power consumption. Another advantage of using the proposed third-order notch filter is that the linearity of the LNA can be improved. Although this improvement is not clear to us at the moment, it has been confirmed by measured results. Measured results also show a power gain of 20.5 dB, an NF of lower than 1.5 dB, an IIP3 of $-5$ dBm, and an IR of 26 dB for the proposed IR LNA, which dissipates a dc current of 4 mA under a supply voltage of 3 V.

## REFERENCES


[1] B. Razavi, "Challenges in portable RF transceiver design," *IEEE Circuits Devices Mag.*, vol. 12, pp. 12–25, Dec. 1996.

[2] ——, *RF Microelectronics*: Prentice Hall, 1998.

[3] T. H. Lee, "5-GHz CMOS wireless LANs," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 268–280, Jan. 2002.

[4] S. Wu *et al.*, "A 900-MHz/1.8 GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998.

[5] S. Lee *et al.*, "A 1 GHz image-rejection down-converter in 0.8 $\mu$m CMOS technology," *IEEE Trans. Consum. Electron.*, vol. 44, no. 2, pp. 235–239, May 1998.

[6] J. P. Maligeorgos *et al.*, "A low-voltage 5.1–5.8 GHz image-rejection receiver with wide dynamic range," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1917–1926, Dec. 2000.

[7] N. Kim *et al.*, "An image rejection down conversion mixer architecture," in *TENCON 2000*, pp. 287–289.

[8] P. B. Khannur *et al.*, "A 2.45 GHz fully differential CMOS image-reject mixer for Bluetooth applications," in *Radio Frequency Integrated Circuits Symp.*, 2002, pp. 415–418.

[9] J. Macedo *et al.*, "A 1.9 GHz silicon receiver with monolithic image reject filtering," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 378–386, Mar. 1996.

[10] H. Samavati *et al.*, "A 5-GHz CMOS wireless LNA receiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.

[11] Y. Chang *et al.*, "An inductorless active notch filter for RF image rejection," in *42nd Midwest Circuits Systems Symp.*, 2000, pp. 166–169.

[12] C. Guo *et al.*, "A monolithic 2-V 950-MHz CMOS bandpass amplifier with a notch filter for wireless receivers," in *IEEE Radio-Frequency Integrated Circuit Symp.*, 2001, pp. 79–82.

[13] Y. Chang *et al.*, "A monolithic RF image-reject filter," in *Southwest Mixed-Signal Design Symp.*, 2000, pp. 41–44.

[14] C. Guo *et al.*, "A full integrated 900 MHz CMOS wireless receiver with on-chip RF and IF filters and 79-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1084–1089, Aug. 2002.

[15] S. S. Mohan *et al.*, "Simple accurate expression for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[16] C. Y. Cha *et al.*, "A 5.2 GHz LNA in 0.35 $\mu$m CMOS utilizing interstage series resonance and optimizing the substrate resistance," in *Eur. Solid-Stage Circuit Int. Conf.*, Sep. 2002, pp. 339–342.

[17] T.-K. Nguyen *et al.*, "CMOS low noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.

[18] T.-K. Nguyen *et al.*, "A power-constrained simultaneous noise and input matching low noise amplifier design technique," presented at the IEEE Circuits Systems Symp., Vancouver, BC, Canada, 2004.

[19] E. Roa *et al.*, "A methodology for CMOS low noise amplifier design," in *IEEE Integrated Circuit Systems Design Symp.*, 2003, pp. 14–19.


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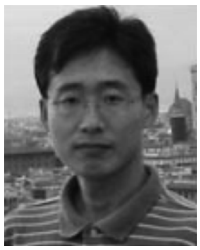

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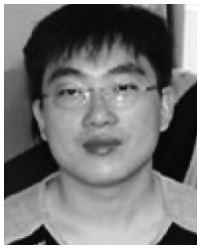

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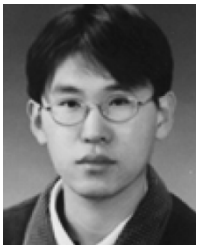

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