A Complementary Colpitts Oscillator in CMOS Technology

Choong-Yul Cha, *Member, IEEE,* and Sang-Gug Lee, *Member, IEEE*

***Abstract*—A new complementary Colpitts (C-Colpitts) oscillator topology is introduced and the oscillation mechanism as a one-port model is analyzed. Based on the one-port analysis and the existing phase-noise model, the phase-noise equation of the proposed C-Colpitts oscillator is derived as the function of the oscillation frequency, Q factor of tank circuit, and bias current. The phase-noise equation provides the design guideline to optimize the phase noise of the proposed Colpitts oscillator, of which the property is proven with simulation and measurement results. The proposed Colpitts voltage-controlled oscillators are fabricated using 0.35-μm CMOS technology for 2-, 5-, 6-, and 10-GHz bands. Measurement shows that the phase noise is −118.1 dBc at 1-MHz offset from 6-GHz oscillation while dissipating 4.6 mA of current from a 2.0-V supply.**

***Index Terms*—CMOS, Colpitts, complementary, phase noise, optimization, voltage-controlled oscillator (VCO).**

I. Introduction

With advancements in submicrometer CMOS technology, CMOS technology has become widely used for low-cost and highly integrated RF integrated circuits (RFICs). Recently, single-chip transceivers that integrate both digital and RF circuits using CMOS technology have been introduced. Among the building blocks in single-chip RFICs, design and implementation of fully integrated low-noise CMOS voltage-controlled oscillators (VCOs) is known as a challenging block because of the inborn limitations of silicon CMOS process technology. Most of the previously reported publications about CMOS VCOs describe the negative-G_m differential topology. In these publications, in order to optimize the phase-noise performance, researchers stress the importance of layout issues such as active and passive device design, and the floor plan of layout to reduce the side effects of the parasitics in CMOS technology [1]–[3]. In negative-G_m-based submicrometer CMOS differential VCOs, the complementary structure shows a better performance than the NMOS-only structure, as a result of the reduced hot carrier effect, better up/down swing symmetry, and higher transconductance of the constituting transistors [3].

Thus, by using low parasitic simple and high transconductance oscillator topology, there exists more potential in the design of a low-noise oscillator in high frequency or with low power. Traditionally, the Colpitts oscillator, which has a simple oscillator core, has been the most favored topology for low phase noise [4]. However, since the conventional Colpitt oscillator needs additional circuits for bias and buffer interfaces, its oscillation performances may be degraded by the parasitics in high frequency.

In this paper, a complementary Colpitts (C-Colpitts) oscillator topology [5] is introduced that is effectively composed of two components, a complementary NMOS and PMOS transistor pair and an inductor, and requires no additional circuits for bias and buffer interfaces. Since the proposed C-Colpitts oscillator is simple, has a complementary structure, and provides high transconductance, better oscillation performance can be achieved. In Section II, the operational principle of the proposed C-Colpitts oscillator is analyzed as a one-port oscillator model. In Section III, the phase-noise equation of the proposed C-Colpitts oscillator is derived. The phase-noise property is confirmed with simulation and provides the design guideline to optimize the phase-noise performance. In Section IV, the phase-noise property of C-Colpitts VCOs is proven with experimental results. Next, the performances of C-Colpitts VCOs with 0.35-μm CMOS technology are compared with the findings from previous research. Conclusions are finally presented in Section V.

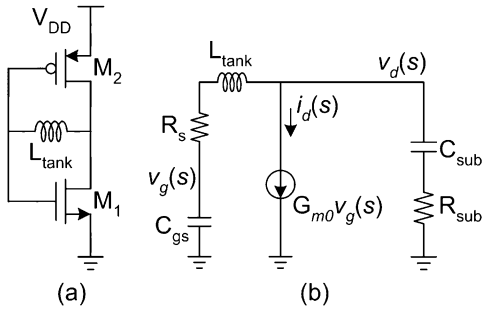

Fig. 1. (a) Proposed C-Colpitts oscillator core. (b) Equivalent circuit of C-Colpitts core including parasitics.

II. C-Colpitts Oscillator Topology and One-Port Analysis

Fig. 1(a) and (b) shows the core of the proposed C-Colpitts oscillator and the small-signal equivalent circuit with parasitic components. In Fig. 1(b), G_{m0} represents the overall transconductance $(g_{mn} + g_{mp})$, $C_{\rm gs}$ represents the overall gate–source capacitance, and $C_{\rm sub}$ and $R_{\rm sub}$ represent the drain to substrate parasitics of M_1 and M_2 in Fig. 1(a), respectively. In Fig. 1(b), R_s represents the series resistance of inductor $L_{\rm tank}$. In Fig. 1(a) and (b), the transistors M_1 and M_2, inductor $L_{\rm tank}$, gate–source capacitors $C_{\rm gs}$, and substrate parasitc $C_{\rm sub}$ constitutes a Colpitts

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oscillator [6]. As described earlier, since the simple and complementary structure of the proposed C-Colpitts oscillator decreases the parasitic components and increases the negative conductance, the potential of high-performance oscillation will increase.

For better understanding and design optimization, the one-port analysis for the small-signal equivalent circuit, shown in Fig. 1(b), is described in the following. From Fig. 1(b), the equivalent conductance $G_m(s)$ can be given by

$$G_m(s) = i_d(s)/v_d(s) = \frac{G_{m0}}{s^2 L_{\rm tank} C_{\rm gs} + sC_{\rm gs}R_s + 1} \tag{1}$$

where i_d and v_d represent the small-signal drain current and node voltage of the NMOS and PMOS transistors. From (1), the equivalent conductance $G_m(s)$ can be re-expressed as a combination of the equivalent real conductance and inductance as follows:

$$G_m(j\omega) = G_{m0}\frac{1-\omega_n^2}{(1-\omega_n^2)^2 + \left(\dfrac{\omega_n}{Q_{\rm sr}}\right)^2} + \frac{1}{j}\frac{\dfrac{G_{m0}\omega_n}{Q_{\rm sr}}}{(1-\omega_n^2)^2 + \left(\dfrac{\omega_n}{Q_{\rm sr}}\right)^2} \tag{2}$$

$$= G_r(\omega_n) + \frac{1}{j\omega_{\rm sr}\omega_n L_i(\omega_n)} \tag{3}$$

where $s = j\omega, Q_{\rm sr} = \sqrt{L_{\rm tank}/C_{\rm gs}}/R_f, \omega_n = \omega/\omega_{\rm sr}$, and $\omega_{\rm sr} = 1/\sqrt{L_{\rm tank}C_{\rm gs}}$. In (2) and (3), $Q_{\rm sr}, \omega_{\rm sr}$, and ω_n represent the quality (Q) factor, series resonance frequency of the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ circuit, and normalized frequency over $\omega_{\rm sr}$, respectively.

From (2) and (3), it is obvious that the real value of the equivalent conductance $G_r\ (\omega_n)$ becomes negative when $\omega_n > 1\ (\omega > \omega_{\rm sr})$. This means that the proposed oscillator can oscillate only the frequencies above $\omega_{\rm sr}$. The negative conductance generation behavior can be explained as follows: at frequencies above $\omega_{\rm sr}$, due to the second-order phase transition of the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ circuit, the phase transition at the gate node of the transistor with respect to the drain node becomes larger than 90°, and this leads to the drain current inversion. As shown in (2) and (3), the imaginary part of $G_m(s)$ can be represented by an equivalent inductor at all frequencies, and by the similar mechanism, the inductance increases rapidly for $\omega > \omega_{\rm sr}$. From (2) and (3), $G_r\ (\omega_n)$ and $L_i\ (\omega_n)$ can be re-expressed as follows:

$$G_r(\omega_n) = G_{m0}\frac{1-\omega_n^2}{(1-\omega_n^2)^2 + \left(\dfrac{Q_{\rm sr}}{\omega_n}\right)^2} \tag{4}$$

$$L_i(\omega_n) = \frac{1}{G_{m0}\omega_{\rm sr}}\frac{Q_{\rm sr}}{\omega_n^2}\left[(1-\omega_n^2)^2 + \left(\frac{\omega_n}{Q_{\rm sr}}\right)^2\right]. \tag{5}$$

Using (4) and (5), the equivalent one-port oscillator circuit can be configured as shown in Fig. 2. As shown in (4) and (5),

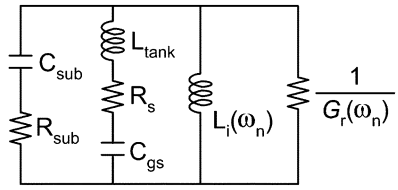

Fig. 2. Equivalent one-port oscillator circuit.

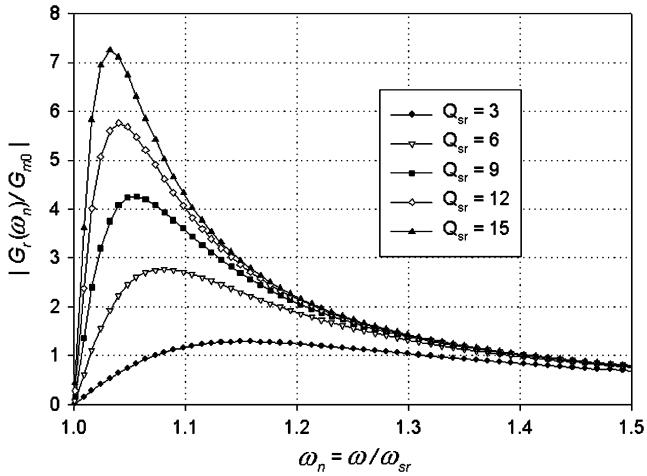

Fig. 3. $|G_r(\omega_n)/G_{m0}|$ over ω_n.

when $\omega_n = 1, G_r(\omega_n) = 0$ and only $L_i(\omega_n)$ has an equivalent value, which means that the phase difference between the gate and drain node in Fig. 1(a) is exactly 90°. At frequencies slightly higher than $\omega_{\rm sr}, \omega_n > 1$, the phase between the gate and drain node rapidly approaches 180°, leading to negative real conductance.

In this frequency region, the voltage drop across the gate–source capacitor is amplified by the amount of the quality factor of the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ circuit, which means a sharp increase in $G_r\ (\omega_n)$ over G_{m0}. As frequency increases further, the phase between the gate and drain node of the series $R_s L_{\rm tank} C_{\rm gs}$ circuit approaches almost 180°, and the imaginary term of $G_m(s)$ is negligibly small, leading to a huge amount of active inductance. In this frequency region, the Q-factor multiplication in the series resonance circuit can no longer be applied any more and the voltage division mechanism dominates in the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ circuit. The negative conductance will decrease with an increase in frequency as a result of a decrease of voltage drop in the gate–source capacitor.

The normalized conductance and active inductance $G_r(\omega_n)$ and $L_i\ (\omega_n)$, shown in (4) and (5), are plotted in Figs. 3 and 4. Fig. 3 shows the variation of $G_r\ (\omega_n)$ over ω_n for the different value of $Q_{\rm sr}$. As can be seen in Fig. 3, the proposed oscillator topology provides a large negative conductance over a wide frequency band of operation and shows a peak near the frequency of $\omega_{\rm sr}$. The large absolute value of $G_r\ (\omega_n)/G_{m0}$ in Fig. 3 indicates that the proposed C-Colpitts topology is suitable for very low-power oscillation, particularly when the high-Q factor inductor is combined.

Fig. 4 shows the variation of $L_i\ (\omega_n) \times G_{m0}\omega_{\rm sr}$ over ω_n for the different value of $Q_{\rm sr}$, where G_{m0} and $\omega_{\rm sr}$ are constant.

Considering the typical values for G_{m0} (1–30 mS) and $\omega_{\rm sr}$ (1–5 GHz), it can be shown that the values for $L_i\ (\omega_n)$ ranges

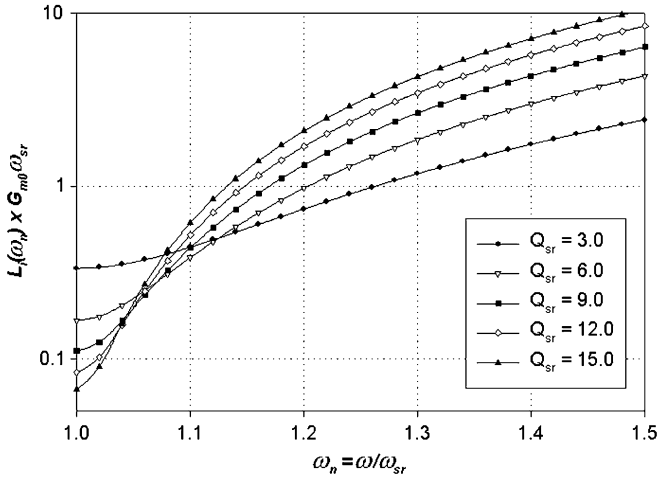

Fig. 4. $L_i(\omega_n) \times G_{m0}\omega_{\rm sr}$ over ω_n.

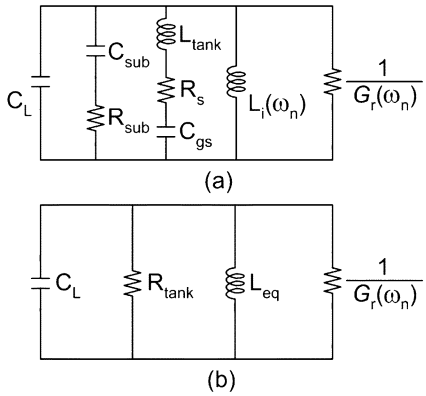

Fig. 5. (a) Equivalent one-port oscillator with C_L. (b) Simplified equivalent one-port oscillator circuit with an equivalent parallel tank.

from a few to a few hundred nanohenry, depending on the frequency of operation and $Q_{\rm sr}$. Therefore, at operation frequencies near $\omega_{\rm sr}, L_i\ (\omega)$ can play a major role in determining the frequency of resonance, but less of a role as the operation frequency moves away from $\omega_{\rm sr}$.

In the proposed C-Colpitts oscillator, the oscillation frequency can be controlled by adding high-Q loading capacitance C_L at the drain node of M_1 and M_2, as shown in Fig. 1(a). The loading capacitance will not affect the frequency behavior of $G_r\ (\omega_n)$, $L_i\ (\omega_n)$, and the Q factor of the R_s–$L_{\rm tank}$–$C_{\rm gs}$ and $C_{\rm sub}$–$R_{\rm sub}$ branch. For the equivalent circuit including C_L, which is shown in Fig. 5(a), the oscillation frequency can be determined by the combined resonance frequency of $L_{\rm tank}, C_{\rm gs}, C_{\rm sub}, C_L$, and $L_i\ (\omega_n)$. In Fig. 5(a), for simplification, by ignoring the substrate parasitics ($C_{\rm sub}$ and $R_{\rm sub}$) and $L_i\ (\omega_n)$, the oscillation frequency ω_o is given as

$$\begin{aligned}\omega_o^2 &= \frac{1}{L_{\rm tank}}\left(\frac{C_L+C_{\rm gs}}{C_L C_{\rm gs}}\right)\\ &= \frac{1}{L_{\rm tank}C_{\rm gs}}\left(1+\frac{C_{\rm gs}}{C_L}\right)\\ &= \omega_{\rm sr}^2\left(1+\frac{C_{\rm gs}}{C_L}\right).\end{aligned} \tag{6}$$

From (6), it is known that the oscillation frequency of the proposed C-Colpitts oscillator is always higher than $\omega_{\rm sr}$. To find the equivalent parallel tank resistance at a given oscillation frequency, we must keep an eye on the fact that the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ can be changed to an equivalent series LR circuit (note: $\omega_o > \omega_{\rm sr}$).

At the oscillation frequency ω_o, the impedance $Z_{RLC}\ (\omega_o)$ of the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ circuit is given as

$$\begin{aligned}Z_{\rm RLC}(\omega_o) &= j\omega_o L_{\rm tank} + R_s + \frac{1}{j\omega_o C_{\rm gs}}\\ &= j\omega_o\left(L_{\rm tank} - \frac{1}{\omega_o^2 C_{\rm gs}}\right) + R_s\\ &= j\omega_o L_{\rm tank}\left(1-\frac{1}{\omega_{\rm no}^2}\right) + R_s, \qquad \omega_{\rm no} = \frac{\omega_o}{\omega_{\rm sr}}\end{aligned} \tag{7}$$

$$= j\omega_o L_{\rm eq} + R_s, \qquad L_{\rm eq} = L_{\rm tank}\left(1-\frac{1}{\omega_{\rm no}^2}\right). \tag{8}$$

In (8), $L_{\rm eq}$ is the equivalent inductance of the equivalent series LR circuit. From (8), the equivalent Q factor, i.e., $Q_{\rm eq}$, of the series LR circuit at the oscillation frequency is given as

$$Q_{\rm eq} = \frac{\lfloor j\omega_o L_{\rm eq}\rfloor}{R_s} = \frac{|j\omega_o L_{\rm tank}|}{R_s}\left(1-\frac{1}{\omega_{\rm no}^2}\right) = Q_{\rm sr}\left(\frac{\omega_{\rm no}^2-1}{\omega_{\rm no}}\right). \tag{9}$$

Using (9), for given oscillation frequency $\omega_o = \omega_{\rm no}\omega_{\rm sr}$, the equivalent parallel tank resistance $R_{\rm tank}$ is derived as

$$R_{\rm tank} = \left(Q_{\rm eq}^2+1\right)R_s = \left\{\left[Q_{\rm sr}\left(\frac{\omega_{\rm no}^2-1}{\omega_{\rm no}}\right)\right]^2+1\right\}R_s. \tag{10}$$

From (8) and (10), the equivalent one-port oscillator circuit with the parallel $R_{\rm tank}\|L_{\rm eq}\|C_L$ tank circuit is given as shown in Fig. 5(b), where the substrate parasitics and active inductance has been omitted.

III. Phase Noise in the Proposed C-Colpitts Oscillator

According to Leeson's [7] and Hajimiri and Lee's [3] phase-noise model, there are two components that contribute to phase noise, i.e., phase perturbation and amplitude fluctuation. In the low-offset frequency, the phase noise is dominated by the phase perturbation term. According to Hajimiri and Lee's phase-noise model, in the $1/f^2$ region, the phase noise is given as [3]

$$L(\Delta\omega) = \frac{1}{R_{\rm tank}q_{\rm max}^2}\frac{2kT\Gamma_{\rm rms}^2}{\Delta\omega^2}. \tag{11}$$

In (11), $R_{\rm tank}$ is the equivalent resistance of the parallel tank circuit. $q_{\rm max}$ is the maximum charge swing across the equivalent tank capacitance $C_{\rm tank}$ of the parallel tank circuit. If the maximum voltage swing of the tank circuit is represented as

$V_{\max}$, then $q_{\max} = C_{\tan k} \times V_{\max}$. $\Gamma_{\rm rms}$ and $\Delta\omega$ is the rms value of the impulse sensitivity function and the offset frequency for phase-noise measurement, respectively. From (11), it is obvious that the phase noise can be improved by maximizing $q_{\max}$ of the parallel tank capacitance.

In the conventional negative-G_m oscillator, it is known that a constant negative conductance is provided over a wide frequency range for the given bias current. Interestingly, as can be seen in Fig. 3, the negative conductance of the proposed C-Colpitts oscillator shows significant changes over the operation frequency. Since the bigger negative conductance requires a more bias current, the equivalent dc-bias current of the C-Colpitts oscillator can be derived for the given oscillation frequency. Assuming the long-channel MOSFET, the equivalent dc-bias current $I_{\rm DCeq}$ in a steady oscillation condition of C-Colpitts can be easily derived using (4) as follows:

$$\begin{aligned}|G_r(\omega_n)| &= mG_{m0} \\ &= m(g_{mn} + g_{mp}) \\ &= \sqrt{2\mu_n C_{{\rm ox}\,n}\frac{W_n}{L_n} m^2 I_{\rm DC}} + \sqrt{2\mu_p C_{{\rm ox}\,p}\frac{W_p}{L_p} m^2 I_{\rm DC}}\end{aligned}$$

where

$$m = \frac{\omega_{\rm no}^2 - 1}{\left(1-\omega_{\rm no}^2\right)^2 + \left(\dfrac{\omega_{\rm no}}{Q_{\rm sr}}\right)^2} \tag{12}$$

$$I_{\rm DCeq} = m^2 I_{\rm DC} = \frac{\left[\omega_{\rm no}^2 - 1\right]^2}{\left[\left(1-\omega_{\rm no}^2\right)^2 + \left(\dfrac{\omega_{\rm no}}{Q_{\rm sr}}\right)^2\right]^2} I_{\rm DC} \tag{13}$$

where $\mu_n, \mu_p, C_{{\rm ox}\,n}, C_{{\rm ox}\,p}, W_n, W_p, L_n$, and L_p is the mobility, oxide capacitance, channel width, and channel length of the NMOS and PMOS transistors, respectively, and $I_{\rm DC}$ is the bias current.

Using (13) and (10), the maximum voltage swing $V_{\max}$ can be derived as

$$\begin{aligned}V_{\max} &= I_{\rm DCeq} R_{\tan k} \\ &= \frac{\left(\omega_{\rm no}^2 - 1\right)^2 \left\{\left[Q_{\rm sr}\left(\dfrac{\omega_{\rm no}^2 - 1}{\omega_{\rm no}}\right)\right]^2 + 1\right\}}{\left[\left(\omega_{\rm no}^2 - 1\right)^2 + \left(\dfrac{\omega_{\rm no}}{Q_{\rm sr}}\right)^2\right]^2} I_{\rm DC} R_s.\end{aligned} \tag{14}$$

From (6), the drain loading capacitance C_L can be represented as the function of $\omega_{\rm no}$ as

$$C_L = C_{\rm gs}\frac{1}{\omega_{\rm no}^2 - 1}. \tag{15}$$

From (14) and (15), the maximum charge swing $q_{\max}$ across the drain loading capacitance is given as

$$\begin{aligned}q_{\max} &= C_L V_{\max} \\ &= C_L I_{\rm DCeq} R_{\tan k} \\ &= \frac{\left(\omega_{\rm no}^2 - 1\right) \left\{\left[Q_{\rm sr}\left(\dfrac{\omega_{\rm no}^2 - 1}{\omega_{\rm no}}\right)\right]^2 + 1\right\}}{\left[\left(\omega_{\rm no}^2 - 1\right)^2 + \left(\dfrac{\omega_{\rm no}}{Q_{\rm sr}}\right)^2\right]^2} I_{\rm DC} R_s C_{\rm gs}.\end{aligned} \tag{16}$$

Finally, using (10), (11), and (16), the phase noise of the proposed C-Colpitts oscillator in the $1/f^2$ region is derived as

$$\begin{aligned}&L(\Delta\omega) \\ &= \frac{2kT\Gamma_{\rm rms}^2 \left[\left(\omega_{\rm no}^2 - 1\right)^2 + \left(\dfrac{\omega_{\rm no}}{Q_{\rm sr}}\right)^2\right]^4}{I_{\rm DC}^2 R_s^3 C_{\rm gs}^2 \left(\omega_{\rm no}^2 - 1\right)^2 \left\{\left[Q_{\rm sr}\left(\dfrac{\omega_{\rm no}^2 - 1}{\omega_{\rm no}}\right)\right]^2 + 1\right\}^3} \frac{1}{\Delta\omega^2}.\end{aligned} \tag{17}$$

In (17), the channel noise, $1/f$ noise, hot carrier effect, and the nonlinear characteristics of the CMOS device are not included. From (17), it can be seen that $L(\Delta\omega) = f(Q_{\rm sr}, \omega_{\rm no}, I_{\rm DC})$.

To verify the above argument, a simulation is carried out for the C-Colpitts oscillator, as shown in Fig. 1(a) using 0.35-μm CMOS technology with 2.0 V and 2.93 mA of supply voltage and bias current. The width of the NMOS and PMOS transistor is 150 and 300 μm, respectively. The overall capacitance from the gate source is 1.645 pF, which includes the intrinsic gate–source capacitance of NMOS and PMOS transistor and an ideal 1 pF at gate-to-ground.

The inductor is 5 nH with 3 Ω of series resistance. By changing the drain loading capacitance C_L, the oscillation frequency is controlled. Simulation shows $Q_{\rm sr}$ and $\omega_{\rm sr}$ of 14.66 and 1.755 GHz, respectively. Using the circuit parameters and $\Gamma_{\rm rms} = 0.5$, the phase-noise performance from phase-noise equation (17) and circuit simulation at 100-kHz offset frequency is plotted in Figs. 6 and 7, as a function of $\omega_{\rm on} = \omega_o/\omega_{\rm sr}$. As was previously discussed, since the noise of the tank resistance is only considered, the phase-noise performance from (17) differs from the circuit simulation result. The channel noise, $1/f$ noise, hot carrier effect, and the nonlinear characteristics of the CMOS device are not considered in (17).

As shown in Fig. 6, the higher $Q_{\rm sr}$ leads to lower phase noise, and the phase noise is improved as ω_o approaches $\omega_{\rm sr}$. As ω_o approaches $\omega_{\rm sr}$, the negative conductance and loading capacitance increase at the same time, which leads to an increase in the maximum charge swing across the oscillator tank and, therefore, the phase noise improves. From Fig. 6, the best phase noise is achieved near the peak of $G_r\ (\omega_n)$ (see Fig. 3). When ω_o approaches near $\omega_{\rm sr}$, the phase noise decreases abruptly as

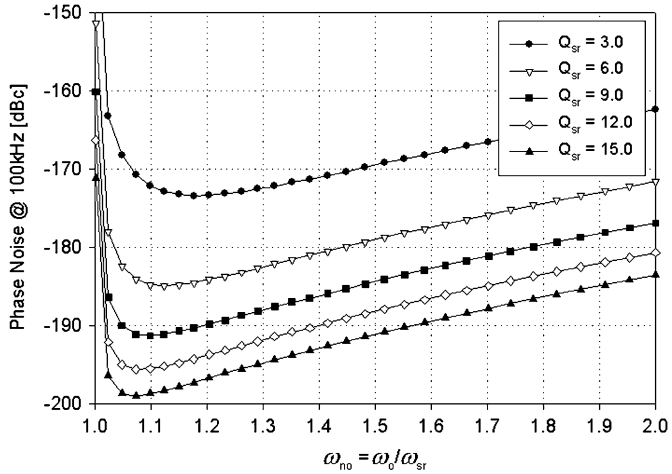

Fig. 6. Phase noise at 100-kHz offset frequency from (17).

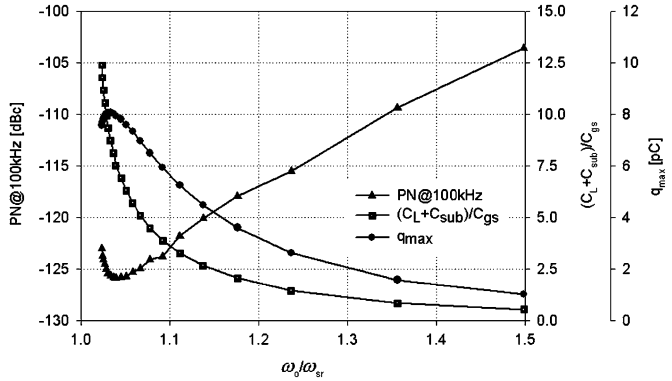

Fig. 7. Simulated phase noise at 100-kHz offset frequency.

the negative conductance quickly decreases (see Fig. 3). However, both the phase noise characteristics shown in Figs. 6 and 7 are well matched in behavior over the oscillation frequency and achieve the minimum phase noise at the almost same frequency region. As discussed in Section II, with ω_o approaching $\omega_{\rm sr}$, the phase difference between the gate and drain node in Fig. 1(a) approaches 90°, which means that the cyclo-stationary phase-noise contribution of the MOSFET can be suppressed [4]. In the proposed C-Colpitts oscillator, the loading capacitance can be larger than that of the negative-G_m oscillator since a greater negative conductance is provided with the same power consumption. In other words, the phase noise that can be achieved is better than that of the negative-G_m oscillator.

Fig. 7 plots the phase-noise performance at the offset frequency of 100 kHz, the ratio between the drain loading and gate–source capacitance, and the maximum charge swing as a function of $\omega_o/\omega_{\rm sr}$. In Fig. 7, the phase-noise behavior shows nearly the same behavior as what is predicted in Fig. 6. The difference in the slope of Fig. 7 compared to Fig. 6 may have resulted from the complex combination of the supply voltage pushing to the output swing, and the nonlinearity of active devices for the large-signal swing.

IV. VCO Design and Experimental Results

To evaluate the phase-noise characteristics of the C-Coplitts oscillator described in Section III, the C-Colpitts oscillator

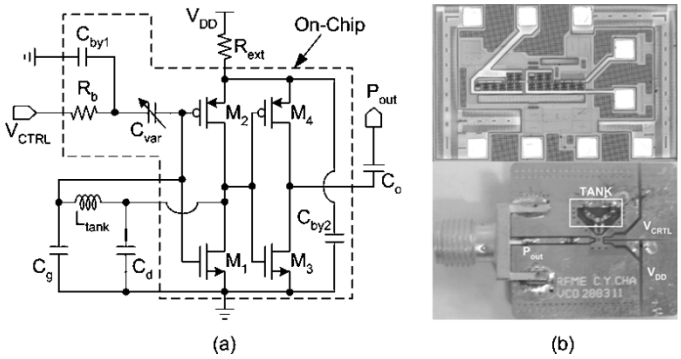

Fig. 8. (a) Test circuit of C-Colpitts oscillator. (b) Core chip micrograph (top) and VCO module (bottom).

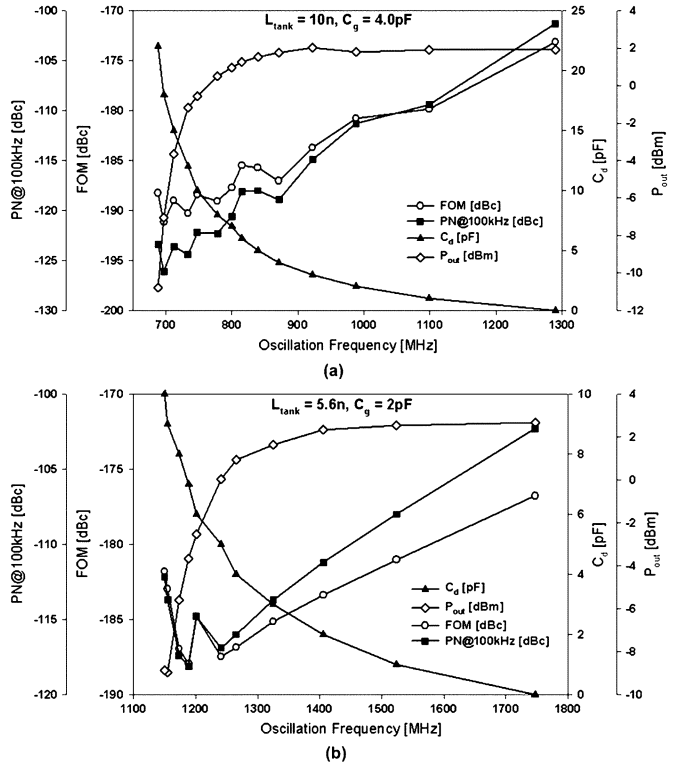

Fig. 9. Measurement results. (a) $L_{\rm tank} = 10$ nH, $C_g = 4$ pF. (b) $L_{\rm tank} = 5.6$ nH, $C_g = 2$ pF.

schematic shown in Fig. 8(a) is composed as a test module with a C-Colpitts core chip and external chip components, as shown in Fig. 8(b). In Fig. 8(a), M_1 (NMOS), M_2 (PMOS), C_g, C_d, and $L_{\rm tank}$ constitute the C-Colpitts oscillator, and M_3 (NMOS) and M_4 (PMOS) constitute the inverter buffer. $C_{\rm var}$ is an accumulation-mode varactor, and $C_{\rm by1}, C_{\rm by2}$ and C_o are the bypass and coupling capacitor, respectively. The C-Colpitts core is integrated using 0.35-μm CMOS technology. The performance of the VCO module is measured with 2.5 V of supply voltage and $R_{\rm ext} = 110\ \Omega$ by changing the value of C_d for the given $V_{\rm ctrl}, L_{\rm tank}$, and C_g. DC current flows from 4.3 to 6.3 mA, which has approximately 40% of variation depending on the value of C_d.

Fig. 9(a) and (b) shows measured performances for the case of (a) $L_{\rm tank} = 10$ nH and $C_g = 4$ pF and (b) $L_{\rm tank} = 5.6$ nH and $C_g = 2$ pF over the oscillation frequency. In Fig. 9(a), the

TABLE I
MEASUREMENT RESULTS WITH $L_{\rm TANK} = 10$ nH AND $C_G = 4$ pF

C_d [pF]	Frequency [MHz]	Power [dBm]	PN@100k [dBc]	Current [mA]	FOM [dBc]
0	1290	1.91	-101.3	4.37	-173.13
1	1099	1.90	-109.4	4.33	-179.87
2	988	1.78	-111.3	4.41	-180.77
3	922	2.04	-114.9	4.51	-183.68
4	871	1.77	-118.9	4.66	-187.04
5	839	1.51	-118.0	4.77	-185.71
6	815	1.26	-118.1	4.86	-185.48
7	800	0.95	-120.6	4.94	-187.75
8	778	0.51	-122.3	5.07	-189.09
10	747	-0.55	-122.2	5.33	-188.42
12	733	-1.19	-124.4	5.51	-190.31
15	712	-3.65	-123.6	5.84	-189.00
18	697	-7.05	-126.1	6.09	-191.14
22	688	-10.8	-123.4	6.18	-188.26

TABLE II
MEASUREMENT RESULTS WITH $L_{\rm TANK} = 5.6$ nH AND $C_G = 2$ pF

C_d [pF]	Frequency [MHz]	Power [dBm]	PN@100k [dBc]	Current [mA]	FOM [dBc]
0	1747	2.66	-102.3	4.35	-176.78
1	1524	2.52	-108.0	4.63	-181.02
2	1406	2.34	-111.2	4.77	-183.39
3	1325	1.64	-113.7	5.01	-185.16
4	1265	0.92	-116.0	5.23	-186.88
5	1241	0.05	-116.9	5.40	-187.47
6	1201	-2.54	-114.8	5.74	-184.82
7	1189	-3.67	-118.1	5.87	-187.95
8	1173	-5.61	-117.4	6.07	-186.97
9	1155	-8.96	-113.71	6.30	-182.98
10	1150	-8.86	-112.17	5.73	-181.82

capacitance of C_d ranges 0(open) $\sim$ 22 pF and the oscillation frequency covers from 688 MHz ($C_d = 22$ pF) to 1290 MHz ($C_d =$ open). In Fig. 9(b), the capacitance of C_d ranges from 0(open)$\sim$10 pF and the oscillation frequency covers from 1150 ($C_d = 10$ pF) to 1747 MHz ($C_d =$ open).

In both cases, measuring $Q_{\rm sr}$ and $\omega_{\rm sr}$ of the $L_{\rm tank}$–C_g branch is impossible. However, from the measurement results in Fig. 9(a) and (b), the frequency of $\omega_{\rm sr}$ can be estimated as approximately 688 and 1150 MHz.

Even though the measurement results in Fig. 6(a) and (b) are not as normalized as $\omega_o/\omega_{\rm sr}$, both measured results are well matched with the phase-noise trend of the previous plots in Figs. 6 and 7. The best phase-noise performance is achieved near the frequency of the estimated $\omega_{\rm sr}$, 688 and 1150 MHz, respectively. Since the oscillation frequency changes over the value of C_d, the power-frequency normalized figure-of-merit (FOM) is provided for an objective performance comparison. As shown in Fig. 9, the FOM also follows the same trend with the phase-noise property, as shown in Fig. 6. In Tables I and II, the measurement results are summarized.

Fig. 10 shows another complete schematic of the proposed C-Colpitts oscillator applied for a VCO, which includes a directly coupled inverter as a buffer. In Fig. 10, $C_{\rm var}$ represents an accumulation-mode MOS varactor, R_b represents the ac blocking resistor, and $C_{\rm by}$ represents the bypass capacitor to an ac ground. In Fig. 10, the varactor is connected on the gate side of the oscillator core in order to obtain a wider tuning range.

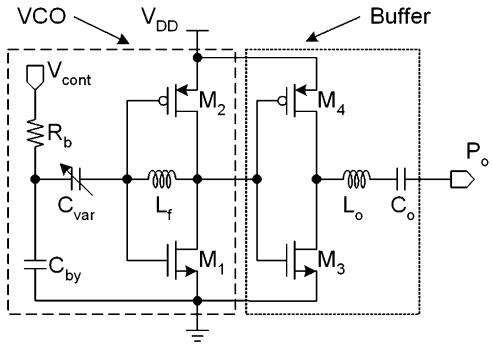

Fig. 10. Complete VCO schematic of the proposed C-Colpitts oscillator.

TABLE III
MEASUREMENT RESULTS OF THE PROPOSED C-COLPITTS VCOS AND OTHER PUBLICATIONS

Ref.	V_{DD} [V]	I_{DC} [mA]	PN [dBc]	Freq. [GHz]	Power [dBm]	FOM [dBc]	Tech. [μm]
F. 12(d)	3.3	15.0*	-114	10.5	+ 0.5	-180.5	0.35
F. 12(c)	3.3	15.0*	-121.7	6.9	+ 5.1	-183.8	0.35
F. 12(b)	2.5	8.93*	-118.9	5.9	+ 1.8	-183.8	0.35
F. 12(b)	2.0	4.63*	-118.1	6.0	- 2.5	-187.0	0.35
F. 12(a)	2.0	4.66*	-123.2	2.53	+ 1.8	-184.6	0.35
F. 12(a)	1.5	2.42*	-116.5	2.55	- 3.4	-182.1	0.35
[2]	1.5	4.7**	-117	5.35	-	-183.1	0.25
[8]	2.5	2**	-112	5.8	+ 0.9	-180.3	0.25
[9]	2.5	5.5**	-114	5.0	-	-176.6	0.25
[10]	2.7	4.0**	-110	4.7	-	-173.1	0.35

* Half of the bias current is considered as VCO core current
** VCO core current only

L_o and C_o are added for impedance matching and dc blocking. Several VCOs with different frequencies of oscillation, i.e., 2-, 5-, 6-, and 10-GHz bands, have been fabricated based on 0.35-μm CMOS technology. With 2- and 10-GHz-band VCOs, the inductors are implemented as an external printed circuit board (PCB) spiral and on-chip bond wire, respectively, while on-chip spiral inductors are used for the 5- and 6-GHz-band VCOs.

The performances of the VCOs are evaluated for various power dissipations by changing the supply voltage. Table III summarizes the measurement results in comparison with other reported 5-GHz-band VCOs. The fabricated VCOs were not optimized for minimum phase noise following analysis, as described in Section III. However, the fully integrated 5- and 6-GHz-band VCOs, shown in Table III, present better performances than that of the corresponding previous study that is implemented using 0.25-μm CMOS technology, as they are designed closer to the optimum point. With the 2-GHz design, the loading capacitance is significantly smaller (only around 0.5 pF) than the optimum point, which leads to higher phase noise.

Fig. 11 shows the measurement result of the phase noise at 6 GHz. In Fig. 9, the phase noise at 1-MHz offset is -118.1 dBc while dissipating 4.6 mA of current from a 2.0-V supply. Fig. 12 shows the micrograph of the fabricated VCOs: 2-, 5-, 6-, and 10-GHz bands, respectively.

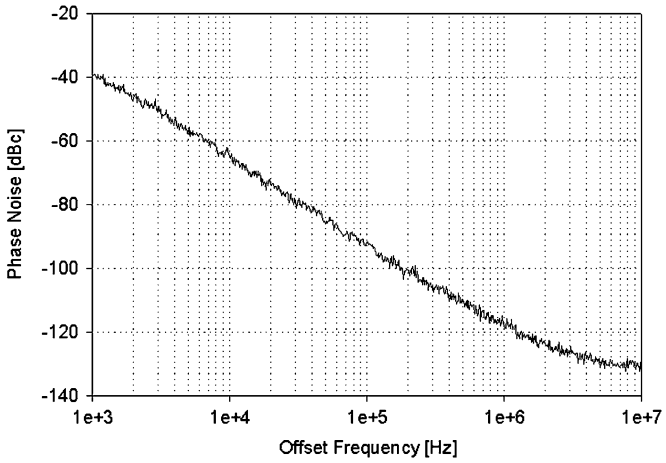

Fig. 11. Measured phase noise at 6.0 GHz as a function of offset frequencies.

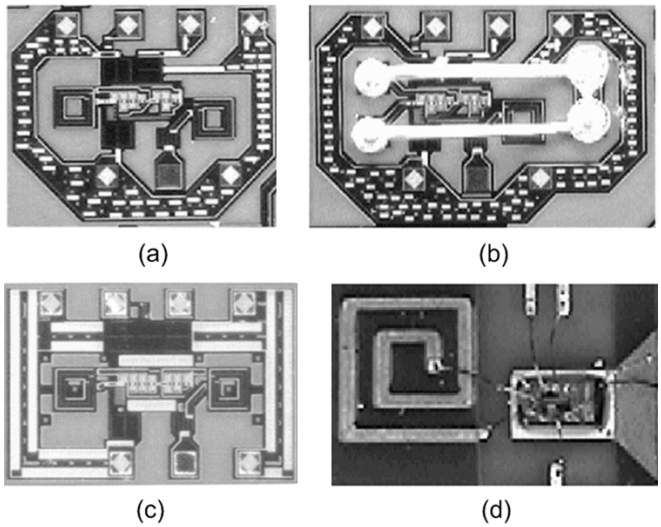

Fig. 12. Micrograph of fabricated oscillator. (a) 2-, (b) 5-, (c) 6-, and (d) 10-GHz bands.

V. Conclusion

A new C-Colpitts CMOS oscillator topology is proposed and the oscillation mechanism based on a small-signal one-port oscillator model is analyzed. The one-port analysis shows that the large negative conductance originated from the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ resonance network can be provided in the proposed C-Colpitts oscillator, which has a peak near the $\omega_{\rm sr}$ of the series R_s–$L_{\rm tank}$–$C_{\rm gs}$ network. Considering the simple and complementary structure and the generation of high negative conductance in the proposed C-Colpitts oscillator, it is adequate for high-performance oscillation in high frequency or with low power.

Based on the result of the one-port analysis and reported phase-noise model, the phase-noise equation of the proposed C-Colpitts oscillator is derived as a function of the oscillation frequency, Q factor of tank circuit , and bias current. The derived phase-noise equation shows that the best phase noise can be achieved by adjusting the oscillation frequency of the proposed Colpitts oscillator near the peak frequency of the negative conductance. Through the simulation and measurement, it is proven that the derived phase-noise property of the proposed Colpitts oscillator has good correlation.

Several VCOs of 2-, 5-, 6-, and 10-GHz bands are fabricated using 0.35-μm CMOS technology. Even though the fabricated VCOs were not optimized for the low phase-noise performance following the design guideline in Section III, the 5- and 6-GHz-band VCO shown in Table I presents better performances than that of the corresponding previous work that is implemented using 0.25-μm CMOS technology. The measured phase noise of 6.0 GHz @1-MHz offset is -118.1 dBc while dissipating 4.6 mA of current from a 2.0-V supply.

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