FREQUENCY-CONTROLLABE IMAGE RERECTION DOWN CMOS MIXER

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Abstract — **This paper presents a low noise frequency controllable image rejection mixer in heterodyne architecture for 2 GHz applications based on 0.18 μm CMOS technology. The designed mixer uses an inductor and capacitors as a notch filter to suppress the image signal and parasitic capacitance to improve the noise figure (NF) and conversion gain. Two small value capacitors in parallel with an inductor are used for precise tuning the desired image frequency. An image rejection of 20-70 dB is obtained in a 200MHz of bandwidth around 2GHz with IF varying from 100 to 300MHz. The simulation results show single-side band (SSB) NF improved 3.7 dB, the voltage conversion gain of 14.7 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.**

I. INTRODUCTION

The heterodyne architecture, shown in Fig. 1, is widely used in wireless receivers since this architecture has the high and stable performance [1,2]. In the heterodyne architecture, the major problem is suppressing the interfering image frequency component, which is 2IF away from the RF signal. After the frequency translation from the down-conversion mixer, the unwanted image signal and wanted RF signal both lie in the IF band and cannot be distinguished. The image signal appears to be noise or interference, it may be much larger than the desired signal and therefore significantly degrades the system sensitivity. The way to deal with image problem is to suppress the image signal before down conversion. Currently, off-chip passive filers, such as surface acoustic wave (SAW) filters or ceramic filters, are used for image rejection. These filters cause the integration problem, increased weight and complexity for the wireless systems, hence increase the cost.

Image rejection mixer is a way to overcome the problem from those off-chip filters, increasing the integration level. In [3,4], image rejection mixer using phase cancellation is developed. Those polyphase filters are utilized but they are very sensitive to gain and phase mismatch. The image rejection level is from 25-35 dB, far from the 60-80 dB requirement of image rejection in different wireless standards. Moreover, poly phase filter is often used in cascade structure with the combination of several stages to obtain enough bandwidth, so it is very complex, consuming more power and sensitive for design.

By utilizing a simple circuitry consisting of an inductor and capacitors, the novel image rejection mixer is introduced. To suppress the image signal exactly at its frequency, a small value capacitor is inserted in parallel with the inductor. With the availability of monolithic inductors, it is possible to implement such a simple circuit filter with no added power consumption.

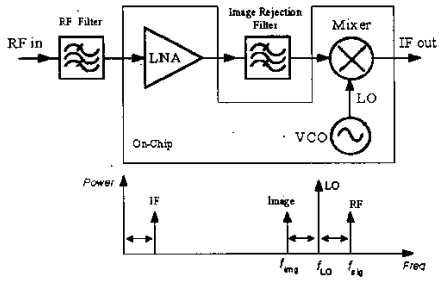

Fig 1. A heterodyne receiver

Not only suppressing the image signal, the designed mixer also eliminates the parasitic capacitance at the common-source nodes of the mixer switching stage. That leads to the further improvement in NF, conversion gain and linearity.

For further requirements on image rejection level of existing wireless systems, additional rejection can be achieved by combining an on-chip image filter [1,5] with this image rejection mixer.

In this paper, a simple low noise image rejection (IR) mixer with controllable frequency of image rejection in heterodyne architecture for 2GHz applications based on 0.18 μm CMOS technology is introduced. The designed mixer uses series inductor and capacitors as a notch filter to suppress the image signal and parasitic capacitance to improve the noise figure (NF) and conversion gain. Two small varactors in parallel with an inductor are used for precise tuning the desired image frequency. An image rejection of 20-70 dB is obtained in a 200MHz of bandwidth from 1.9 to 2.1GHz with local oscillator (LO) frequency of 1.8GHz. The simulation results show single-side band (SSB) NF is improved about 3.7 dB, the voltage conversion gain of 14.7 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.

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II. THE ANALYSIS

For the simplicity, single balanced mixer is used for illustration of the proposed circuit technique. In Fig. 2(a), LC tank circuit is inserted. The series resonant frequency of the LC tank is chosen at the image frequency. The transfer function of the LC circuit is:

$$Z_f(s) = \frac{1}{sC_1} + sL_1 = \frac{s^2 L_1 C_1 + 1}{sC_1} \quad (1)$$

$$f_{img} = \frac{1}{2\pi\sqrt{C_1 L_1}} \quad (2)$$

At the image frequency (f_{img}), Z_f is zero, so LC tank steals the current away from showing up at the output and reduces the gain at that frequency. Thus, image signal is suppressed.

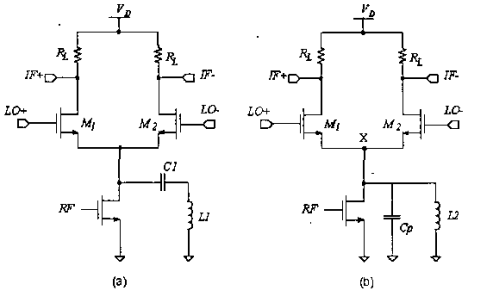

Fig. 2. Illustration of single balanced mixer for (a) image rejection, (b) parasitic capacitance suppression

However, the mixer topology shown in Fig. 2 has some drawbacks due to the parasitic capacitance at the drain node X of the switching transistors pair M_1-M_2. The parasitic capacitance (C_p) lowers the impedance at node X, leading to the reduction of the transconductance, RF signal loss and cause the noise such that the conversion gain and NF of mixer are degraded. To restrict the bad effect of C_p on NF and conversion gain, C_p must be nullified. An inductor is inserted in parallel with C_p to overcome the drawback caused by this parasitic capacitance, Fig. 2(b). The parallel resonant frequency of LC tank is determined equal to the RF signal. At RF signal frequency, node X has the highest impedance, in other words, lowest amount of signal leaks through C_p.

$$Z_f(s) = \frac{1}{sC_p} // sL_2 = \frac{sL_2}{s^2 L_2 C_p + 1} \quad (3)$$

$$f_{sgn} = \frac{1}{2\pi\sqrt{C_p L_2}} \quad (4)$$

From the above analysis, a solution circuit showned in Fig. 3 is introduced which can deal with the both two mentioned problems.

The proposed circuit includes a series LC tank, C_3 and L_3, and a small variable capacitor C_e, shown in Fig.3. Its function is similar to a notch filter. This filter will have the low impedance at the image frequency and high impedance at the frequency of signal.

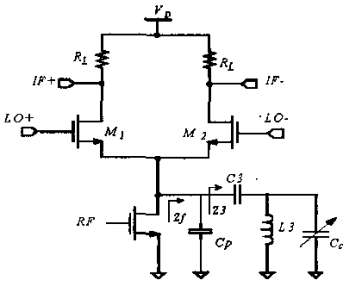

Fig. 3. Image rejection and parasitic capacitance single balanced mixer

For precise tuning the image frequency, C_e is added in parallel with L_3. The input impedance of the filter can be derived and expressed as follows:

$$Z_f = Z_3 // \frac{1}{sC_p} \quad (5)$$

$$\text{where} \quad Z_3 = \frac{1}{sC_3} + sL_3 // \frac{1}{sC_e}, \text{ and } s = j\omega \quad (6)$$

$$Z_f(s) = \frac{s^2 L_3(C_3 + C_e) + 1}{s^3 C_3 L_3 C_e + s^3 L_3 C_p (C_3 + C_e) + sC_3 + sC_p} \quad (7)$$

Z_f is a function of frequency, near the zero frequency, the filter has low impedance and near the pole, high impedance is observed.

From (7), the frequency of the zero is

$$\omega_z = \frac{1}{\sqrt{L_3(C_3 + C_e)}} = \frac{1}{\sqrt{L_3 C_e + L_3 C_3}} \quad (8)$$

The zero frequency is understood as the image frequency.

The frequency of the pole is

$$\omega_p = \sqrt{\frac{C_3 + C_p}{L_3 C_p (C_3 + C_e) + L_3 C_3 C_e}} \quad (9)$$

$$\omega_p = \frac{1}{\sqrt{L_3 C_e + L_3 C_3 \dfrac{C_p}{C_3 + C_p}}} \quad (10)$$

The pole frequency corresponds to signal frequency. From (8) and (10), the pole and zero gap is controlled by the ratio of C_p over C_3. For correct and effective image rejection, the image frequency or zero must be chosen at the precise frequency. By slightly changing the value of C_e, the suppression of image is achieved at the desired image frequency. The value of C_e is much smaller than C_3. For given RF signal frequency, we can determine the image frequency, and then using (8) and (10) together with simulation, the values of L_3 and C_3 are determined.

II. THE PROPOSED MIXER DESIGN

The double-balanced Gilbert-type mixer topology shown in Fig.5 is preferred in CMOS mixer design since it suppresses the LO signal and the even order distortion products at the output.

Double balanced mixer consists of two single balanced mixers. When applying the circuit technique mentioned above for double balanced mixer, two LC circuits are put in series and symmetric. The two LC circuits like in Fig. 2(a) can be simplified by using only one common inductor L_i with two capacitors C_i at the two ends, shown in Fig. 4. That is because, for double balanced mixer, the input signal is the differential, hence the middle point of L_i is considered as the virtual ground. We have the equivalent circuit transform as follows:

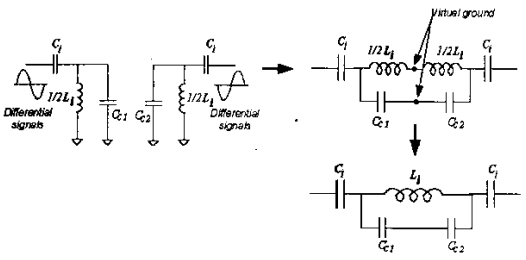

Fig 4. Tranformation of two differential LC circuits

Figure 5 introduces a novel image rejection mixer with the proposed image rejection filter. The value of L_i is twice the value of L_3. From the simulation, L_i is determined a 6.4nH on-chip inductor. From the RF signal and image frequencies, C_i is calculated according to equations (8) and (10), it is chosen as a 2.7pF capacitor. C_{c1} and C_{c2} are small value varactors for precise tuning image frequency, they are controlled by V_c. In Fig. 6, by varying V_c, the values of these varactors (C_c) are changed, having the values of 0.25, 0.3 and 0.35pF corresponding to the center frequencies of image signal at 1.6, 1.614 and 1.63GHz, respectively. At image frequency of 1.614GHz corresponding to RF signal frequency of 1.986GHz, the notch is deepest. With 55.6 dB of attenuation at image frequency and 14.7 dB of gain at band pass, highest image rejection ratio of 70.3 dB is achieved.

In this design, current bleeding technique is utilized, PMOS transistors M_7 and M_8 create the bleeding currents under the gate bias voltage as shown in Fig. 3. With the bleeding technique, the current through switching transistor is reduced by steering part of drive stage current from the switching transistors, such that the output load resistance is increased leading to a higher conversion gain. It also improves the switching efficiency that leads to lower NF [6].

The filter not only reject the image signal but also suppressed the parasitic capacitances at the common-source nodes of the switching transistor, as well as the effects of current through it. The conversion gain and NF of the mixer are improved [7,8].

Furthermore, with the image rejection filter, the impedance at twice the signal frequency is lower, in other words the current components at the high order harmonic frequencies, especially second harmonic, and intermodulation products running through common-source nodes of switching transistors are reduced partly, as a result, IIP2 is improved [9].

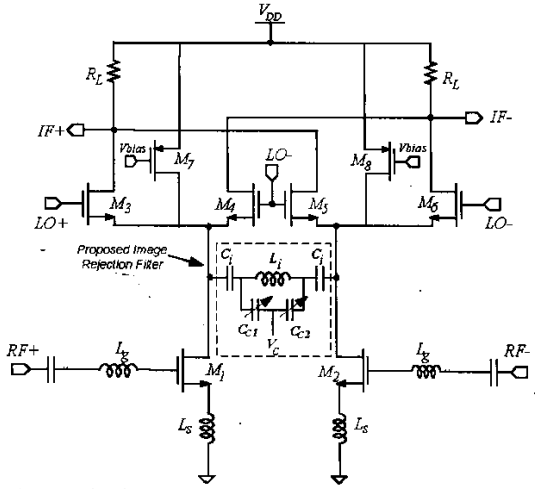

Fig. 5. The down-conversion mixer topology with proposed image rejection filter

L_g and L_s are for input impedance matching at 50 Ohm, L_s inductor is the bonding wire, it helps decrease the noise figure and increase the third order input intercept point (IIP3) [10].

IV. SIMULATION RESULTS AND DISCUSSION

The proposed mixer in Fig. 5 is simulated in a TSMC 0.18 μm CMOS process by Cadence. The results are shown below.

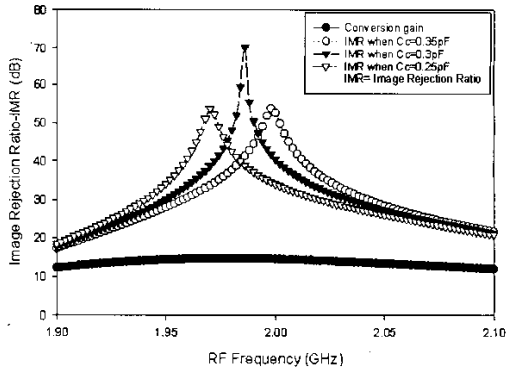

Fig 6. Image Rejection Ratio and Conversion gain versus RF frequency

With the presence of the proposed image rejection filter, the parasitic capacitances at the common-source nodes of the switching transistors are eliminated, therefore the RF signal loss through C_p can be avoided, and higher gain can be achieved.

Moreover, all the negative effects of C_p on NF, high order intermodulations such as IIP2, IIP3 are also eliminated [9]. For the proposed IR-mixer, simulation shows IIP3 of -4.3 dB, improved by 1.9 dB, shown in Table 1.

The voltage conversion gain is improved by around 4 dB due to the elimination of C_p. In Fig. 6, the simulation shows the conversion gain is 14.7dB at center frequency band when image rejection filter is used. Image rejection level is ranging from 20 –70 dB in the wide band-with of 200MHz. For narrow bandwidth centered around 2GHz, the rejection level reaches about 50 dB and the peak reaches 70.3 dB of image rejection.

The peak of the image rejection characteristic corresponds to the zero frequency as analyzed in equation (8). Changing the value of C_e will help us choosing the right image frequency.

The most effective and very impressive improvement in the designed mixer when utilizing image rejection filter is on the noise.

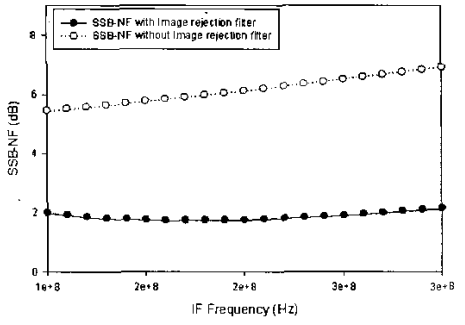

Fig. 7. SSB- NF with and without image rejection filter

For the down mixer in the heterodyne architecture, the main noise contribution come from the side-band noise translation, from RF band and image band to IF. Hence, when the image rejection filter is used, the image band noise is suppressed, the noise performance of the mixer is clearly improved. Figure 7 shows the SSB-NF performance of the mixer with and without using the image rejection. About 4 dB of improvement is obtained. The simulated NF is surprisingly small, probably due to the modeling inaccuracy, but the trend of improvement in NF showed in Fig. 7 is more important, it proved the effect of the filter on the image rejection and as a result, NF is improved.

The performances of the proposed mixer are summarized in Table 1.

TABLE. 1
MIXER PERFORMANCE COMPARISION

Parameters	Without Filter	With Filter
Input IP3 (dBm)	-6.2	-4.3
Voltage Conversion Gain (dB)	10	14.7
SSB NF (dB)	5.7	2
Image Rejection level (dB)	-	20 - 70
Image/Signal Frequency (GHz)	1.5 – 1.7 / 1.9 –2.1	
Supply Voltage (V)	1.8 (TSMC 0.18μ)	
Power Consumption (mW)	11.34	

V. CONCLUSION

Image rejection is the main problem in heterodyne architecture. To avoid using off-chip filter to increase the integration level, reduce the cost and complexity of receiver, the new image rejection mixer topology was designed. By adding a simple circuitry of inductor and capacitors, not only suppresses the image signal, the designed mixer also eliminates the parasitic capacitance at the common-source nodes of the mixer switching stage. Two small varactors in parallel with the inductor are used for precisely controllable image suppression at the desired image frequency. The mixer topology, designed and manufactured in 0.18 μm CMOS process, shows an excellent performance, particularly in image rejection ratio and NF. The image rejection level is from 20–70 dB in a wide bandwidth of 200MHz around 2GHz. The proposed tunable IR-mixer is suitable for wireless applications where high degree of integration is desirable.

The simulation results show single-side band (SSB) NF of 2 dB, improved about 3.7 dB, the voltage conversion gain of 14.7 dB, improved by more than 4 dB. The circuit operates at the supply voltage of 1.8V, and dissipates 11.34 mW.

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