Ultra-wideband CMOS low noise amplifier

C.-W. Kim, M.-S. Jung and S.-G. Lee

A two-stage ultra-wideband CMOS low noise amplifier (LNA) is proposed. The first stage is optimised for wideband input matching and low noise figure, while the second stage is optimised to extend the −3 dB bandwidth of the overall amplifier. The combination of stages can provide lower noise figure and wider bandwidth simultaneously over that of previously reported feedback-based CMOS amplifiers. The implemented LNA shows a peak gain of 13.5 dB, more than 8.5 dB of input return loss, and a noise figure of 2.5–7.4 dB over a −3 dB bandwidth from 2 to 9 GHz with DC power consumption of 25.2 mW.

Introduction: Because of recent technology trends towards multi- and wideband wireless communication systems, the design of a wideband low noise amplifier (LNA) has become a research interest for many. In particular, with technology scaling, CMOS wideband LNAs have shown excellent performance [1–3].

In wideband amplifier topologies, the resistive shunt-feedback topology [2, 3] has been extensively used because of its superior broadband characteristics. However, this topology has a well-known trade-off between noise figure and −3 dB bandwidth (also wideband input matching). The −3 dB bandwidth of the shunt-feedback topology can be given by

$$\omega_{-3\,\mathrm{dB}} = [1 + A_v]/[R_f(C_{gs} + (1 + A_v)C_{gd})] \quad (1)$$

where A_v is the open-loop gain of the amplifier, R_f the shunt-feedback resistor, and C_{gs} and C_{gd} the parasitic capacitances of the input transistor. As shown in (1), higher A_v and smaller R_f lead to wider −3 dB bandwidth. However, because of noise figure degradation, smaller R_f is not a desirable approach. Therefore, high A_v allows for not only wider bandwidth, but also lower noise figure. However, in CMOS technology, because of poor transconductance, higher A_v requires a large DC current. In this Letter we report a two-stage UWB CMOS LNA, which adopts shunt-series feedback and stagger-tuning technique for the first stage and second stage, respectively, in order to achieve high gain, low noise and wide bandwidth simultaneously.

Circuit design: Fig. 1 shows the proposed two-stage UWB CMOS LNA. In Fig. 1, the first stage adopts a shunt-series feedback for wideband input matching and low noise figure. The second stage uses a shunt-peaking load [4] to extend the −3 dB bandwidth of the overall amplifier. In the Figure, an output buffer is added for measurement purposes.

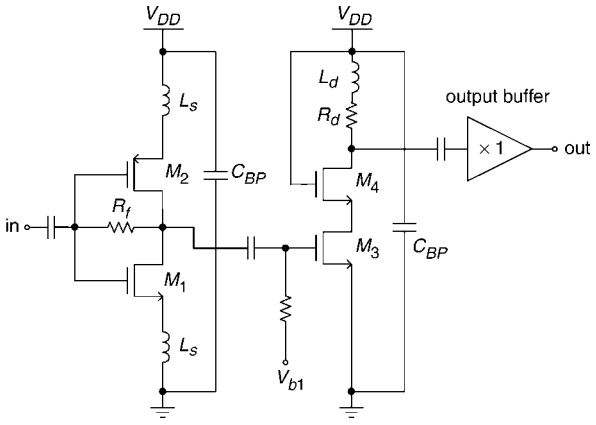

Fig. 1 *Circuit schematic of proposed LNA*

To increase the open-loop voltage gain with low DC power, the first stage of the proposed LNA adopts an inverter configuration (M_1, M_2 and L_s) with shunt feedback resistor R_f. The first stage can provide higher total transconductance ($g_{m1} + g_{m2}$). This allows higher R_f for the given −3 dB bandwidth, which leads to lower noise figure. The total noise figure of the proposed two-stage amplifier in Fig. 1 is dominated by the first stage. However, the large input parasitic capacitances of the first stage due to the Miller effect can lead to degradation in input impedance (below 50 Ω) and −3 dB bandwidth at high frequencies. To overcome this problem, two on-chip spiral inductors L_s are adopted for the partial tuning-out of the input parasitic capacitances. In the second stage of the LNA, a cascode amplifier (M_3, M_4, L_d and R_d), a shunt-peaking inductor L_d is added for additional bandwidth extension [4]. By optimising the size of L_d and R_d, the second stage compensates for the gain roll-off of the first stage at high frequencies and also provides good flatness over the frequency band of interest.

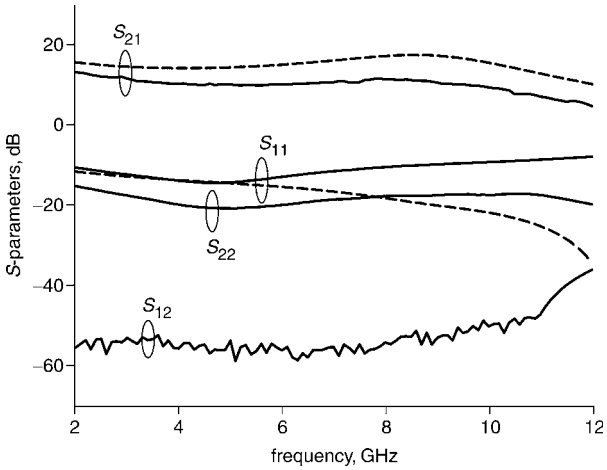

Fig. 2 *Measured and simulated S-parameters*
——— measured – – – – – simulated

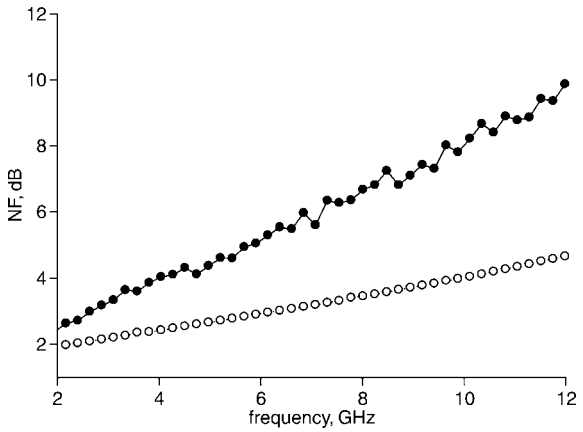

Fig. 3 *Measured and simulated noise figure*
-●-●-●- measured -○-○-○- simulated

Measurement results: The proposed two-stage LNA shown in Fig. 1 is optimised to cover full UWB band (3.1–10.6 GHz) based on 0.18 µm CMOS technology. From Fig. 1, the first stage is self-biased from the feedback resistor R_f, while the second stage is biased by an external voltage source (V_{b1}). Two MOS-capacitors C_{BP} (20 pF) are used to maintain a constant bounce between V_{DD} and ground. All inductors are implemented as on-chip elements ($L_s = 0.5$ nH and $L_d = 0.6$ nH), and designed and modelled with an electromagnetic simulator. Fig. 2 shows the on-wafer S-parameter measurement results of the fabricated UWB CMOS LNA along with the simulated S_{11} and S_{21}. In Fig. 2, the measured S_{21} shows a peak gain of 13.5 dB with −3 dB bandwidth from 2 to 9 GHz, which is much better than that of previously reported feedback-based CMOS amplifiers [2, 3]. Also, the measured S_{11} and S_{22} are better than −8.5 and −15 dB, respectively, over the −3 dB bandwidth. The degradation of measured S_{11} and S_{21}, compared to the simulation, is presumably caused by the improper modelling of the two inductors L_s and L_d. Fig. 3 shows the measured noise figure of 2.5, 3.3, 4.5, 7.4 and 8 dB, at 2, 3, 5, 9 and 10 GHz, respectively. The discrepancy between measurement and simulation in noise figure is due to the degradation of power gain (S_{21}) compared to the simulation, and the inaccurate noise model of the transistor. The input referred IP3 is tested at 4 and 4.5 GHz and shows −5.4 dBm. The measured performances of the wideband amplifier are summarised in Table 1

and compared with the simulation results. The proposed LNA excluding the output buffer draws 14 mA from a 1.8 V supply. Fig. 4 shows the microphotograph of the fabricated UWB CMOS LNA with a chip size of 0.87 mm^2.

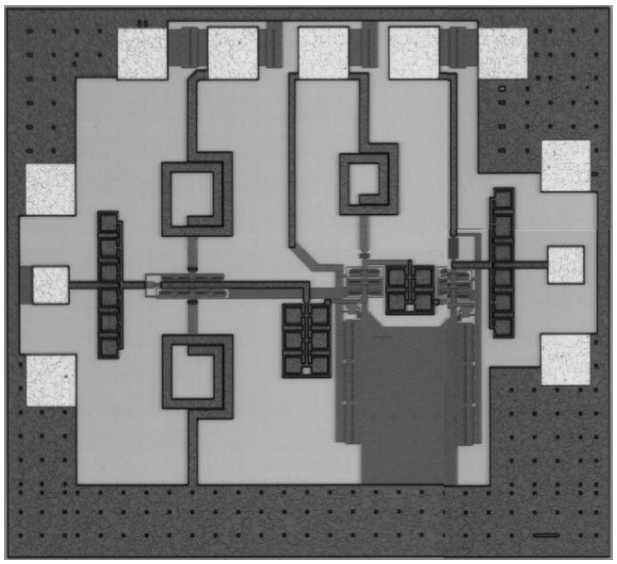

Fig. 4 *Chip photograph of LNA (1000 × 870 μm)*

Table 1: Summary of measured and simulated LNA performances

Parameter	Simulated	Measured
$BW_{-3\ dB}$	2–10 GHz	2–9 GHz
S_{11}	> −12 dB	> −8.5 dB
S_{22}	> −15 dB	> −15 dB
S_{21}	14.5–17.5 dB	10.5–13.5 dB
S_{12}	> −73 dB	> −50 dB
NF	1.9–4 dB	2.5–7.4 dB
IIP3	−7.2 dB	−5.4 dB
DC power	25.2 mW	25.2 mW

Conclusions: The design and measurement results of the two-stage UWB CMOS LNA, which is implemented in 0.18 μm CMOS technology, are presented. From a combination of shunt-series feedback and shunt-peaking technique, the implemented two-stage CMOS LNA can provide lower noise, wideband input matching, and wider −3 dB bandwidth, simultaneously. The measurement results show a −3 dB bandwidth of 2–9 GHz, a peak gain of 13.5 dB, more than 8.5 dB of input return loss, higher than 15 dB output return loss, and noise figure of 2.5–7.4 dB over a −3 dB bandwidth, while dissipating 14 mA from a 1.8 V supply.

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C.-W. Kim, M.-S. Jung and S.-G. Lee (*School of Engineering, Information and Communications University, 119 Munjiro, Yuseong-gu, Daejeon 305-732, Korea*)

E-mail: cwkim@icu.ac.kr

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