Ultra-low-power 2.4 GHz image-rejection low-noise amplifier

T.-K. Nguyen, S.-K. Han and S.-G. Lee

An ultra-low-power image-rejection low-noise amplifier (IR-LNA) for 2.4 GHz ZigBee applications based on 0.18 μm CMOS technology is presented. By using the third-order active notch filter the proposed IR-LNA can achieve high image-rejection ratio. Measurements show 12 dB gain, 1.8 dB noise figure, 38 dB image-rejection, −3 dBm input third-order intercept point, −18 and −19 dB input and output return loss while dissipating 0.6 mA from a supply voltage of 1.5 V.

Introduction: With the introduction of IEEE 802.15.4 ZigBee standard [1], the demands for low-cost, low-power and small-size wireless transceivers has been increased significantly. The superhererodyne architecture is the most widely used architecture in modern handsets [2]. However, the most critical problem in the superhererodyne architecture is image signal suppression which is typically done by off-chip filters leading to high cost. Therefore, improving the image-rejection ratio with an on-chip integrated circuit is the most active research topic in superhererodyne architecture implementation. In this Letter, an ultra-low-power 2.4 GHz image-rejection low-noise amplifier (IR-LNA) for ZigBee applications is introduced. By using an on-chip third-order active notch filter the proposed IR-LNA can achieve high image-rejection ratio.

Circuit design: The proposed IR-LNA shown in Fig. 1 consists of two parts: the LNA core and the third-order active notch filter. As can be seen from Fig. 1, the LNA core differs by one additional capacitor, C_{ex}, in comparison with the conventional inductive degeneration cascode LNA topology. This LNA topology was used to obtain the noise figure equal to the noise figure minimum of the given LNA topology under very low power consumption [3]. In Fig. 1, the DC bias of M_1, size of M_1 (W_1), C_{ex} and L_s are chosen following the design principle of the power-constrained simultaneous noise and input matching technique introduced in [3], and L_g is inserted for the input matching to the signal source impedance of 50 Ω. A simple L_o-C_o network is used to match the output impedance of the IR-LNA.

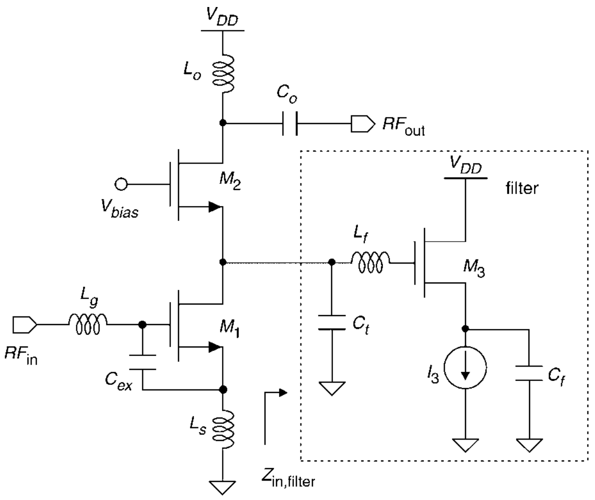

Fig. 1 *Schematic of IR-LNA*

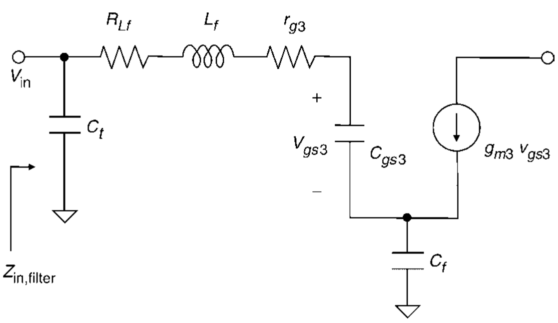

Fig. 2 *Small-signal equivalent circuit of notch filter*

Fig. 2 shows the small-signal equivalent circuit of the proposed third-order active notch filter alone. As can be seen from Fig. 2, the input impedance of the filter, $Z_{in,filter}$, is given by

$$Z_{in,filter} = \frac{1}{j\omega C_t} // Z_1 \tag{1}$$

where

$$Z_1 = j\omega L_f + \frac{1}{j\omega}\left(\frac{1}{C_{gs3}} + \frac{1}{C_f}\right) - \frac{g_{m3}}{\omega^2 C_{gs3} C_f} + R_{Lf} + r_{g3} \tag{2}$$

Note that the negative term in the right-hand side of (2) represents the negative resistance (proportional to g_{m3}) seen at the gate of transistor M_3. Thus, by adjusting g_{m3} by means of the bias current I_3, sufficient negative resistance can be generated to cancel R_{Lf} and r_{g3}. Therefore, the quality factor of this filter is not affected by the quality factor of an on-chip inductor, i.e. the proposed notch filter topology can achieve a very high quality factor regardless of a low quality factor of an on-chip inductor.

Assuming that all the parasitic components are cancelled, $Z_{in,filter}$ is re-expressed as

$$Z_{in,filter} = \frac{s^2 L_f C_{eq} + 1}{s(s^2 C_t L_f C_{eq} + C_t + C_{eq})} \tag{3}$$

Here

$$\frac{1}{C_{eq}} = \frac{1}{C_{gs3}} + \frac{1}{C_f}$$

From (3), the image and wanted signals are located at

$$f_{im} = \frac{1}{2\pi\sqrt{L_f C_{eq}}}$$

and

$$f_{wanted} = \frac{1}{2\pi\sqrt{1/L_f(1/C_t + 1/C_{eq})}} \tag{4}$$

At the image frequency, $Z_{in,filter}$ looking into the filter is minimised such that the entire image signal will be extracted from the original path. Conversely, at the wanted frequency, $Z_{in,filter}$ is maximised such that the wanted signal is not extracted from the original path. As a result, the image signal is suppressed while the wanted signal is not degraded. The proposed IR-LNA is fabricated in a standard 0.18 μm CMOS technology. Fig. 3 shows the microphotograph of the fabricated IR-LNA with a chip area of 0.56 mm^2.

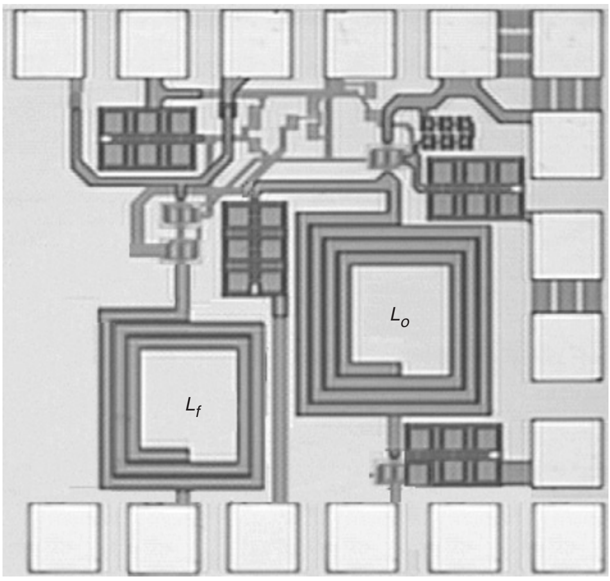

Fig. 3 *Microphotograph of fabricated IR-LNA*

Measured results: The proposed IR-LNA is optimised for 2.4 GHz ZigBee and a local oscillator signal of 2 GHz for 400 MHz intermediate frequency. Fig. 4 shows the measured *S*-parameters and NF results of the proposed IR-LNA. As can be seen from Fig. 4, the proposed IR-LNA exhibits 12 dB gain, 38 dB image-rejection, −18 dB input return loss, −19 dB output return loss, and 1.8 dB NF. Fig. 5 shows the measured third-order nonlinearity (IIP3) of the proposed IR-LNA. For the IIP3 measurement, two tones were applied with equal power levels at 2.4 and 2.41 GHz. As can be seen from Fig. 5, the obtained result of IIP3 is about −3 dBm. The proposed IR-LNA dissipates 0.6 mA from a 1.5 V supply.

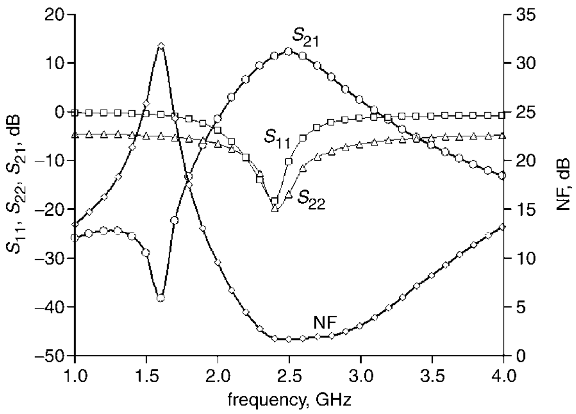

Fig. 4 *Measured S-parameters and NF of IR-LNA*

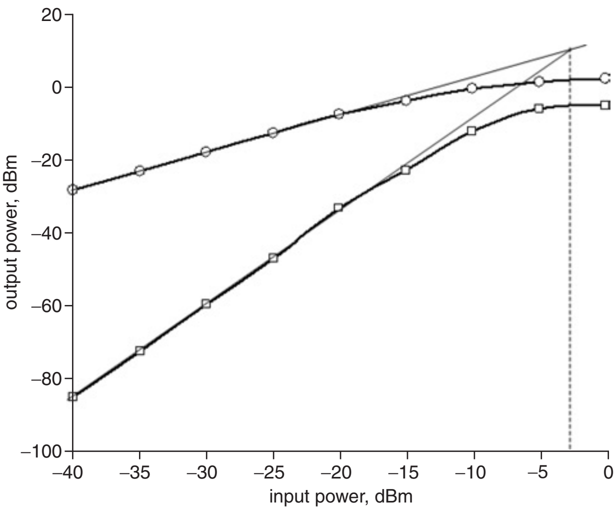

Fig. 5 *Measured IIP3 of IR-LNA*

Conclusion: An ultra-low-power image rejection LNA is designed for 2.4 GHz ZigBee applications based on 0.18 μm CMOS technology. Using the proposed on-chip third-order active notch filter very high image-rejection ratio is achieved. The IR-LNA exhibits 12 dB gain, 1.8 dB NF, 38 dB image rejection, and −3 dBm IIP3 while dissipating 0.6 mA from a 1.5 V supply.

Acknowledgment: This work was supported by the Research Institute of Ubiquitous Bio-Information Technology, South Korea.

4 April 2005

Electronics Letters online no: 20051032

doi: 10.1049/el:20051032

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