

11-GHz CMOS Differential VCO With Back-Gate Transformer Feedback

Nam-Jin Oh and Sang-Gug Lee

Abstract—A fully integrated back-gate transformer feedback CMOS differential voltage-controlled oscillator (VCO) has been designed for high-frequency and low-phase noise operation using an 0.18- μm CMOS process. The proposed VCO topology utilizes the monolithic transformer feedback configuration from the drain to the back-gate of the switching transistors in VCO. The VCO operating in an 11-GHz band shows the phase noise of -109 dBc/Hz at 1-MHz offset, and draws around 3.8 mA in the differential core circuits from a 1.8-V power supply.

Index Terms—Back-gate, CMOS, monolithic transformer, phase noise, voltage-controlled oscillator (VCO).

I. INTRODUCTION

AMONG the building blocks of a wireless transceiver, the voltage-controlled oscillator (VCO) is an important block since it affects the system performances of the transceiver to a large extent. Presently, passive monolithic transformers have been integrated into radio-frequency integrated circuits (RFICs) such as an image-reject mixer, a VCO, and a passive balun, especially for low-power designs [1], [2].

Recently, literature on transformer-based LC VCOs has been published [3]–[6]. Since the transformer-based LC tank has a higher quality factor than that of a single LC tank, a lower phase noise of a VCO can be achieved. Until recently, most of literature published has dealt with transformer-based CMOS LC VCOs below 8 GHz.

In this paper, a new transformer-based differential VCO is presented by utilizing a back-gate feedback operating at a frequency of 11 GHz. In this topology, the signal at the tank feeds back through the body terminal (sometimes, called the back-gate) of switching transistors.

II. TRANSFORMER FEEDBACK DIFFERENTIAL VCO

Fig. 1 shows two examples of previous works for transformer feedback oscillators. In Fig. 1(a), the drain voltage feeds back to the source terminal with an impedance transformation of n^2/g_m , where n is the number of turns of the primary winding, and g_m is the transconductance of the switching transistor, M_{sw} [7]. Since the impedance seen at the source terminal is $1/g_m$, a relatively high turns-ratio is required for the transformer to make an impedance transformation from the drain to the source, thereby entailing complexity in transformer design, making it possible to lower the oscillation frequency. In other

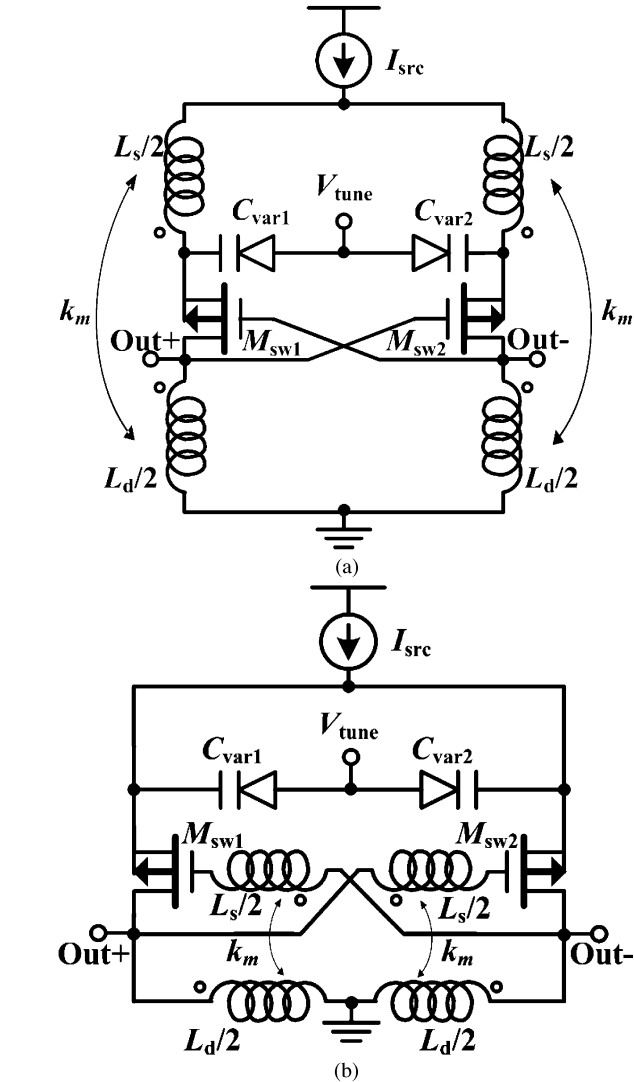


Fig. 1. Differential VCOs with (a) transformer feedback to the source and (b) transformer feedback to the front-gate.

topology, as shown in Fig. 1(b), the drain voltage feeds back to the front-gate. Since the impedance seen at the gate of the switching transistor is relatively high, the turns-ratio of the transformer can be optimized with a smaller number of turns. However, the parasitic capacitances of the transformer directly couple to the tank, and lower the oscillation frequency significantly compared to that of the transformer feedback to the source terminal. To obtain both higher frequency and simplify the transformer design (smaller number of turns-ratio), the front-gate feedback path in Fig. 1(b) can be modified to have a feedback to the back-gate.

Manuscript received April 13, 2005; revised June 9, 2005. This work was supported in part by the Korea Intellectual Property Office (KIPO). The authors are with the Department of Engineering, Information and Communications University, Daejeon 305-732, Korea (e-mail: onanjin@icu.ac.kr). Digital Object Identifier 10.1109/LMWC.2005.858994

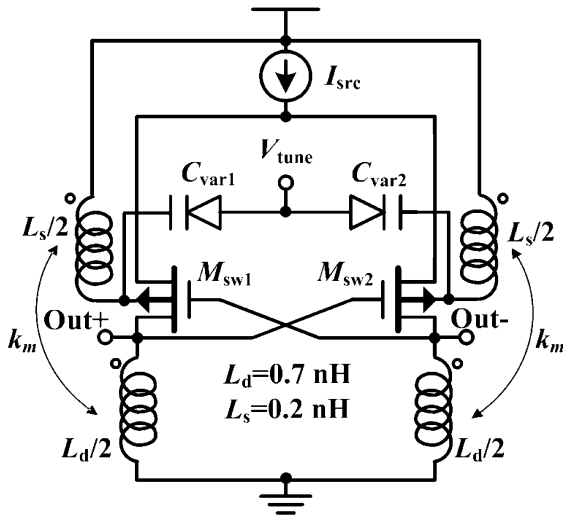


Fig. 2. Proposed differential VCO with transformer feedback to the back-gate.

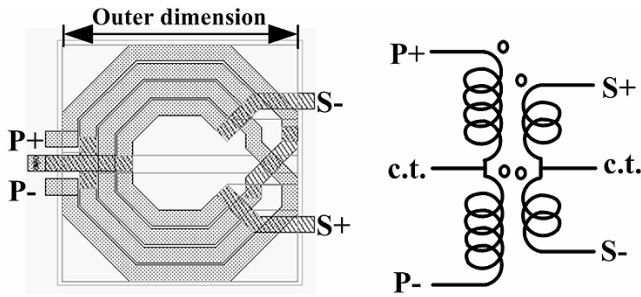


Fig. 3. Physical layout and schematic symbol of step-down symmetric transformer.

This topology can oscillate at higher frequency while keeping comparable performances compared to those of the other topologies discussed. Fig. 2 shows the proposed VCO in which the inductors, L_d and L_s , form a transformer with a coupling coefficient, k_m . To optimize the turns-ratio and size of the transformer, a circuit simulation is investigated. The turns-ratio of the transformer is determined with an ideal transformer by varying the number of turns for each topology. About a 2:1 turns-ratio is chosen which has sufficient feedback in the VCO. A lumped-element compact model is adopted to estimate the figures of merit (coupling coefficient (k_m), self-inductances of the individual windings, and self resonant frequency) of the designed monolithic transformer. The equivalent compact model can be implemented using inductors, resistors, capacitances, and an ideal transformer [1]. Since a transformer fabricated in CMOS technology has a parasitic signal loss mechanism, the model includes parasitic capacitances and dissipation in the substrate represented by shunt elements of C_{ox} , C_{sub} , and R_{sub} , where C_{ox} is the parasitic capacitance in the oxide layer, C_{sub} is the substrate capacitance, and R_{sub} is the substrate resistance. Also, it includes interwinding capacitances between the primary and secondary windings.

A 2- μm -thick top AlCu metal is used for the windings to increase the quality factor. The transformer is designed with a 10- μm metal width, 1.5- μm line spacing, and a 148- μm outer dimension as shown in Fig. 3. The simulated primary inductor

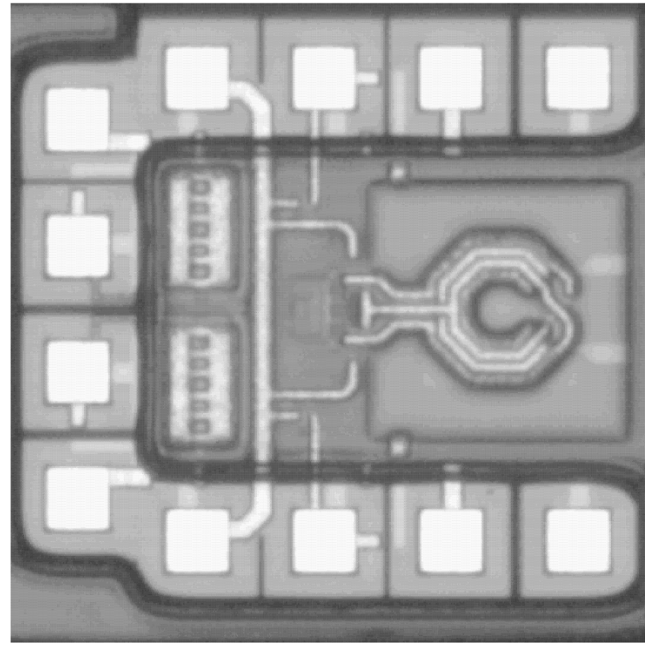


Fig. 4. Chip micrograph. The die size is $530 \times 625 \mu\text{m}^2$.

(L_d) value is 0.7 nH, and the secondary inductor (L_s) is 0.2 nH. The coupling coefficient is about 0.75. The quality factor of the inductor is about nine at the oscillation frequency. The simulated phase error between the secondary ports is almost zero at an oscillation frequency of around 11 GHz, where the phase error is the deviation from a 180° phase difference between secondary ports. Two accumulation mode MOS varactors with $n+$ polygate in n -well [8] are used for frequency tuning. The measured capacitance varies from about 500 to 1200 fF with the gate bias voltage from -0.4 V to +0.4 V, and the quality factor is around 10 at a frequency of 10 GHz. Using the given transformer, circuit-electromagnetic (EM) co-simulations have been investigated for the three topologies for a fair comparison.

The target oscillation frequency is set to around 11 GHz. Simulation results show that the proposed VCO has the same level of output swing and almost the same oscillation frequency compared to the VCO with source feedback. The VCO with front-gate transformer feedback has an oscillation frequency that is 3 GHz lower compared to those of the other topologies. In terms of phase noise, the proposed VCO performs about 10 dB better at 100-kHz offset and 5 dB better at 1-MHz offset frequency compared to the VCO with source feedback; however, it performs only 2–3 dB worse in the frequency offset ranges from 100 kHz to 10 MHz compared to the front-gate transformer feedback VCO (see Fig. 6).

III. MEASUREMENT RESULTS

Fig. 4 shows the micrograph of the proposed VCO fabricated in an 0.18- μm six-metal CMOS process. The chip size is $530 \times 625 \mu\text{m}^2$ including the pads. The phase noise of the proposed VCO is measured with a spectrum analyzer. The output spectrum of the VCO is given in Fig. 5. The tuning range is about 300 MHz with varactor tuning voltage from 1.6 to 2.0 V. The core current is about 3.8 mA from a 1.8-V

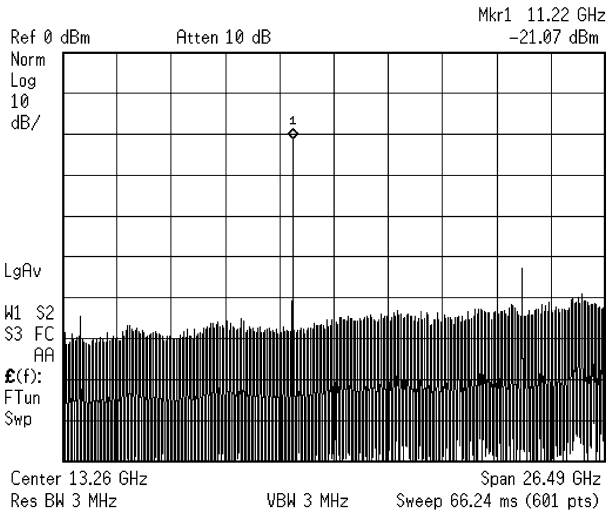


Fig. 5. Output spectrum of the proposed VCO.

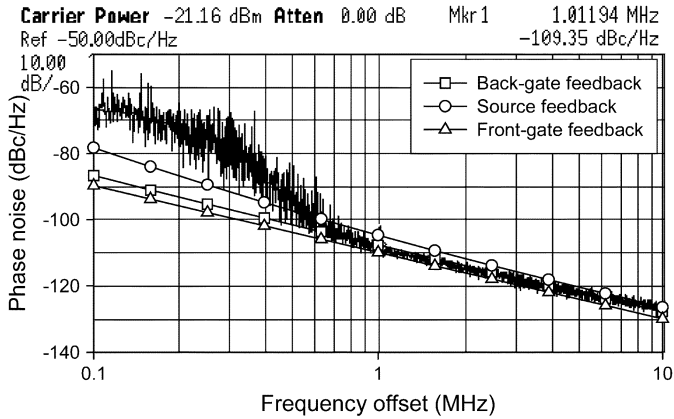


Fig. 6. Measured phase noise of the proposed VCO compared to the simulation results with different transformer feedback topologies.

power supply. As shown in Fig. 6, the measured phase noise is about -109.35 dBc/Hz at 1-MHz offset, and agrees well with the simulation result at higher frequency offsets above 600 kHz. The difference between the measured and simulated phase noise at the lower frequency offset probably results from an inaccurate noise model for RF transistors used in the VCO. The oscillation frequency of the proposed VCO is the highest among the transformer-based VCOs ever published, and the figure of merit (FOM) of the VCO is about -182 dBc/Hz. A comparison of the transformer-based VCO performances is summarized in Table I.

TABLE I
COMPARISON OF TRANSFORMER-BASED VCO PERFORMANCE [9]

Ref	f_{osc} (GHz)	V_{DD} (V)	I_{tail} (mA)	Phase Noise*	FOM (dBc/Hz)
[3]	5.00	1.6	7.5	-123.0	-186.2
[5]	8.00	3.0	8.0	-117.0	-181.7
[6]	10.00	1.8	6.6	-118.7	-187.9
[9]	5.88	1.5	5.1	-124.2	-190.7
This work	11.22	1.8	3.8	-109.4	-181.8

* dBc/Hz at 1 MHz offset

IV. CONCLUSION

A fully integrated back-gate transformer feedback CMOS differential VCO is presented for high-frequency, low-phase noise operation. The VCO utilizes the drain to back-gate transformer feedback configuration, and makes use of the quality factor improvement of the transformer-based LC tank. Fabricated in $0.18\text{-}\mu\text{m}$ CMOS technology, the VCO oscillates in an 11-GHz band. The measured phase noise of the VCO is -109 dBc/Hz at 1-MHz offset consuming around 3.8 mA from a 1.8-V power supply. The FOM of the VCO is about -182 dBc/Hz.

REFERENCES

- [1] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
- [2] D. T. S. Cheung, J. R. Long, R. A. Hadaway, and D. L. Harame, "Monolithic transformers for silicon RF IC design," *Proc. Bipolar/BiCMOS Circuits Technology Meeting*, pp. 105–108, Sep. 1998.
- [3] A. Ravi, K. Soumyanath, R. E. Bishop, B. A. Bloechel, and L. R. Carley, "An optimally transformer coupled, 5GHz quadrature VCO in a $0.18\ \mu\text{m}$ digital CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2003, pp. 141–144.
- [4] S. L. J. Gierkink, S. Levantino, R. C. Frye, C. Samori, and V. Bocuzzi, "A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1148–1154, Jul. 2003.
- [5] D. Baek, T. Song, E. Yoon, and S. Hong, "8-GHz CMOS quadrature VCO using transformer-based LC tank," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 446–448, Oct. 2003.
- [6] S. Ko, J.-G. Kim, T. Song, E. Yoon, and S. Hong, "20 GHz integrated CMOS frequency sources with a quadrature VCO using transformers," *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, pp. 269–272, Jun. 2004.
- [7] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.
- [8] A.-S. Porret, T. Melly, C. C. Enz, and E. A. Vittoz, "Design of high-Q varactors for low-power wireless applications using a standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 337–345, Mar. 2000.
- [9] T. Song, S. Ko, D.-H. Cho, H.-S. Oh, C. Chung, and E. Yoon, "A 5 GHz transformer-coupled CMOS VCO using bias-level shifting technique," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2004, pp. 127–130.