Current Reused LC VCOs

Nam-Jin Oh and Sang-Gug Lee

***Abstract*—This paper presents current reused voltage controlled oscillator (VCO) topologies by stacking switching transistors in series like a cascode. The VCOs can operate with only half the amount of dc current compared to those of the conventional VCO topologies. Fabricated in 0.18-μm CMOS process, a differential VCO operates in a 2.1-GHz band with a phase noise of −110 dBc/Hz at 1-MHz offset, and a quadrature VCO operates in a 3.1-GHz band with a phase noise of −102 dBc/Hz at 1-MHz offset. The proposed topologies can be adopted for low-power applications.**

***Index Terms*—CMOS, differential voltage controlled oscillator (VCO), phase noise, quadrature VCO (QVCO), radio-frequency (RF).**

I. Introduction

With the demand for low cost and high integration of wireless transceiver building blocks, a low-power design is a great concern for radio-frequency integrated circuit (RFIC) designers. Among the building blocks of the transceiver, a voltage controlled oscillator (VCO) is an important block. A great deal of research has focused on integrated VCOs using passive inductors, transformers, and varactors, which was made possible with the advancement of CMOS technology [1]–[4]. When evaluating performances of VCOs, several parameters such as phase noise, tuning linearity, harmonic output power, frequency pushing, output power, and power consumption need to be considered [5].

Since most of the modern day digital wireless transceivers require quadrature generations in the VCOs, many works have focused on how to generate accurate quadrature signals [6]–[8]. For quadrature signals, in-phase and quadrature-phase (I/Q) match is an important requirement while meeting the requirements of low-phase noise and low power for integrated VCOs. The quadrature characteristics can be evaluated in terms of phase error and amplitude imbalance.

There are several ways to generate the quadrature signals [7]–[13]. As shown in Fig. 1(a), the most popular method is to use a differential VCO that oscillates at twice a desired frequency, and then to obtain quadrature waveforms via frequency division. However, a higher oscillation frequency and the frequency division result in increased power consumption. Another way is shown in Fig. 1(b) in which two differential LC VCOs directly couple to obtain quadrature signals and exploit a good phase noise performance of LC-oscillators. The results of several kinds of quadrature VCO (QVCO) topologies which directly coupled two LC VCOs have been published [7]–[9]. The widely known conventional LC QVCO couples two differential LC VCOs by coupling transistors placed in parallel with switching transistors.

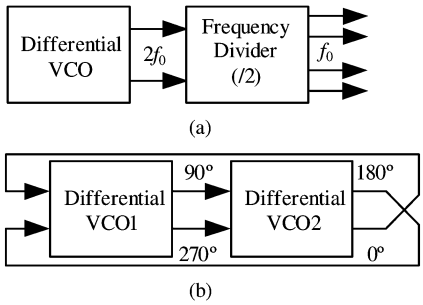

Fig. 1. Examples of quadrature signal generation methods of (a) frequency division and (b) quadrature coupling.

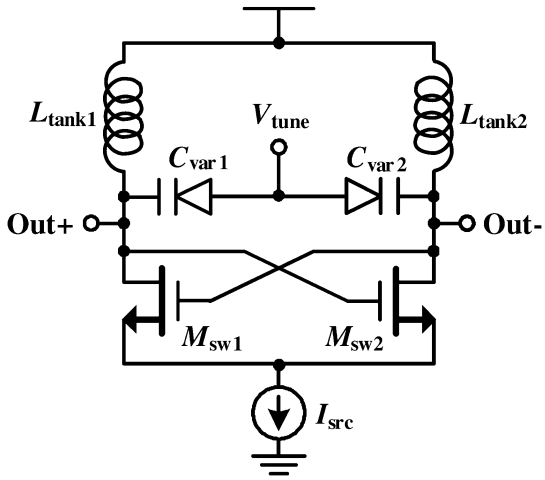

Fig. 2. Conventional differential LC VCO.

Since the differential VCO plays a key role for quadrature signal generations as shown in Fig. 1, this paper proposes a current reused differential VCO topology by stacking switching transistors in series like a cascode, and also applies the same idea to QVCO.

II. Current Reused LC VCO Topologies

A widely known oscillator is the conventional differential negative-G_m oscillator that is shown in Fig. 2 [14]. The topology consists of two identical half circuits composed of switching transistors $M_{\rm sw}$, inductors $L_{\rm tank}$, and varactors $C_{\rm var}$. A signal feeds back from the drain of $M_{\rm sw1}(M_{\rm sw2})$ to the gate of $M_{\rm sw2}(M_{\rm sw1})$ which acts as an active buffer, and vice versa. Fig. 3 shows the proposed VCOs by modifying the conventional VCO topologies for low-power applications. In Fig. 3(a), the switching n-channel metal oxide semiconductor

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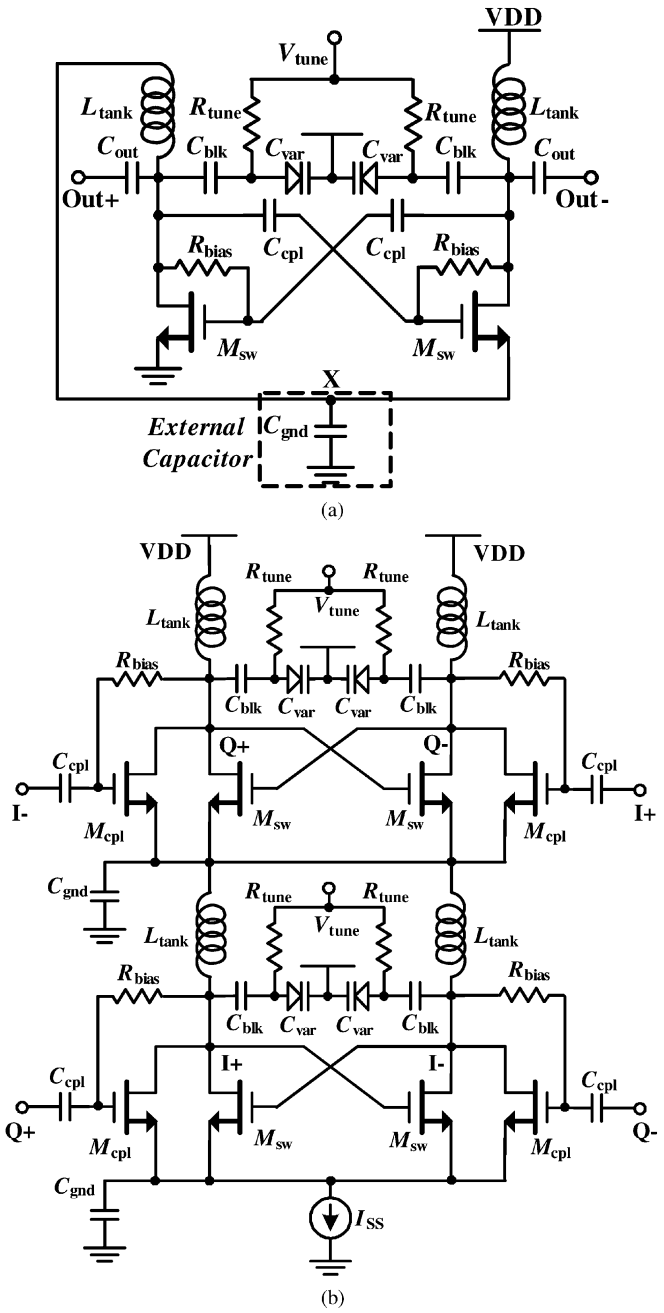

Fig. 3. Proposed topologies of (a) current reused differential VCO and (b) current reused quadrature VCO (QVCO).

(NMOS) transistors are stacked vertically in dc while constituting a differential VCO in ac operation. The capacitors $C_{\rm cpl}$ and $C_{\rm out}$ are adopted for ac coupling, $C_{\rm gnd}$ for ac ground, and $C_{\rm blk}$ for dc block and ac short, respectively. Resistors $R_{\rm bias}$ are adopted for diode connection of the switching transistors in dc while providing an open in ac operation. By comparing the schematics shown in Figs. 2 and 3(a), it can be shown that $L_{\rm tank}$, $C_{\rm var}$, and $M_{\rm sw}$ perform the same role. In ac wise, the schematic shown in Fig. 2 is exactly the same as that of Fig. 3(a). The same idea of the current reused differential VCO is applied to the QVCO in Fig. 3(b). Since the dc voltages are different between two differential output nodes in Fig. 3(b), a frequency tuning circuit is designed to control varactors by only one control voltage $V_{\rm tune}$ through resistors $R_{\rm tune}$, which is possible through capacitors $C_{\rm blk}$ for dc block and ac short.

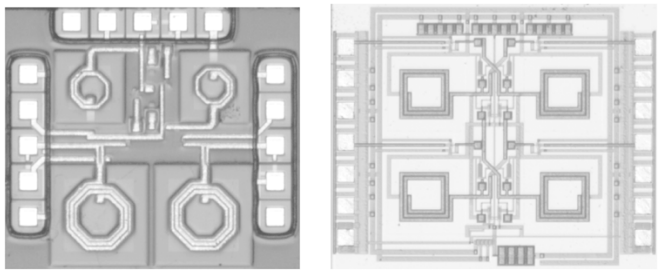

Fig. 4. Chip Micrographs of (a) current reused differential VCO ($936 \times 945\ \mu\text{m}^2$) and (b) current reused quadrature VCO ($1.3 \times 1.0\ \text{mm}^2$).

For the proposed VCOs, power consumption can be cut in half by reusing the dc current compared to the conventional VCO topologies. Although the proposed designs involve a larger number of capacitors, their sizes are not required to be bulky at higher frequencies, and can be integrated on chip. However, the ac ground capacitor in Fig. 3(a) is implemented with an external capacitor which has a large value to have a tight ground effect at node X and symmetric differential output swing. For inductors, a 2-μm-thick top metal is used to increase Q factor over ten, which is simple to design compared to a multilayer helical inductor [15]. Since different foundry processes are used for the chip fabrications, different shapes of inductors are used for each VCO with different oscillation frequency. Octagonal inductors are used in Fig. 3(a) for which a wideband inductor model is adopted to describe the decreasing inductance and drop-down characteristics of a series resistance as frequency increases [16]. Whereas, rectangular inductors are used in Fig. 3(b) for which a simple nine-element π inductor model is adopted [17].

III. Measurement Results

Fig. 4 shows micrographs of the proposed VCOs fabricated in 0.18-μm six-metal CMOS processes. The chip sizes are $936 \times 945\ \mu\text{m}^2$ and $1.3 \times 1.0\ \text{mm}^2$ including the pads, respectively. The phase noise of the proposed VCOs is measured with a spectrum analyzer. For measurements, current reused output buffers are also adopted for the differential VCO by stacking two source followers, and open drain output buffers are implemented for the QVCO. For the current reused differential VCO, the measured tuning frequency range is 2.12–2.25 GHz, and the core current is about 1 mA from an 1.8-V power supply. For the current reused QVCO, the measured tuning frequency range is 3.0–3.2 GHz, and the core current is about 2.4 mA from an 1.8-V power supply.

Fig. 5 shows the measured phase noise compared to those of the simulation. The insets in Fig. 5 show the measured spectrum and time domain output swings of the proposed VCOs. The measured phase noise of the current reused differential VCO is about -110 dBc/Hz at 1-MHz offset, and has a slope of -20 dB/dec in the frequency offset from 100 kHz to 10 MHz. The measured phase noise of the current reused QVCO is about -102 dBc/Hz at 1-MHz offset, and has a slope of -30 dB/dec

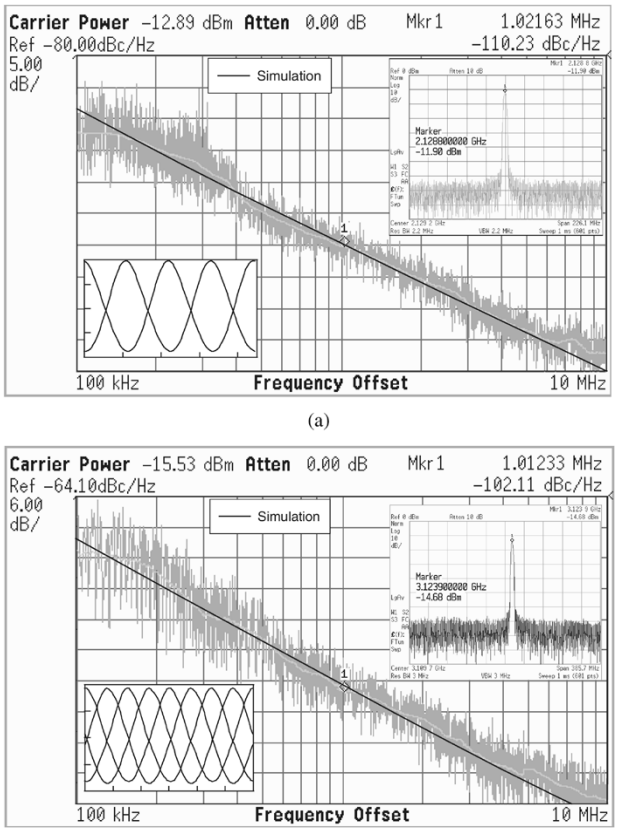

Fig. 5. Measured phase noise of (a) current reused differential VCO and (b) current reused quadrature VCO compared to the simulation. The insets show the measured spectrum of the VCOs, and simulated output swings.

TABLE I
SUMMARY OF THE CURRENT REUSED VCO PERFORMANCES AT $V_{DD} = 1.8$ V

Parameter	Differential VCO	QVCO
Technology	Samsung 0.18 μm CMOS	TSMC 0.18 μm CMOS
Core current (mA)	1	2.4
Tuning range (GHz)	2.12-2.25	3.0-3.2
Phase noise@ 1 MHz offset	-110	-102
FOM (dBc/Hz)	-174	-166

in the frequency offset from 100 kHz to 1 MHz whereas it has -20 dB/dec in the frequency offset from 1 MHz to 10 MHz. The simulated phase noise of proposed VCOs agrees well with the measurement results. The measured amplitude imbalance of the proposed QVCO is about 1 dB. The calculated figure of merits (FOM) of the VCOs are -174 dBc/Hz and -166 dBc/Hz, respectively. Table I summarizes the performances of the proposed current reused VCOs for a fair comparison with other VCOs.

IV. CONCLUSION

Current reused LC VCO topologies have been presented in this paper. By stacking the switching transistors in series like a cascode, the new proposed VCOs reuse the dc current and the current consumptions can be cut in half compared to those of conventional VCO topologies. Optimally designed current reused VCOs can be implemented to have comparable overall performances with the conventional VCOs while meeting low power requirements.

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