A CMOS 868/915 MHz Direct Conversion ZigBee Single-Chip Radio

Nam-Jin Oh and Sang-Gug Lee, Information and Communications University
Jinho Ko, Phychips Inc.

ABSTRACT

In this article the 868/915 MHz radio transceiver specifications have been derived for IEEE 802.15.4, a low-rate, low-cost, and low-power network standard. The radio specifications include parameters such as noise figure, nonlinearity, channel filtering, phase noise of local oscillator, dynamic range, and bit resolutions of analog-to-digital and digital-to-analog converters. Based on a direct conversion scheme, top-down system-level performance analyses using the radio specifications are realized. Low-power and low-cost circuit topologies are also discussed with chip implementations using 0.18 μm CMOS technology.

INTRODUCTION

Most wireless LAN standards such as IEEE 802.11 a/b/g [1–3] do not meet low-cost design objectives because of the high performance required in bit error rate (BER), range, and data rate. To meet the low cost requirement, a standard with lower performance constraints is needed to address cost-sensitive applications for industrial and commercial, home automation, personal computer (PC) peripherals, consumer electronics, personal health care, and toys and games. To this end, IEEE has recently ratified the 802.15.4 standard for operation at 868/915 MHz and 2.4 GHz [4].

This article describes a top-down system design and simulation for a 868/915 MHz ZigBee transceiver and derives a set of system-level radio specifications that meets the IEEE 802.15.4 physical (PHY) layer standard requirement. The system-level radio specifications include system noise figure, sensitivity, phase noise of local oscillator, order of channel shaping and selection filters, intermodulation characteristics, bit resolutions of analog-to-digital and digital-to-analog converters (ADC/DAC), channel rejection performances, and spectrum shaping. Circuit topologies that led to the implementation of a single-chip low-power low-cost ZigBee transceiver in 0.18 μm complementary metal oxide semiconductor (CMOS) technology are also discussed.

The research is supported in part by the IT-SoC Center under the Korea IT Industry Promotion agency (KIPA)

PHY SPECIFICATIONS

In comparison to other wireless LAN standards such as IEEE 802.11 a/b/g, ZigBee PHY specifications are much more relaxed, as shown in Table 1. For example, the low transmit power of 1 mW enables a simpler output power amplifier with reduced chip size and low power consumption. Moreover, with ample channel spacing, adjacent or alternate channel rejection can be achieved with low order integrated filters. This results in further reduction of power consumption, chip size, and cost. Also, the system noise figure (NF) is relaxed by exploiting the processing gain provided by direct sequence spread spectrum (DSSS) technique [5, 6] and the short range requirement. Thereby, the required signal-to-noise ratio (SNR) is reduced, resulting in increased sensitivity for a given BER. With relaxed NF, the radio frequency (RF) front-end blocks in the receiver can be simplified, for example, by stacking the low noise amplifier (LNA) and mixer, and thus results in reduced power consumption and silicon area. Finally, the local oscillator (LO) can be designed with reduced power consumption because of the relaxed phase noise requirement.

As specified in the specifications, ZigBee devices can operate in the 2.4 GHz band worldwide or the 868 and 915 MHz bands in Europe and the United States, respectively. In terms of data rate, 250 kb/s at 2.4 GHz, 20 kb/s at 868 MHz, and 40 kb/s in 915 MHz are supported. Sixteen channels are assigned in the 2.4 GHz band with 5 MHz channel spacing, 10 channels for 915 MHz band with 2 MHz channel spacing, and only one channel for 868 MHz, respectively.

For all three frequency bands, the ZigBee standard employs DSSS that uses digital spreading based on a pseudorandom noise (PN) chip sequence. The chip rates are 300 kchips/s and 600 kchips/s for the 868 and 915 MHz bands, respectively. For the 2.4 GHz PHY, 2 Mchip/s chip rate is used for a spreading parameter. The input data is mapped onto a data symbol, and then mapped to PN chip sequences. The chip sequences are modulated onto the carrier using binary phase shift keying (BPSK) with raised cosine pulse shaping for the 868/915 MHz PHY,

0163-6804/05/$20.00 © 2005 IEEE

Standards	IEEE 802.15.4	IEEE 802.11a	IEEE 802.11b	IEEE 802.11g
Frequency band (MHz)	868–868.6/902–928 2400–2483	5150–5350	2400–2483	2400–2483
Bandwidth (MHz)	0.6/1.2 2	20	22	20
Channel spacing	0/2 5	20	25 (U.S.) 30 (Europe)	20
Transmit power (mW)	1	200	1000 (U.S.) 100 (Europe)	1000 (U.S.) 100 (Europe)
Min. sensitivity (dBm)	–92 –85	–82	–76	–76
Max. sensitivity (dBm)	–20	–30	–10	–20
Intermodulation (dBm) (signal/adjacent/alternate)	–89/–89/–59	–82/–66/–50	–70/–35/–30	–70/–35/–30
Blocking (dBm)	–30	–30	–30	–30
Noise figure (dB)	< 19	< 7.5	< 15	< 7.5
Phase noise (dBc/Hz @ 1 MHz offset)	–88	–102	–101	–102

Table 1. *Radio specifications of several standards.*

Superheterodyne architecture is a well-established transceiver architecture that has disadvantages such as requiring discrete external components, image problems, difficulties in multi-mode transceivers, high power consumption, and high cost.

and offset quadrature phase shift keying (O-QPSK) with half-sine pulse shaping for the 2.4 GHz PHY.

The modulation accuracy of ZigBee can be characterized with an error vector magnitude (EVM) measurement. The ZigBee standard requires that EVM should be less than 35 percent when measured over 1000 chips. The ZigBee standard requires that the modulated transmit power be at least –3 dBm, which is constrained by local regulatory requirements.

In the receiver path, the required sensitivity is defined as a threshold input signal power of the receiver that yields less than 1 percent packet error rate (PER). The ZigBee standard requires that the minimum sensitivity be –92 dBm for the 868/915 MHz band, and –85 dBm for the 2.4 GHz band. The ZigBee receiver should be able to receive an input level up to –20 dBm. With the transmit power of 0 dBm, the typical operational range of ZigBee applications is 10–20 m.

Transceiver Architecture

Wireless transceivers are usually implemented in the superheterodyne, low-intermediate frequency (low-IF), or direct conversion architecture [5]. Regardless of which architecture is used, quadrature mixing is generally required for most amplitude and phase/frequency modulated signals that have a quadrature component. Quadrature mixing requires shifting either the RF signal or the LO output by 90°. In either case, the amplitude of the in-phase (I) and quadrature (Q) signals are not exactly equal; nor is the phase exactly in quadrature. This is often referred to as I/Q mismatch, and corrupts the signal constellation, thereby increasing the BER.

Superheterodyne architecture is a well-established transceiver architecture that achieves good I/Q matching. In addition, it has advantages such as flexibility in frequency planning, no DC offset problems, and no LO leakage. However, it has disadvantages such as requiring discrete external components, an image problem, difficulties in the multimode transceiver, high power consumption, and high cost.

The low-IF scheme can avoid the DC offset problem and eliminate the expensive IF surface acoustic wave (SAW) filter, IF phase locked loop (PLL), and image filtering. However, it suffers from impairments such as even-order nonlinearity and LO pulling/leakage. LO pulling arises when the power amplifier output may couple to the LO in the transmit path or the desired signal is accompanied by a large interferer, thereby corrupting the LO spectrum. LO leakage arises since the isolation between the LO port and the inputs of the mixer and LNA is not perfect; thus, a finite amount of feedthrough

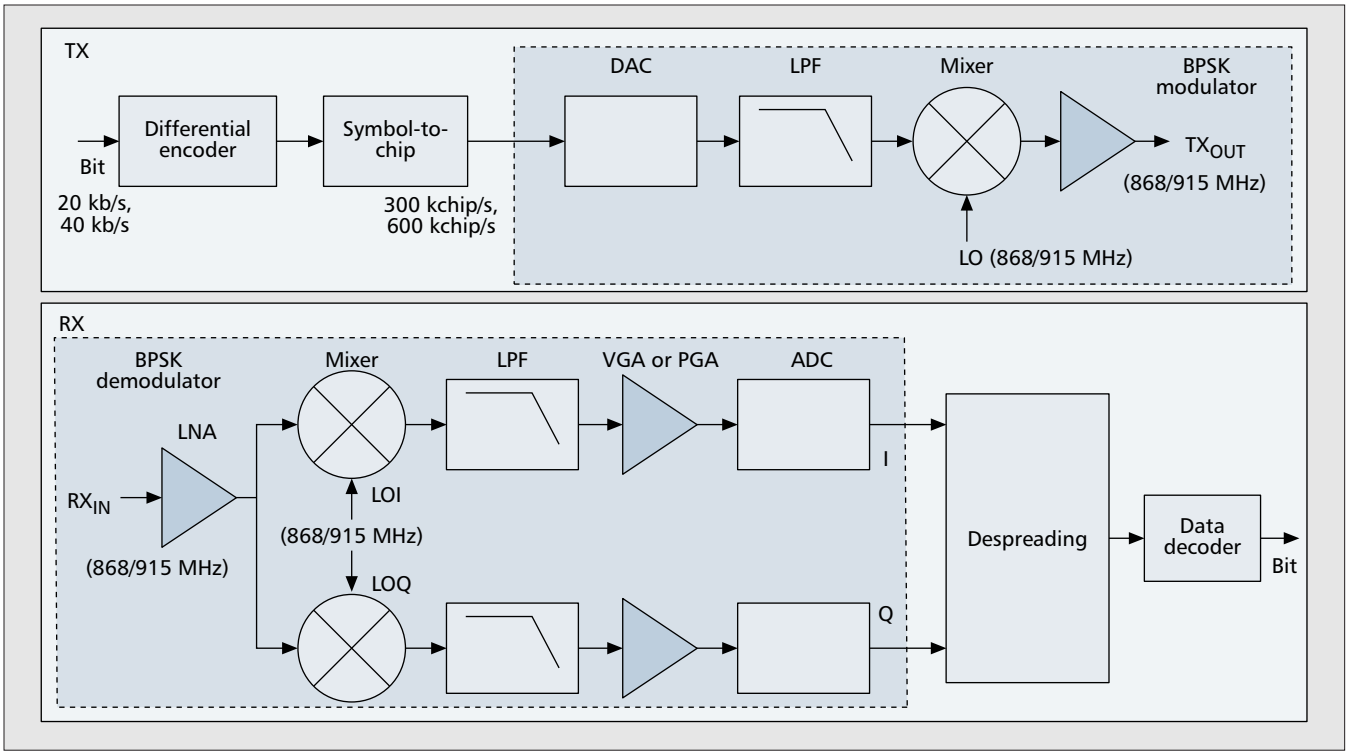

Figure 1. *868/915 MHz direct conversion ZigBee transceiver architecture.*

exists from the LO port to the other mixer input and LNA input.

Additionally, the low-IF scheme requires stringent image rejection to suppress strong adjacent channel interferers, which are images of the desired signal due to the low IF used. The image rejection in low-IF can be achieved in either the analog or digital domain. The analog solution increases the chip size and power consumption, and still requires an additional second low-frequency digital mixer. The digital solution does not increase the chip size, but requires good I/Q matching and more constraints on the analog blocks. Furthermore, the low-IF requires a high-resolution ADC with higher sampling rate to digitize not only the desired signal but also the interferer, which results in increased design complexity and high power consumption.

In contrast to the low-IF receiver, a direct conversion receiver translates the RF signal directly to baseband and therefore relaxes the ADC sampling rate and resolution requirement. Moreover, it has advantages in low cost and elimination of image requirements. However, it suffers from impairments of DC offset, I/Q mismatch, even-order nonlinearity, flicker (1/f) noise, and complication of LO frequency planning to evade LO pulling/leakage [5].

The DC offset and flicker noise are most prominent in a direct conversion receiver. Since the bandwidth of the ZigBee signal is wide, the DC offset can be cancelled easily without information loss using a capacitive coupling or DC offset cancellation technique [5]. The flicker noise in direct conversion can corrupt the signal since the downconverted spectrum extends to zero frequency, and its corner frequency can be as high as 1 MHz for CMOS technology. However, several technologies can solve the flicker noise problems [7].

Considering the advantages and disadvantages of low-IF and direct conversion architectures described above, the latter architecture is chosen since it enables a low-cost low-power implementation for the ZigBee transceiver.

Radio Specifications

Figure 1 shows a simplified schematic of a complete 868/915 MHz direct conversion ZigBee transceiver. The main characteristic of the 868/915 MHz ZigBee transceiver is using differentially encoded BPSK, also known as DPSK. The DPSK transceiver architecture makes it possible to implement a lower-cost noncoherent receiver rather than a coherent BPSK receiver that requires a carrier synchronization loop [6].

For the transmit (TX) path in Fig. 1, the input data stream is differentially encoded. The encoded output bit is then mapped into a 15-chip sequence, shaped by a raised cosine filter to reduce the intersymbol interference (ISI), modulated onto the carrier frequency, and then transmitted through an antenna. For the receive (RX) path in Fig. 1, the received signal at the antenna is demodulated, despread, and then differentially decoded [6].

Transmitter Specifications

In the design of digital communications, Nyquist filtering [6] is typically used to limit the required bandwidth of the transmitted signal. A common Nyquist filtering method is to use a raised cosine pulse shaping with a rolloff factor between zero and one. Since the ZigBee standard allows larg-

er channel spacing, the bandwidth limitation can be relaxed with increasing rolloff factor. The standard specifies a rolloff factor of one for the raised cosine filter, and this condition relaxes the filtering requirements in the transmit path. With decreasing the rolloff factor of the raised cosine pulse-shaping filter, the peak-to-average power ratio (PAPR), which is defined as the ratio of the peak envelope power to the average power of the transmit signal, increases. This PAPR gives a theoretical maximum output backoff requirement in the transmitter. From a PAPR simulation with rolloff factor of one, the required PAPR is about 2 dB.

Assuming a nominal transmit output power of 0 dBm, 2 dB PAPR means that the transmitter should be capable of transmitting up to 2 dBm. Therefore, the output 1 dB gain compression point (OP_{1dB}) of the transmitter output stage should be over 2 dBm.

For the relaxed filter requirements, only the filter order and cutoff frequency need to be characterized. From the power spectral density (PSD) characteristic of BPSK [6], the first null occurs at the frequency of chip rate, 600 kchips/s. Therefore, the cutoff frequency of the filter needs to be over 600 kHz. Moreover, for digital baseband signal processing, an oversampling ratio of four to eight times the baseband chip rate can be employed to improve the SNR significantly. However, when using a clock frequency of 4.8 MHz or eight times the chip rate, the sampled signal power appears in the frequency domain at integer multiples of clock frequency that must be attenuated by the filter. Considering around 30 dB suppression needed at 4.8 MHz, a second order Butterworth low pass filter (LPF) with 700 kHz corner frequency and about 33 dB signal suppression has been chosen.

DAC performance is measured with a spurious free dynamic range (SFDR), which is the most important parameter to determine the DAC quality. The overall SFDR can be calculated from the requirement of the PSD mask. The PSD mask requires –20 dBr relative to the peak level and absolute limit of –20 dBm at and above 1.2 MHz frequency offset. With some margin, the overall SFDR is chosen to be 30 dB. Since about 6 dB/bit is required for the converter, the required bit resolution is about 5 bits.

The phase noise requirement of the LO can be inferred from the local regulatory requirements [4]. For the European 868 MHz band, the transmit center frequency is 868.3 MHz. The European requirements specify a wideband spurious emission limit of –80 dBm/Hz. Therefore, the allowed phase noise with respect to carrier for 0 dBm transmit power is approximately –68 dBc/Hz at 300 kHz offset including the processing gain of 12 dB. For the U.S. 915 MHz band, the restricted band edge is 960 MHz. The U.S. requirements specify an out-of-band spurious emission limit of –91 dBm/Hz. Thus, the allowed phase noise for 0 dBm transmit power is –79 dBc/Hz at 32 MHz offset. If the transmit power is increased to 10 dBm, the required phase noise decreases to –78 dBc/Hz at 300 kHz offset for 868 MHz band, and –89 dBc/Hz at 32 MHz offset for 915 MHz band. Therefore, the European rules set a more stringent requirement for phase noise. The transmitter target specifications and phase noise requirement are summarized in Table 2.

	Blocks	Specification
Transmitter	DAC	Bit resolution: 6 bits
		Sampling: 6 MHz (> 8 × chip rate)
	LPF	Second order Butterworth, f_c = 700 kHz
	OP_{1dB}	2 dBm
	Output power	0 dBm
Receiver	Noise figure	< 19 dB
	ADC	Bit resolution: 4 bits
		Sampling: 6 MHz (> 8 × chip rate)
	IIP_3	> –40 dBm at minimum input power
		> –10 dBm at maximum input power
	IIP_2	> 7.2 dBm
	LPF	Third order Butterworth, f_c = 650 kHz
	SFDR	43 dB
	Input power	–92 to –20 dBm (gain control = 72 dB)
LO	Phase noise	–78 dBc/Hz at 300 kHz offset frequency

Table 2. *Summarized direct conversion transceiver target specifications.*

Receiver Specifications

The simulated BER curve of a DPSK receiver is plotted in Fig. 2, and compared to other variations of ideal DSSS DPSK and BPSK modulation schemes. As shown in Fig. 2, a DPSK receiver requires a minimum SNR (SNR_{min}) of about 9.5 dB for PER = 1 percent as required by the standard. Employing the DSSS technique, the receiver has a processing gain of 11.8 dB. From Fig. 2, the simulated SNR_{min} of a DSSS DPSK receiver is –2.8 dB, 0.5 dB lower than the theoretical value of –2.3 dB.

Since the noise floor in an ideal receiver is –113 dBm (–174 dBm/Hz+10log(BW)) for 1.2 MHz bandwidth, the minimum signal needs to be above –115.8 dBm considering the SNR_{min} of -2.8 dB for a DSSS DPSK receiver. Based on the minimum sensitivity of –92 dBm, the total implementation loss margin is about 24 dB. Assuming a 5 dB implementation margin, which accounts for board losses, external component losses, and digital losses in the receiver, the maximum allowed system NF of the receiver is found to be 19 dB.

The channel selection filter requirements can be derived from the jamming resistance and sampling clock frequency. For the receiver jamming resistance, the standard requires 0 dB rejection at the adjacent channel (2 MHz apart

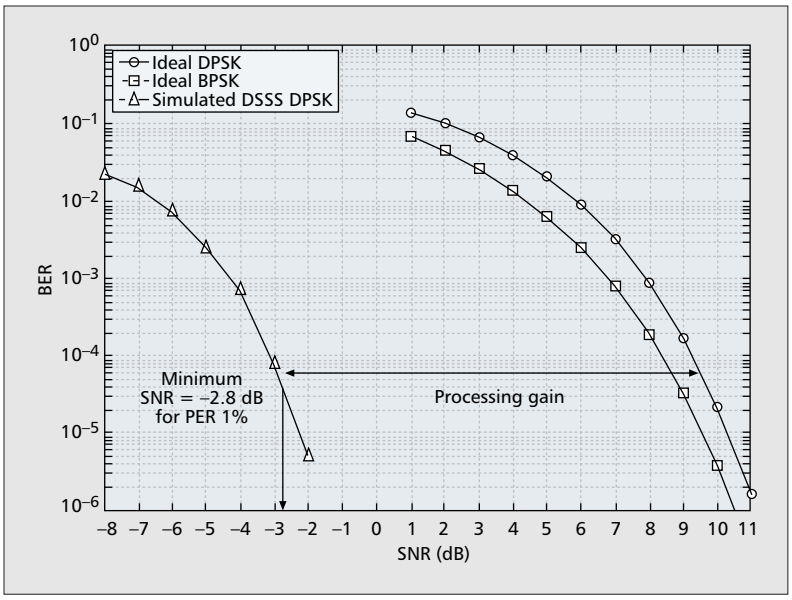

Figure 2. *Simulated BER performance of DSSS DPSK compared to ideal DPSK and BPSK modulation.*

from the desired signal) and 30 dB rejection at the alternate channel (4 MHz apart from the desired signal). Considering some margins, 40 dB rejection at the alternate channel is enough with a corner frequency of 650 kHz. To meet this specification, a third order Butterworth filter with corner frequency of 650 kHz can be chosen to provide about 47 dB rejection at the alternate channel. With ample channel spacing, this filter requirement has become very relaxed compared to that of other wireless LAN standards.

The required phase noise described in the TX specifications can also be calculated from an interferer profile and jamming resistance requirements. For the 868/915 MHz ZigBee applications, the interferers at the adjacent and alternate channels are –92 dBm and –62 dBm, respectively, according to the specifications of jamming resistance requirements. The phase noise is given by [5]

$$\text{Phase Noise}(dBc/Hz) = P_{sig} - P_{int} - SNR_{\min} - 10\log(BW) - \text{Margins}, \quad (1)$$

where P_{sig} is the power of the signal, P_{int} is the power of the interferers, and BW is the bandwidth of the ZigBee signal. With a minimum sensitivity signal power of –92 dBm, $SNR_{\min}$ of –2.8 dB, BW of 1.2 MHz, and 10 dB margins are assumed, the calculated phase noise is –68 dBc/Hz at the adjacent channel and –98 dBc/Hz at the alternate channel. The worst case phase noise then is set by the transmitter with a requirement of –78 dBc/Hz at 300 kHz offset for 10 dBm transmit power. Assuming –6 dB slope per octave scale, the required phase noise is then –78 dBc/Hz at 300 kHz, –84 dBc/Hz at 600 kHz, and –88 dBc/Hz at 1 MHz offset.

The ZigBee standard does not specify the receiver nonlinearity requirements such as input third-order intercept point, IIP_3, or second-order intercept point, IIP_2. However, the nonlinearity requirements can be inferred from the interferer profile and jamming resistance requirements. To derive the nonlinearity requirements, intermodulation and blocking power levels, shown in Table 1, need to be considered.

The IIP_2 and IIP_3 can be given by

$$IIP_2 = 2P_{\text{int}} - P_{sig} + SNR_{\min} + \text{Margins}$$
$$IIP_3 = \frac{(3P_{\text{int}} - P_{sig} + SNR_{\min} + \text{Margins})}{2}, \quad (2)$$

where P_{int} is the power of two interferers (±4 MHz apart and ±8 MHz apart from the signal, respectively), and P_{sig} is the power of the desired signal. With an interfering power at the blocker level of –30 dBm and $SNR_{\min}$ of –2.8 dB, the desired signal power is at least –60 dBm to satisfy the jamming resistance requirements. With a 10 dB margin, the resulting IIP_2 is 7.2 dBm. Similarly, the calculated IIP_3 is –40 dBm with a weaker signal at –89 dBm and an interfering power of –59 dBm, and –11.4 dBm with a blocker level of –30 dBm and a signal power of –60 dBm. Alternatively, consider a single tone maximum signal at –20 dBm specified in the ZigBee standard; the input 1 dB gain compression point should be over –20 dBm. Given that the compression point is 10 dB lower than the IIP_3 [5], the required IIP_3 needs to be over –10 dBm. Therefore, the required IIP_3 is –40 dBm with minimum sensitivity input power, and –10 dBm with maximum input power.

The receiver SFDR is calculated from [5]

$$SFDR = \frac{2}{3}(IIP_3 - P_n - NF) - SNR_{\min}. \quad (3)$$

From Eq. 3, the calculated SFDR is about 43 dB with IIP_3 of –34 dBm, noise floor (P_n) of –113 dBm, NF of 19 dB, and $SNR_{\min}$ of –2.8 dB.

The bit resolution of ADCs can be derived as follows. For 1.2 MHz bandwidth and 19 dB NF, the receiver thermal noise power is –94 dBm. With the required minimum sensitivity power level of –92 dBm as specified in the ZigBee standard, the SNR due to the thermal noise component (SNR_{therm}) is 2 dB. Since the SNR of the ADCs should be 20 dB above SNR_{therm} for which the receiver SNR loss generated by the ADC is negligible [8], the required SNR_{adc} for the ZigBee signal is 10 dB accounting for the processing gain of 12 dB. Given that approximately 6 dB is obtained per bit of resolution for an ADC, the bit resolution required for ZigBee signal is then 1.7 bits. Moreover, since the Butterworth channel selection filter attenuates an alternate channel interferer by about 47 dB, an interfering signal at –30 dBm will drop to –77 dBm, which is 15 dB above the required sensitivity level of –92 dBm. Therefore, approximately 2 bits are required to prevent the interferer from saturating the ADC. Thus, a total of 4 bits are needed for the ADC to accommodate the ZigBee signal and interferer. The sampling clock frequency of 4.8 MHz can be set for the ADC as is done for the DAC. The receiver target specifications are summarized in Table 2.

System Simulation Results

System simulation was performed for the 868/915 MHz direct conversion ZigBee transceiver to verify the transceiver target specifications in Table 2. An Agilent ADS Ptolemy signal processing simu-

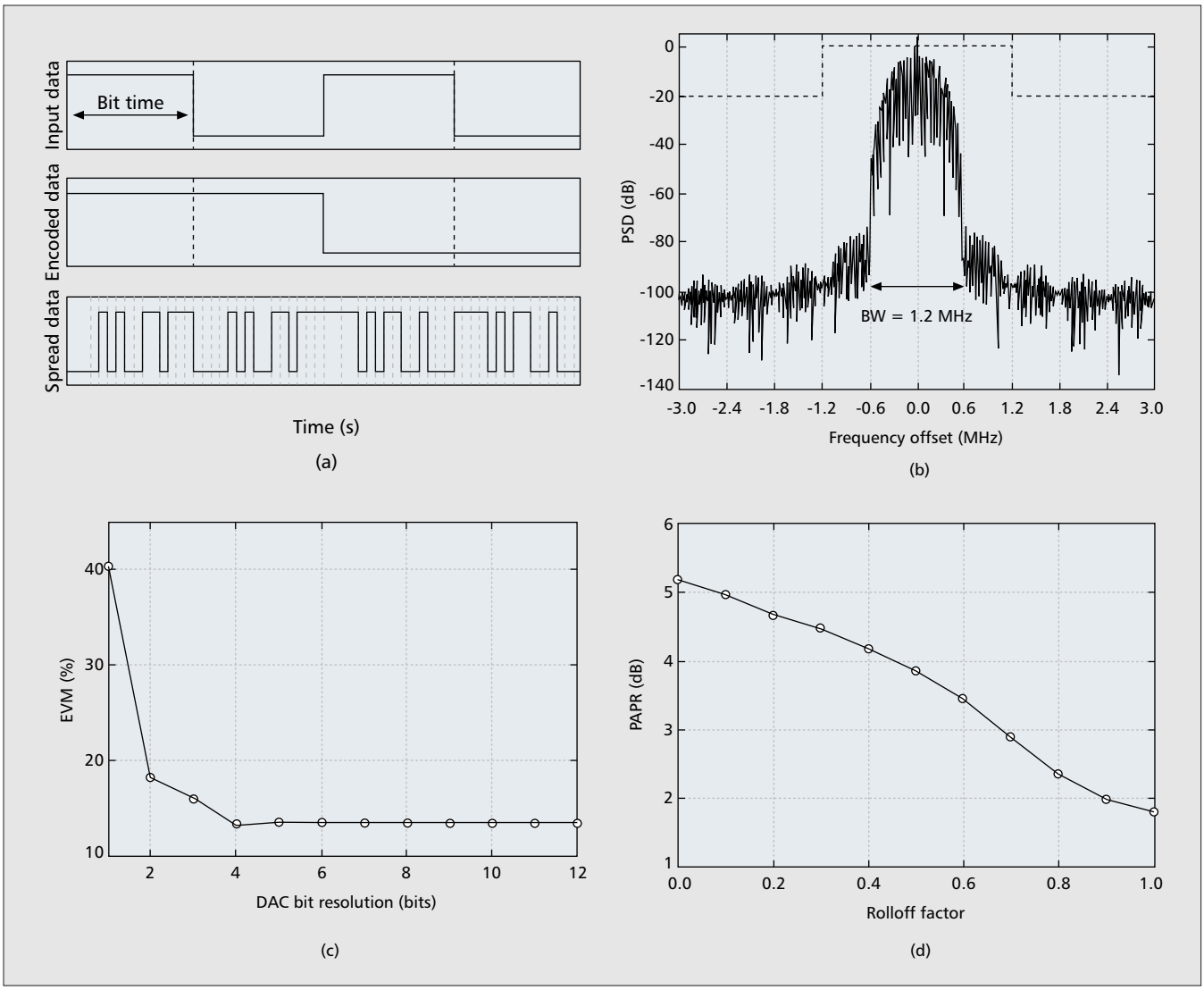

Figure 3. *868/915 MHz ZigBee transmitter system simulation results: a) time domain stream of input, encoded, and spread data; b) spectrum of the baseband signal; c) EVM with different DAC bit resolutions; d) PAPR with different rolloff factors.*

lator is used. For simplicity, the signal is assumed to propagate through an additive white Gaussian noise (AWGN) channel with no fading, frequency selectivity, interference, and nonlinearity [5]. Because the receiver budget cannot be uniquely defined, it is assumed that the overall system noise figure, nonlinearity, and gain are largely determined by the LNA block, while the other blocks are idealized to simplify the simulations.

Figure 3 shows the 868/915 MHz ZigBee transmitter system simulation results. Figure 3a shows the simulated time domain stream of input, encoded, and spread data. 40 kb/s binary input data is differentially encoded, and then spread by the 15-chip PN sequence. Figure 3b shows the spread spectrum of the baseband signal. The power spectral density of output signal spectrum is shown along with a spectrum mask.

Figure 3c shows the simulated EVM performance by varying the DAC bit resolution. The simulation result shows that increasing the DAC resolution beyond 4 bits does not further improve EVM performance. The PAPR is characterized by varying the rolloff factor of the raised cosine pulse shaping filter as shown in Fig. 3d. The PAPR simulation result shows that the driver amplifier should be backed off by at least 2 dB from the OP_{1dB} for a rolloff factor of one. This requires OP_{1dB} of the driver amplifier of 2 dBm when the transmitter delivers 0 dBm output power.

Figure 4 shows the 868/915 MHz ZigBee receiver system simulation results. Figure 4a shows the input power spectrum at the receiver input along with AWGN for a signal level of –92 dBm and noise floor of –113 dBm. Figure 4b shows the received decoded data stream compared to the transmitted raw data. In the decoded data the first several symbols can have some errors because the receiver does not know the initial state of the differential encoder of the transmitter. Figure 4c shows the BER performance with different ADC bit resolutions. The simulation result shows that at least 4 bits should be used for the ADC to not degrade the receiver BER performance significantly. Note that the simulated BER is above the requirement of 0.00625 percent BER since the simulation is performed with an NF of 19 dB and signal power of

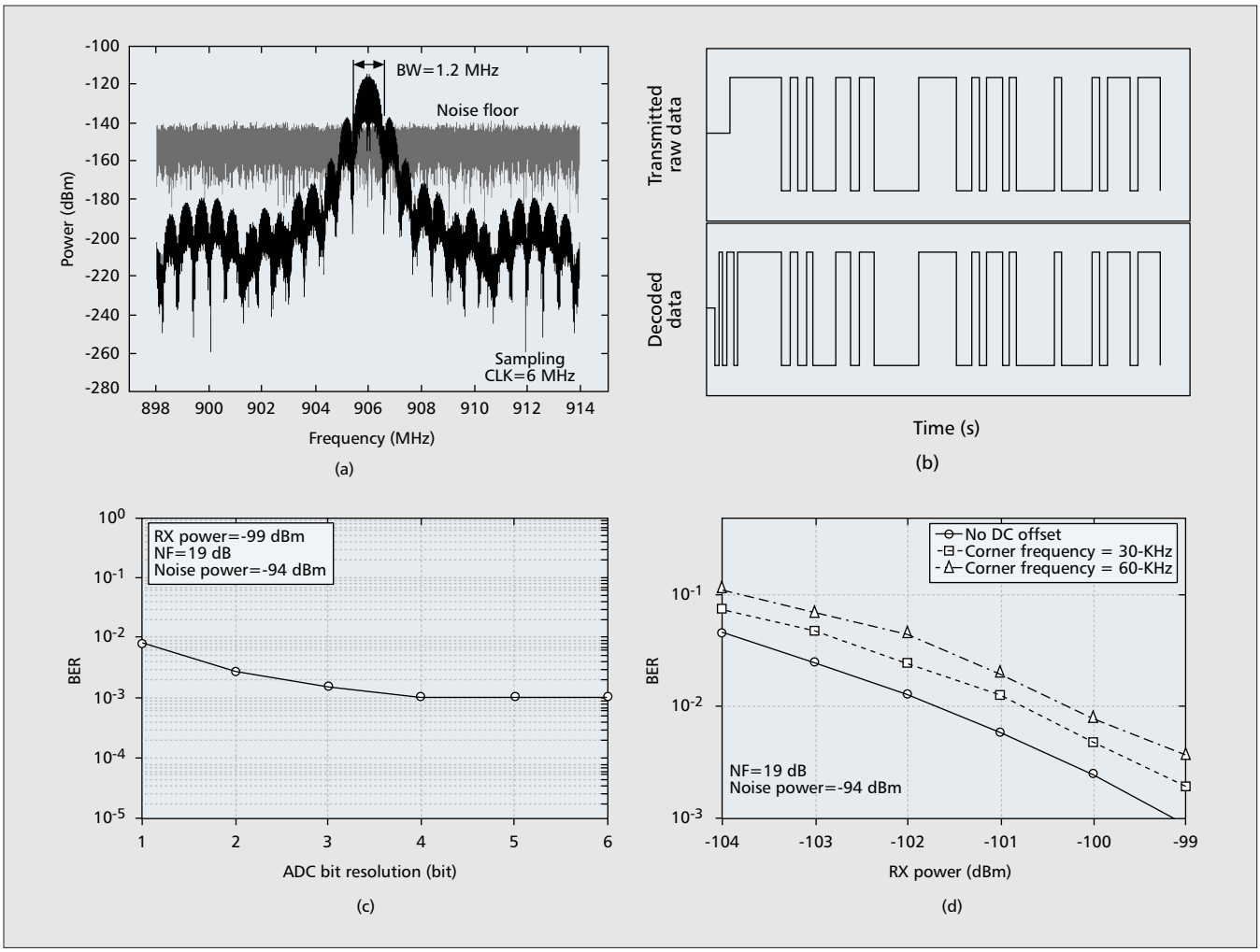

Figure 4. *868/915 MHz ZigBee receiver system simulation results: a) the received input power spectrum (–92 dBm at 1.2 MHz bandwidth) at the receiver input with AWGN (–113 dBm at 1.2 MHz bandwidth); b) time domain stream of original transmitted raw data compared to the decoded data stream; c) BER performance with different ADC bit resolutions; and d) BER performance with different high pass filtering corner frequencies of 30 kHz and 60 kHz.*

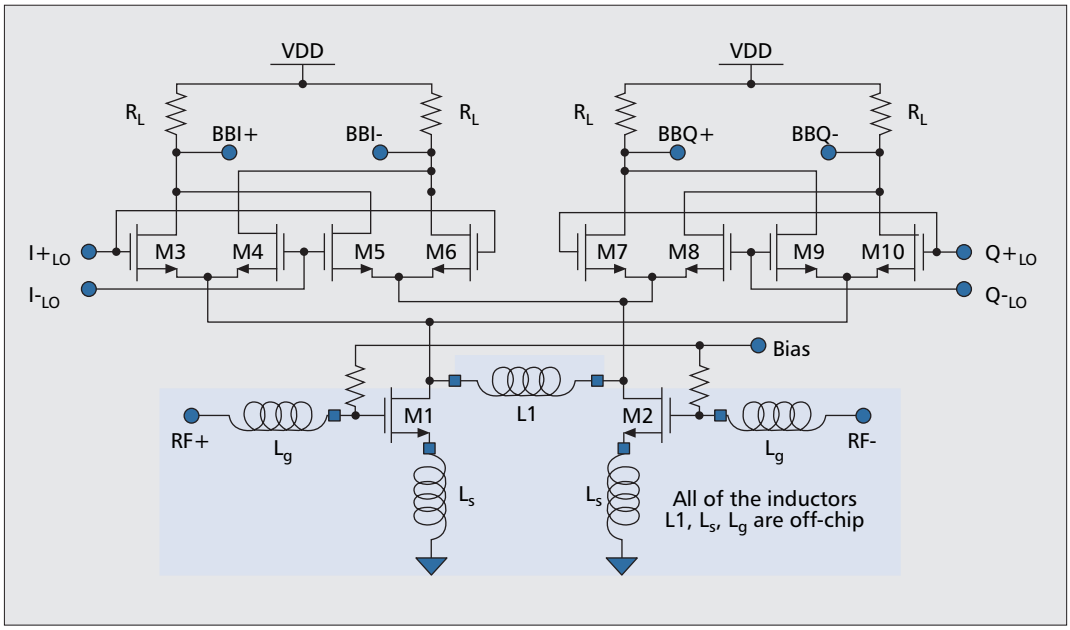

Figure 5. *Receiver front-end.*

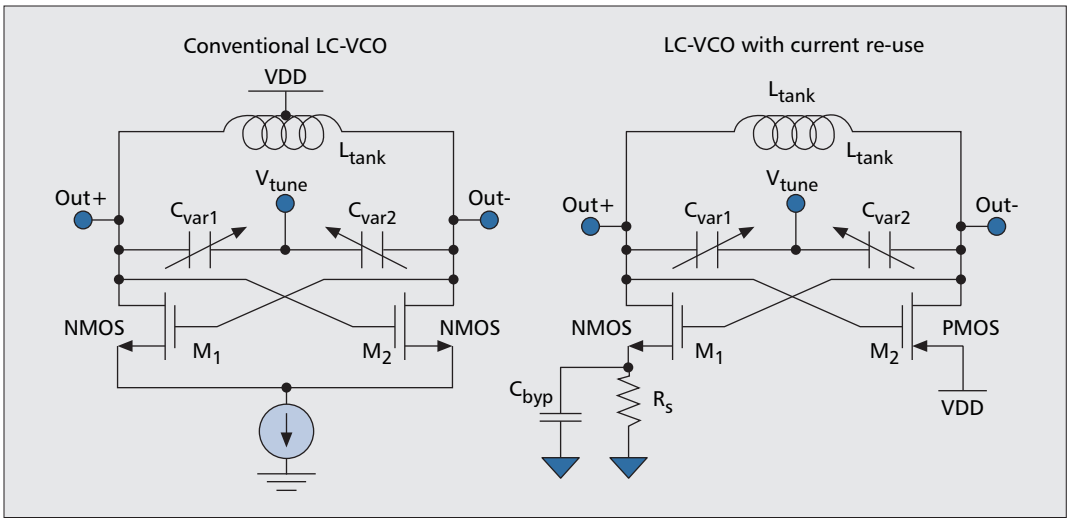

Figure 6. *Conventional and curent reuse CMOS differential LC-VCOs.*

In consideration of chip implementation, the transceiver should satisfy both low power consumption and low cost. To achieve this, stringent trade-offs are required for system noise, nonlinearity, gain, power consumption, and chip area.

–99 dBm, which is 5 dB less than the receiver noise power.

For a direct conversion receiver, a strong interferer or LO leakage can self-mix to produce a DC component at mixer output, corrupt the wanted signal, and hence saturate the analog baseband amplifiers. To overcome this problem, a DC offset cancellation loop circuit can be included in the analog baseband blocks, which has a characteristic of a high pass filter (HPF). The ZigBee standard requires turnaround time less than 12 symbols [4] or 300 μs with a symbol rate of 40 ksymbols/s. A fast settling time for the DC offset cancellation loop is preferable. Given that the 1 percent settling time is defined as $4.6/(2\pi f_L)$, where f_L is the corner frequency of the HPF, and it is set to 30 μs, f_L needs to be less than 40 kHz, which results in about 6.7 percent information loss.

Figure 4d shows the BER performances with different HPF corner frequencies of 30 and 60 kHz compared to those of the ideal case with no DC offset. As expected, the lower corner frequency of HPF reduces the information loss. However, too low a corner frequency of HPF will not suppress the DC offset and thus will result in saturation of the receiver due to unsuppressed DC offset. Simulation results show that the corner frequency of HPF can be chosen within 5 percent of the corner frequency of LPF, f_H, and the receiver needs just about 1 dB stronger signal power to produce the same error performances.

Chip Implementation

In consideration of chip implementation, the transceiver should satisfy both low power consumption and low cost. To achieve this, stringent trade-offs are required for system noise, nonlinearity, gain, power consumption, and chip area. For low power consumption, several circuit implementation methods are already developed [9, 10]. In [9] micropower CMOS front-end blocks including LNA and down-conversion active mixer have been implemented using high-quality (Q) factor off-chip inductors fabricated in low-cost low-temperature co-fired ceramic (LTCC) technology. LTCC technology does not increase module size by much, and further reduces power consumption significantly by implementing much higher Q inductors. Also, a micropower CMOS voltage controlled oscillator (VCO) that has a single side-band phase noise of less than –100 dBc/Hz at 100 kHz offset frequency is reported using the same technology.

The other method for a low-power circuit is based on the current reuse technique in which several blocks are stacked like a cascode configuration [10]. The current reuse technique is applied in the receiver RF front-end blocks by merging the LNA with a double balanced mixer, as shown in Fig. 5, whereby transistors M1 and M2 reuse DC current with M3–M10. With the relaxed system noise figure of the IEEE 802.15.4 standard, this technique eliminates the separate LNA block, which consumes considerable amount of power consumption and results in reduced chip size even though the system NF can be somewhat degraded. Among the inductors in Fig. 5, a source degeneration inductor, Ls, can be implemented with bond wires since its value is comparatively small. The inductors, Lg, are assumed to be implemented off-chip using LTCC technology. Inductor L1 resonates out the parasitics at the drain nodes of the transconductance transistors, M1 and M2. By nullifying the parasitics, the 1/f noise problem of MOS transistors can be significantly improved.

For low cost requirements, it is necessary to minimize the use of on-chip spiral inductors that occupy very large silicon areas. Instead, off-chip high-Q inductors should be used. With relaxed system requirements for the ZigBee transceiver, inductive loading for RF blocks is to be avoided as much as possible. For example, only one on-chip inductor is implemented for the VCO design shown in Fig. 6, where the conventional cross-coupled negative g_m VCO is modified to reuse the DC current by stacking the NMOS and PMOS transistors. Furthermore, the on-chip inductor can be replaced by a low-cost off-chip high-quality factor inductor exploiting the LTCC technology, as can be seen in [9].

Since the transmit power is very low compared to other standards, as shown in Table 1, the transmit RF front-end can be implemented in a simpler

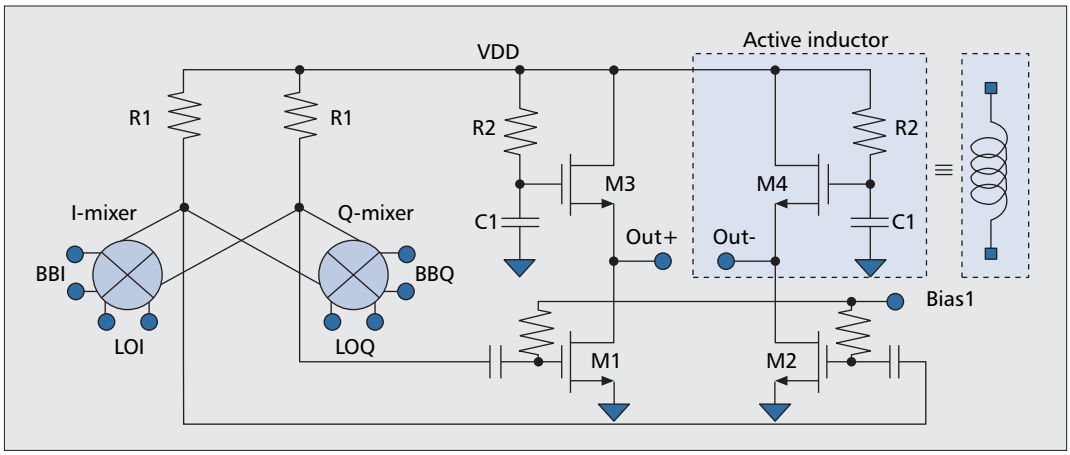

Figure 7. *Transmitter RF front-end.*

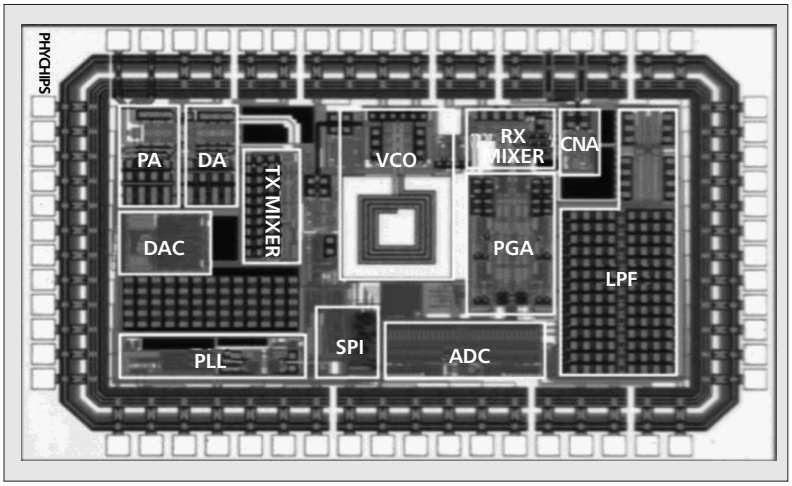

Figure 8. *Implemented chip micrograph.*

way and with low power consumption. As shown in Fig. 7, resistive loading for the upconversion mixer, and active inductor loading for the driver amplifier (which consists of a transistor, a resistor, and a capacitor) are adopted to reduce the silicon area instead of using passive on-chip spiral inductors.

In this transceiver implementation, several techniques discussed above are applied. For the receiver RF front-end, the LNA and active mixer is merged to reuse the DC current as shown in Fig. 5. To reduce the 1/f noise of the mixer, vertical NPN transistors rather than NMOS are used instead for the switching transistors of the mixer [7]. For the transmitter RF front-end, the topology shown in Fig. 7 is adopted. For the frequency synthesizer, a typical integer-N PLL is employed. The VCO core employs a conventional cross-coupled negative g_m cell to generate 1.8 GHz frequency oscillation and is divided by a frequency divider to generate I/Q signals, which are applied to the mixers. For the Butterworth LPF, an active RC filter is implemented to have a high linearity and low power consumption.

Based on the system specifications derived from the ZigBee standard, a direct conversion transceiver chip is implemented in 0.18 μm CMOS technology, as shown in Fig. 8. By using only one on-chip inductor, the die area can be significantly reduced to 3.84 mm^2 (core size is 1.8 mm^2), and thus achieves a great cost advantage. The fabricated chip is packaged in a 48-pin Quad Flat No-Lead (QFN) package. The measured NF and IIP_3 of the receiver are 10 dB and –19 dBm, respectively. The programmable gain control range of the receiver is 3–92 dB. The channel filter with a corner frequency of 680 kHz attenuates the adjacent channel interferer by 26 dB and the alternate channel interferer by 48 dB. The measured phase noise of the phase locked loop is –79 dBc/Hz and –112 dBc/Hz at 100 kHz and 1 MHz offset, respectively. The transmitter can deliver output power of 1.4 dBm. The transceiver chip consumes 17.5 mA in the receive mode and 18.5 mA in the transmit mode from a supply voltage of 1.8 V, respectively.

Conclusion

This article presents an overview of an emerging low-rate personal area network standard, IEEE 802.15.4, and discusses transceiver architectures for this standard. Based on the PHY requirements, system-level radio specifications have been derived for the 868/915 MHz transceiver. Using the derived radio specifications, top-down system-level simulations and chip implementations have been realized based on a direct conversion scheme.

References

[1] IEEE Std 802.11a-1999, "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications — High-Speed Physical Layer in the 5 GHz Band," Sept. 1999.
[2] IEEE Std 802.11b-1999, "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications — High-Speed Physical Layer in the 2.4 GHz Band," Sept. 1999.
[3] IEEE Std 802.11g-2003, "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications — Further Higher-Speed Physical Layer in the 2.4 GHz Band," June 2003.
[4] IEEE Std 802.15.4-2003, "Low Rate Wireless Personal Area Networks," Oct. 2003.
[5] B. Razavi, *RF Microelectronics*, Prentice Hall, 1998.
[6] L. W. Couch, *Digital and Analog Communications Systems*, 5th ed., Prentice Hall, 1997.
[7] I. Nam and K. Lee, "High-performance RF Mixer and Operational Amplifier BiCMOS Circuits Using Parasitic Vertical Bipolar Transistor in CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, Feb. 2005, pp. 392–402.
[8] —, Ch. 13, "Wireless Communication: Signal Conditioning for IF Sampling," http://focus.ti.com/lit/ml/sloa085/sloa085.pdf

[9] R. Rofougaran *et al.*, "CMOS Front-End LNA-Mixer for Micropower RF Wireless," *Low Power Elect. and Design*, 1999, pp. 238–42.
[10] A. Zolfaghari and B. Razavi, "A Low-power 2.4-GHz Transmitter/Receiver CMOS IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, Feb. 2003, pp. 176–83.

BIOGRAPHIES

NAM-JIN OH (onamjin@icu.ac.kr) received his B.S. degree in physics from Hanyang University, Seoul, Korea, in 1992 and his M.S. degree in electrical engineering from North Carolina State University, Raleigh, in 1999. From 1992 to 1997 he was with LG Corporate Institute of Technology, Seoul, Korea. From 1999 to 2001 he was with Samsung Electronics, Suwon, Korea. From May to July 2004 he had an internship at PHYCHIPS Inc., Daejeon, Korea. Currently, he is working toward a Ph.D. degree at the Information and Communications University, Korea.

JINHO KO received his B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1994 and 1996, respectively, where he is currently working toward a Ph.D. degree. From 1996 to 1998 he was with the R&D Center, SK Telecom, Daejeon, where he was involved in designing a CMOS baseband analog processor for CDMA cellular phones. Between 1999 and 200 he was with Havin' Company, Ltd, Daejeon, where he worked on developing a low-power CMOS Bluetooth and GPS RFIC. In 2002 he founded PHYCHIPS Inc., Daejeon, which is focused on developing low-power RF system-on-chip (SoC) solutions. His research interests include low-power low-cost CMOS RF-SoC for WPANs and wireless sensor networks.

SANG-GUG LEE received his B.S. degree in electronic engineering from Gyungbook National University, Korea, in 1981, and his M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1989 and 1992, respectively. In 1992 he joined Harris Semiconductor, Melbourne, Florida, where he was engaged in silicon-based RFIC design. From 1995 to 1998 he was with Handong University, Pohang, Korea, as an assistant professor in the School of Computers and Electrical Engineering. Since 1998 he has been with Information and Communications University, Daejeon, Korea, where he is an associate professor. His research interests include silicon-technology-based (BJT, BiCMOS, CMOS, and SiGe BiCMOS) RFIC designs such as LNA, mixer, oscillator, and power amp. He is also active in designing high-speed IC for optical communications such as TIA, driver amp, limiting amp, CDR, and mux/demux.