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BUILDING A 2.4-GHZ RADIO TRANSCEIVER USING IEEE 802.15.4

The ZigBee Alliance has been developing a standard-based wireless network platform aimed at sensor and control applications with low-data rate and low-power consumption. IEEE 802.15.4 [1], ratified in 2003, specifies the physical (PHY) layer and medium access control (MAC) layers, while the ZigBee Alliance defines upper layers such as network, security and application profile layers for an IEEE 802.15.4-based system. IEEE 802.15.4 assigns three frequency bands of operation: the 868-MHz, 915-MHz, and 2.4-GHz unlicensed industrial, scientific, and medical (ISM) bands. Among the three, the 2.4-GHz band is highly attractive, since this unlicensed band is commonly available throughout the world. Typical applications of this low data rate standard include

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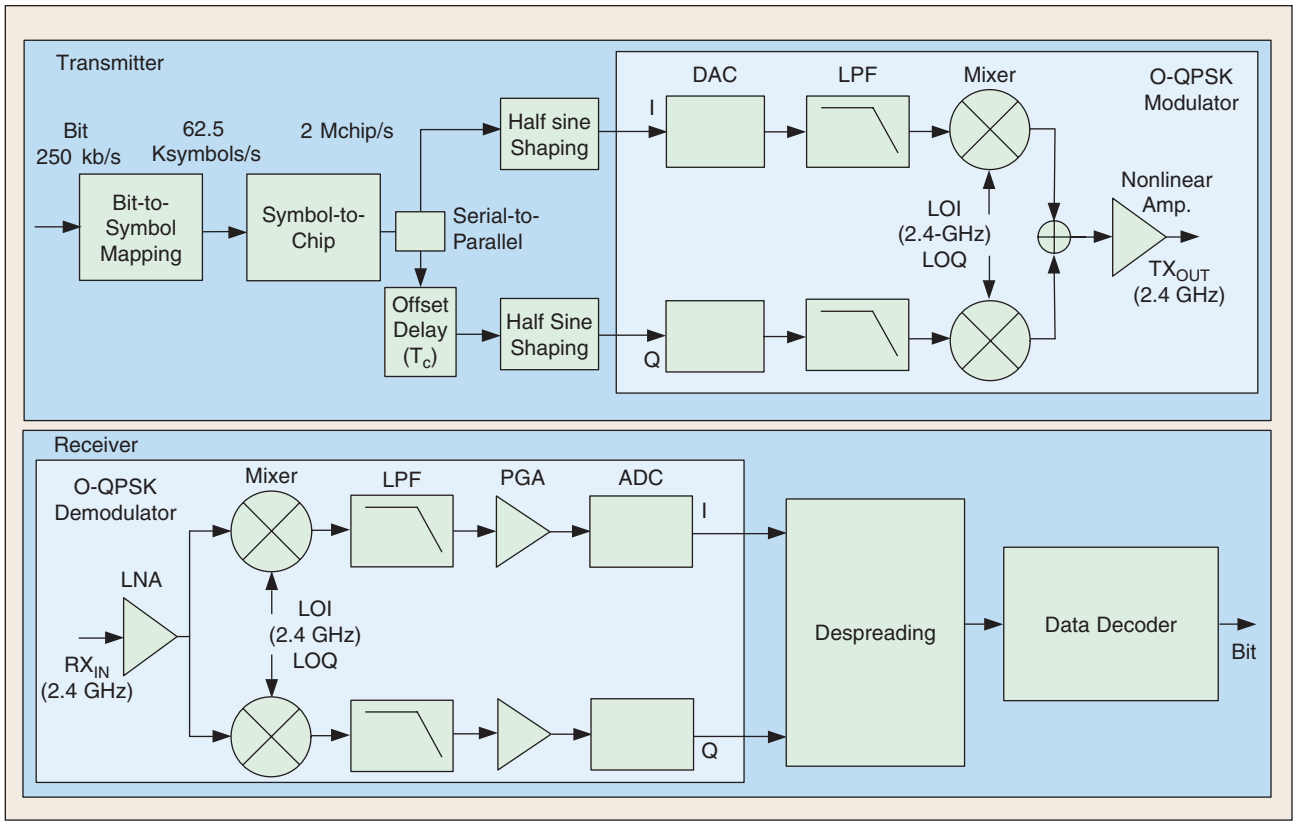


1. Direct conversion 2.4-GHz PHY.

those for industrial and commercial uses, home automation, PC peripherals, consumer electronics, and personal health care appliances, as well as for toys and games that should be able to run for six months to two years on just button cells or batteries [2].

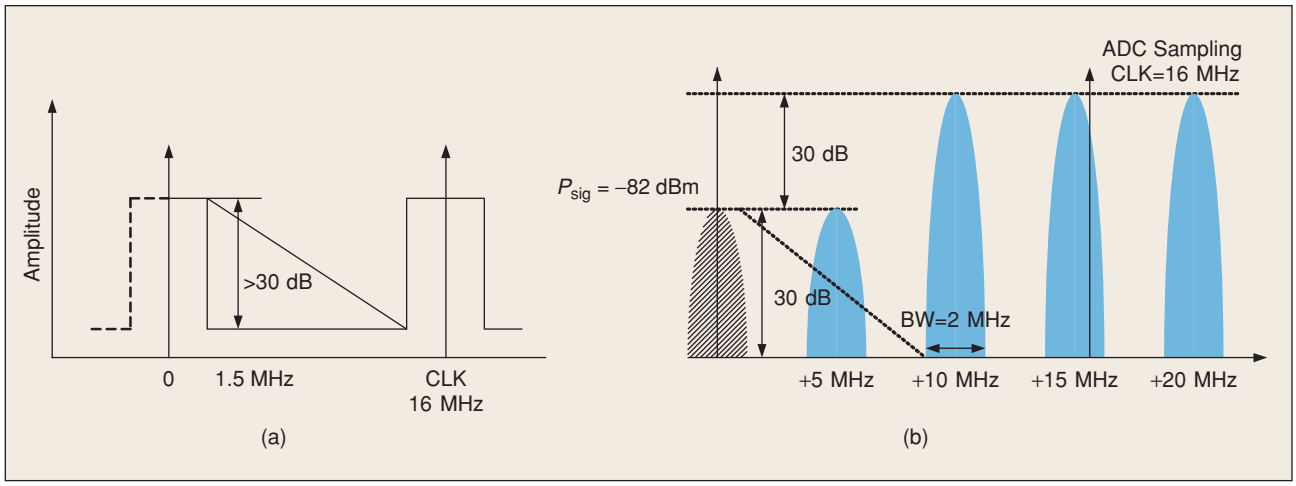
Focusing on the 2.4-GHz PHY, this article presents top-down system-level performance analyses using system-level radio specifications derived from IEEE 802.15.4. The system-level radio specifications include such things as system noise figure (NF), system nonlinearity, phase noise of the local oscillator (LO), channel-filter requirements, and bit resolutions of analog-to-digital or digital-to-analog converters. Radio transceiver architectures, such as heterodyne, low intermediate frequency (IF), and direct conversion are discussed, an optimal architecture is chosen, and system-level radio specifications are derived. Based on the derived system-level radio specifications, detailed top-down system-level simulations are performed for the 2.4-GHz radio transceiver, and a chip is implemented by exploiting low-power design techniques for the transceiver.

RADIO TRANSCEIVER ARCHITECTURES AND SPECIFICATIONS

An IEEE 802.15.4-based 2.4-GHz PHY can support 250 kb/s data rate. Sixteen channels are available for 2.4-GHz band applications, with ample channel spacing of 5 MHz. IEEE 802.15.4 employs a direct-sequence spread spectrum (DSSS) that uses a digital-spreading function representing pseudo-random noise (PN) chip sequences. For a 2.4-GHz PHY, a two-megachips-per-second chip rate is used for the spreading parameter, and the chip sequences are modulated onto a carrier using offset-quadrature phase-shift keying (O-QPSK) with half sine pulse shaping for the 2.4-GHz PHY, which is equivalent to minimum shift keying (MSK) [3]–[5].

In terms of architectures, a radio transceiver can be implemented as a heterodyne, low-intermediate frequency (low-IF) or direct-conversion scheme. As a conventional and well-established transceiver architecture, the heterodyne scheme has advantages of good overall performance, flexibility in frequency planning, no dc offset problems, and superior in-phase (I) and quadrature-phase (Q) matching. However, its disadvantages are that it requires discrete external components and suffers from image problems, difficulties in the multi-mode transceiver, higher power consumption, and high implementation costs. Considering the requirements of low power and low cost addressed in IEEE 802.15.4, heterodyne architecture is not preferred.

A low-IF scheme, which combines the advantages of both heterodyne and direct-conversion schemes, is able to avoid the dc offset problem and eliminate the expensive IF surface acoustic wave (SAW) filter, IF phase-locked loop (PLL) and image filtering. However, it suffers impairments such as even-order nonlinearity, LO pulling, and LO leakage [6]. Additionally, the low-IF scheme requires stringent image rejection as an adjacent channel becomes its image. Image rejection in low-IF can be achieved either in the analog or digital domain. The analog solution uses analog complex band pass filters (BPFs).



2. Requirements of (a) DAC reconstruction filters and (b) channel selection filters.

This method increases chip size and power consumption but requires a second low-frequency digital mixer. The digital solution for image rejection does not increase chip size, but requires good in-phase and quadrature-phase matching and more constraints on analog blocks. Furthermore, signal bandwidth (BW) in the low-IF scheme is twice that in direct conversion, thus requiring double the anlog-to-digital converter (ADC) sampling rate, resulting in higher power consumption. Two times the signal BW in low-IF requires doubling the baseband analog filter BW, thus increasing design complexity and power consumption.

A direct-conversion scheme that translates the RF signal directly to the baseband signal has the advantages of low cost, no image problem, and no image filters. However, it suffers the impairments of dc offset, I/Q mismatch, even-order nonlinearity, flicker or 1/f noise [especially severe in complementary metal-oxide semiconductor (CMOS) implementation], and complications of LO frequency planning in its attempts to evade LO pulling and leakage [6]. Among the problems in the direct conversion scheme, dc offset and flicker noise are the most prominent. Since the signal BW is wide (2 MHz for 2.4 GHz PHY), the dc offset can be cancelled easily without impairing the signal information using a capacitive-coupling method or dc offset-cancellation technique [6]. The flicker or 1/f noise (which arises from the random trapping charge at the oxide-silicon interface of MOSFETs and the noise density being inversely proportional to frequency) in direct conversion can corrupt the signal, since the down-converted spectrum extends to zero frequency, and the corner frequency of the 1/f noise can be as high as 1 MHz for CMOS technology. However, flicker-noise problems can be avoided by using passive mixers in exchange for some overall NF degradation or using parasitic vertical NPN transistors in CMOS technology for the switching core of active mixers [7].

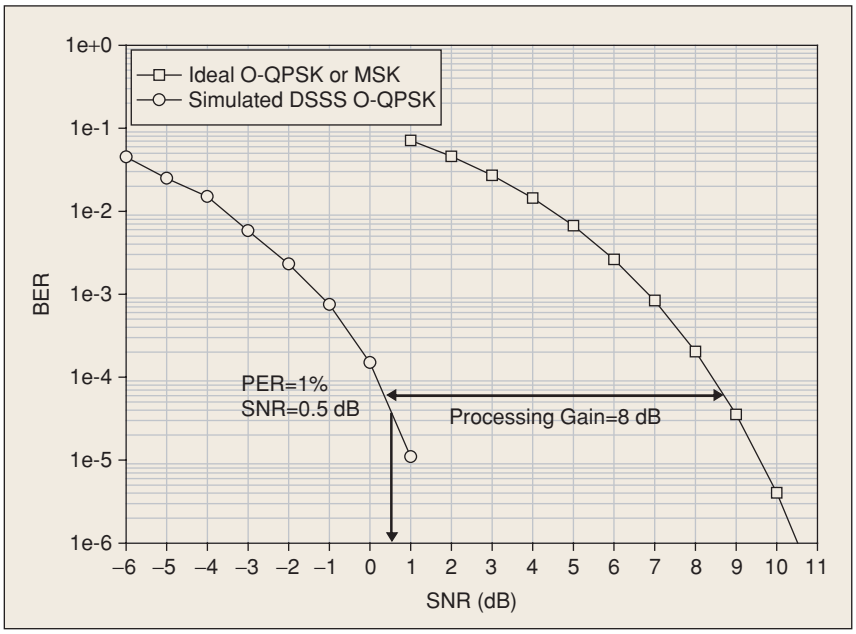
Considering the advantages and disadvantages of the low-IF and direct-conversion architectures described, the latter architecture is chosen for 2.4-GHz PHY since it enables the implementation of a low-power, low-cost, and highly integrated single chip.

Figure 1 shows a complete 2.4-GHz PHY based on a direct-conversion scheme. Each of the four information bits of the 250 kb/s input data is mapped into a symbol, making the symbol rate 62.5 kilosymbols per second. The symbol is then used to select one of 16 nearly orthogonal 32-chip PN sequences to be transmitted and results in a chip rate of two megachips per second. Since the time average of the modulated chip sequence is zero, there is no dc component in the modulated signal [8]. The received signal passes through the reverse processing of the transmit path. The signal from an antenna is split into I/Q paths, demodulated, de-spread, and then data decoded.

As shown in Figure 1, the RF/analog blocks of the modulator consist of digital-to-analog converters (DACs), reconstruction analog low-pass filters (LPFs), up-conversion mixers, and an output driving amplifier. The O-QPSK demodulator consists of a low-noise amplifier (LNA), down-conversion mixers, anti-aliasing LPFs, gain-control amplifiers, and ADCs. For the transmit path in Figure 1, the chip sequences are split into I/Q paths by a serial-to-parallel (S/P) converter, half-sine pulse shaped, and then modulated onto a carrier by direct up-conversion. Even-indexed chips are modulated onto the I carrier and odd-indexed chips are modulated onto the Q carrier. The Q-path chips are time delayed by T_c which is the inverse of the chip rate [1]. A less linear amplifier can be used at the output driving stage, which is aimed at low power consumption. For the receive path, the input analog signal is amplified by an LNA, down-converted by I and Q mixers, filtered by anti-aliasing channel-selection LPFs, gain-controlled by programmable gain amplifiers (PGAs), and then digitized by ADCs.

Transmitter Specifications

The DAC requirements can be derived from knowing the required spurious free dynamic range (SFDR). Since IEEE 802.15.4 specifies power spectral density at a relative limit of -20 dB at $|f - f_c| > 3.5$ MHz, where f_c is the center frequency of the signal [1], the minimum required dynamic range needs to be above 30 dB, assuming about 10-dB margins. Since about 6 dB/b resolution is required, the bit resolution of the DAC is about 5 b. For digital signal processing, an oversampling



3. The BER curve of DSSS O-QPSK modulation compared to O-QPSK or MSK modulations.

technique that samples the signal four to eight times the baseband data rate is typically employed to improve the signal to noise ratio (SNR) significantly. Therefore, an oversampling clock (CLK) frequency of 16 MHz is chosen with eight times the chip rate for the DAC.

Since the 2.4-GHz PHY allows ample channel spacing of 5 MHz, the DAC reconstruction anti-aliasing filter requirements can be relaxed. From a power-spectral density (PSD) characteristic of O-QPSK with half-sine pulse shaping [9], the first null occurs at the frequency of 0.75 times the two-megachips-per-second chip rate. Therefore, the modulated signal at the baseband can be filtered with a LPF having a −3 dB corner frequency of about 1.5 MHz [8]. Employing the oversampling technique for the DAC, the sampled signal power appears in the frequency domain at the integer multiples of clock frequency that are to be attenuated by the LPF. The required attenuation is over 30 dB at the sampling CLK frequency. A low-order LPF (for example, the second-order Butterworth-type LPF, which has about 38-dB signal suppression at the oversampling CLK frequency) is chosen to meet the attenuation requirements, as shown in Figure 2(a).

Since the 2.4-GHz PHY employs a constant envelope modulation scheme of O-QPSK with half-sine pulse shaping, the benefit of this constant envelope modulation is the flexibility to use simple, low-cost, less linear power amplifiers at the output driving stage [4]–[5], making the output driving stage operate at or near saturation power levels and resulting in lower power consumption with higher power efficiencies. Considering the nominal transmit power of 0 dBm, the saturation output power level of the driver amplifier which is specified with output 1 dB compression point (OP_{1dB} is defined as the output power level that causes the small signal gain to drop by 1 dB when the input signal power increases) needs to be above 0 dBm. The output third order intercept point (OIP_3), which specifies the third-order nonlinearity characteristics of the amplifier, is 10 dBm considering OIP_3 is about 10 dB higher than OP_{1dB} [6].

Receiver Specifications

The overall performances of an IEEE 802.15.4-based 2.4-GHz PHY can be characterized with packet-error rate (PER) that defines the average fraction of transmitted packets that are not detected correctly. The required PER should be less than 1% measured over random PHY service data unit (PSDU) data [1]. The PER can be roughly estimated by multiplying the bit-error rate (BER) by the number of bits per packet, which is about 20 B or 160 b. Thus, 1% PER can be extrapolated to 0.00625% BER only if acquisition effects are ignored.

The BER of O-QPSK modulation with half-sine pulse shaping is given by [4]

$$P_e = Q\left(\sqrt{2\text{SNR}}\right). \quad (1)$$

The simulated BER curve of DSSS O-QPSK is plotted in Figure 3 [1] and compared to other variations of ideal O-QPSK or MSK modulation schemes. As shown in Figure 3, the ideal O-QPSK or MSK receiver requires a SNR_{min} of about 8.5 dB for 1% PER. Employing the DSSS technique, the radio transceiver has a processing gain that can be derived from the ratio of chip rate to bit rate. With a chip rate of two-megachips-per-second and a data rate of 250 kb/s, the calculated processing gain is about 9 dB. Including the processing gain, the required minimum SNR_{min} for the ideal DSSS O-QPSK receiver is about −0.5 dB. However, the simulation result in Figure 3 shows about 8-dB processing gain obtained for the receiver, thus the minimum required SNR_{min} of 2.4-GHz PHY is about 0.5 dB.

Since the noise power for an ideal noiseless receiver system is about −111 dBm [−174 dBm/Hz+10log(BW)] with 2-MHz BW, which is defined in the transmit PSD mask specification of IEEE 802.15.4, the minimum signal level needs to be above −110.5 dBm, considering the simulated minimum SNR_{min} of 0.5 dB. Based on the minimum sensitivity of −85 dBm specified in IEEE 802.15.4, the total implementation loss margins are about 25.5 dB. Assuming about 5 dB implementation margins, which account for such things as board, external-component, and digital losses in the receiver, the maximum allowed system NF of the RF/analog front-end of the 2.4-GHz PHY is found to be about 20.5 dB.

The channel selection anti-aliasing LPF specifications can be derived from the requirements of jamming resistance and ADC sampling CLK frequency, as shown in Figure 2(b). The IEEE 802.15.4 PHY requires 0-dB rejection at the adjacent channel (±5 MHz) and 30-dB rejection at the alternate channel (±10 MHz), respectively. Assuming 10-dB margins, 40-dB

rejection at the alternate channel is enough; therefore, the third-order Butterworth-type filter with corner frequency of 1.5 MHz, which has about 50-dB rejection at 10 MHz apart from the wanted signal, can be chosen for the channel selection anti-aliasing filter.

The bit resolution of ADCs can be derived as follows. For 2-MHz BW and 20.5 dB NF, the receiver noise power can be calculated from -174 dBm/Hz + 10log(BW) + NF, thus -90.5 dBm. With -85 dBm minimum sensitivity power level, the SNR due to the thermal noise component (SNR_{therm}) is 5.5 dB. Since the SNR of the ADCs should be 20 dB above the SNR_{therm} for which the receiver SNR loss generated by the ADC is small enough to ignore [10]–[11], the required SNR_{ADC} for the 2.4-GHz signal is 16.5 dB, accounting for the processing gain of 9 dB. Given that about 6 dB is obtained per bit of resolution for the ADC, the effective number of bits (ENOB) required for the 2.4-GHz signal is 3 b.

Since the channel selection filter attenuates an interferer by 50 dB, and assuming the interferer power is -30 dBm, it drops to -80 dBm, which is 5 dB above the minimum sensitivity level. The required bit resolution to fit the interferer is 1 b. Thus, a total of 4-b resolution ADC is required to accommodate the signal and interferer in the 2.4-GHz band. More bits can be assigned for headroom if desired.

The phase-noise requirements of the LO can be inferred from local regulatory requirements such as the Federal Communications Commission (FCC) (Section 15 of FCC CFR47) and European Telecommunications Standards Institute (ETSI) rules (ETSI EN 300), which specify out-of-band spurious emissions power limits [1]. European 2.4-GHz band operation allows a wideband spurious limit of -80 dBm/Hz from 1–12.5 GHz. Since the nearest channel to the band edge in the 2.4–2.4835-GHz band is 2.48 GHz, this sets the worst-case phase noise at 3.5 MHz offset of -80 dBc/Hz. This is converted to phase noise relative to the carrier by taking into account the spreading gain and the maximum carrier power. The phase noise is relaxed by spreading gain (about 9 dB for the 2.4-GHz PHY), allowing a phase noise of -71 dBc/Hz at 3.5-MHz offset. If the maximum transmit power is increased to 10 dBm, the phase noise should be about -81 dBc/Hz at 3.5-MHz offset. This is a relaxed phase noise requirement. The U.S. requirements on phase noise for 2.4-GHz are more restrictive. The allowed emission level for U.S. 2.4-GHz operation is -41.2 dBm/MHz or an average of -101.2 dBm/Hz. The spreading gain of 9 dB raised the allowed phase noise for a 0-dBm transmit power to about -92 dBc/Hz at 3.5-MHz offset. At 10-dBm transmit power, the phase-noise requirement is, therefore, about -102 dBc/Hz at 3.5-MHz offset.

The required phase noise can also be calculated from the interferer profile, as shown in Figure 2(b), by using

$$\text{phase noise (dBc/Hz)} = P_{sig} - P_{int} - SNR_{min} - 10\log(BW) - \text{margins}, \quad (2)$$

where P_{sig} is the power of the signal, P_{int} is the power of the interferers, and the BW of the signal is 2 MHz. With minimum signal power of -85 dBm and SNR_{min} of 0.5 dB, the calculated phase noise is -73.5 dBc/Hz at 5-MHz offset and is -103.5 dBc/Hz at 10-MHz offset, respectively, assuming 10-dB margins. Figure 4 shows the required phase noise compared to that of the conventional cross-coupled voltage-controlled oscillator (VCO), which can be easily obtained with modern sub-micron CMOS technology [12].

Since the receiver nonlinearity requirements such as input third-order intercept point (IIP_3) or second-order intercept point (IIP_2) are not specified in IEEE 802.15.4, the nonlinearity requirements need to be inferred from the interferer profile, as shown in Figure 2(b).

IIP_3 can be given by

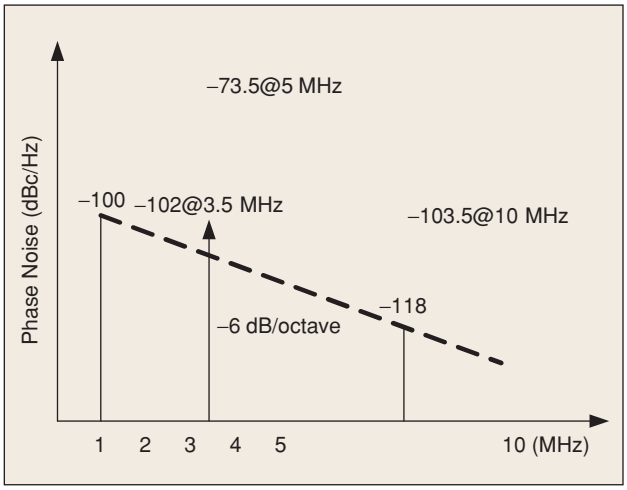
$$IIP_3 > \frac{(3P_{int} - P_{sig} + SNR_{min} + \text{margins})}{2}, \quad (3)$$

where P_{int} is the power of two interferers (± 10 MHz apart and ± 20 MHz apart from the signal, respectively), and P_{sig} is the power of the desired signal. With an interfering power of -52 dBm, a minimum signal power of -82 dBm (3 dB above minimum sensitivity level), and an SNR_{min} of 0.5 dB, the calculated IIP_3 is -32 dBm, assuming 10 dB margins. Considering the maximum input level of -20 dBm [1], which is the highest blocking interferer specified in IEEE 802.15.4, the input 1-dB gain compression point (IP_{1dB}) needs to be above -20 dBm, and the input IP_3 (IIP_3) needs to be over -10 dBm considering IIP_3 is about 10 dB higher than IP1dB [6].

In a similar way, the second order nonlinearity characteristic (IIP_2) which becomes problematic in the direct conversion receiver [6] can be given by

$$IIP_2 > 2P_{int} - P_{sig} + SNR_{min} + \text{margins}, \quad (4)$$

where P_{int} is the power of two interferers (± 10 and ± 20 MHz apart from the signal, respectively) and P_{sig} is the power of



4. Phase noise requirements of IEEE 802.15.4-based 2.4-GHz PHY. As a comparison, the phase-noise characteristics of a conventional CMOS VCO are plotted (dotted line). IEEE 802.15.4 specifies –102 dBc/Hz at 3.5 MHz offset.

the desired signal. With an interfering power of −30 dBm and SNR_{min} of 0.5 dB, the calculated IIP_2 is 10.5 dBm, assuming 10-dB margins.

The receiver SFDR [6] is calculated from

$$SFDR = \frac{2}{3}(IIP_3 - F) - SNR_{min}, \quad (5)$$

where F is the receiver NF plus the noise floor power P_n in decibel scale. From (5), the calculated SFDR is about 38.5 dB with an IIP_3 of −32 dBm, a P_n of −111 dBm, an NF of 20.5 dB, and an SNR_{min} of 0.5 dB.

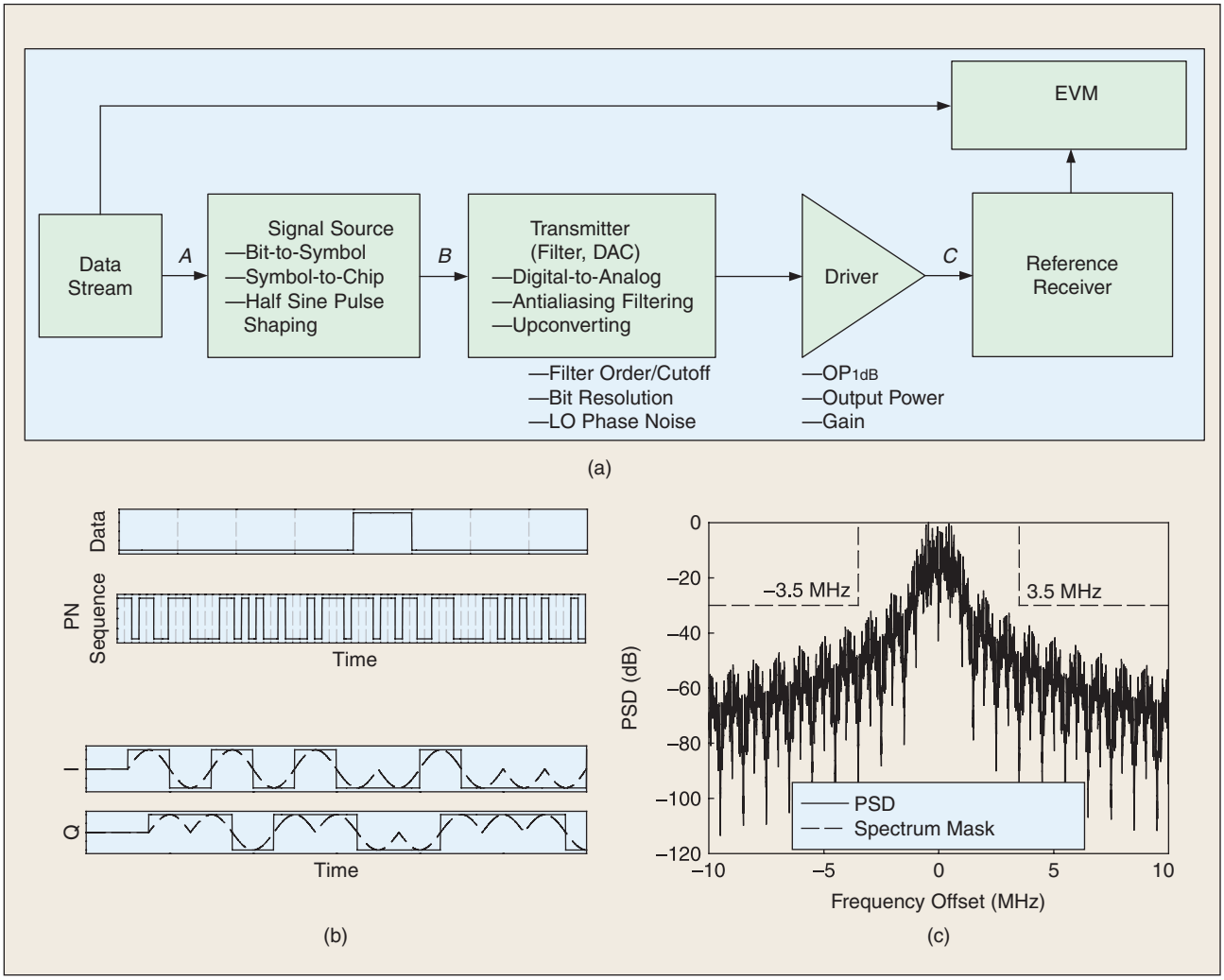
The 2.4-GHz PHY overall specifications are summarized in Table 1. A budget plan can be allocated to each RF/analog block in Figure 1 to meet the derived overall system specifications.

Table 1. Summarized Transceiver Target Specifications

	Blocks	Specification
Transmitter	DAC	Bit resolution : 5 b Sampling CLK: 16 MHz (> 8 × chip rate)
	LPF	The second order, f_c = 1.5 MHz
	$OP1_{dB}$	0 dBm
	Output Power	0 dBm
Receiver	ADC	Bit resolution : 4 b Sampling CLK: 16 MHz (> 8 × chip rate)
	Noise Figure	< 20.5 dB
	IIP3	> −32 dBm at maximum gain, > −10 dBm at minimum gain
	IIP2	> 10.5 dBm
	LPF	The third order, f_c = 1.5 MHz
	SFDR	> 38.5 dB
	Input Power	–85 to −20 dBm (Gain control = 65 dB)
LO	Phase Noise	−102 dBc/Hz at 3.5 MHz offset

SYSTEM SIMULATION RESULTS AND LOW POWER DESIGN TECHNIQUES

Figure 5(a) and Figure 6(a) show system simulation setups for a 2.4-GHz radio transceiver based on direct conversion architecture. For simplicity, the signal is assumed to propagate through an additive white Gaussian noise (AWGN) channel with no fading, frequency selectivity, interference, nonlinearity or dispersion [6]. Since the budget plan can not be uniquely defined for the receiver, it is assumed that the overall system NF,



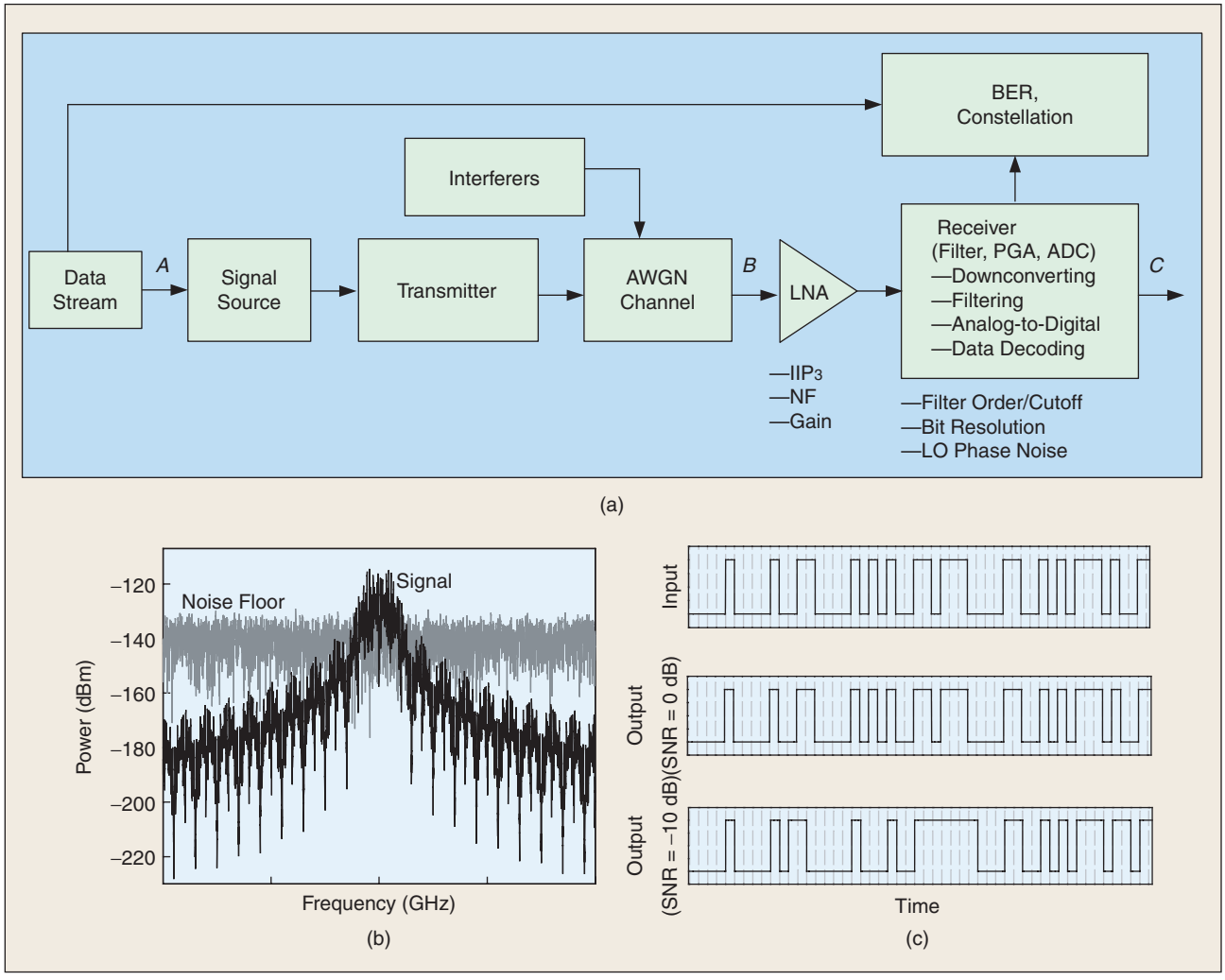
5. IEEE 802.15.4-based 2.4 GHz radio transmitter (a) system simulation setup, (b) time domain data stream at points A and B, and (c) the spectrum mask at point C.

nonlinearity requirements, and gain are set in the LNA block, while the other blocks are idealized to simplify the simulations.

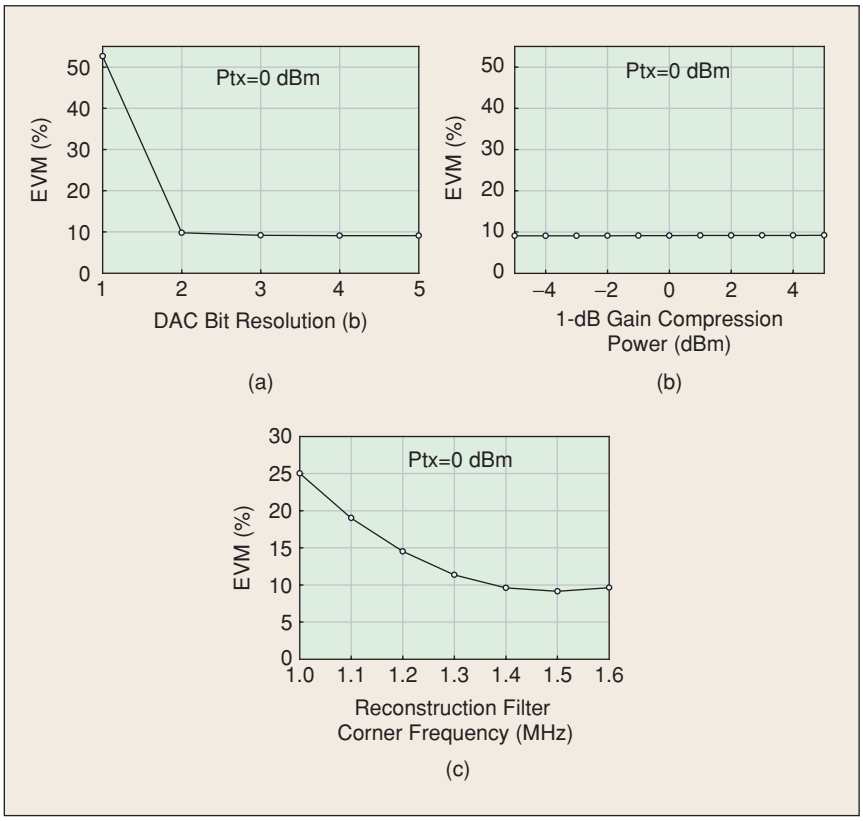
Figure 5(b) and (c) shows the simulated time domain data stream and the transmitted spectrum, respectively. As shown in Figure 5(b), the 4-b data symbols (0000, 1000) are mapped into 32 chip sequences (1101100 . . . , 1110110), converted to parallel I/Q chip data, and then half-sine pulse shaped in the digital baseband. Positive half-sine is assigned for binary 1 state, and similarly negative half-sine for binary 0 state. The PSD of the output signal spectrum is shown in Figure 5(c) along with a spectrum mask. IEEE 802.15.4 specifies a relative limit of −20 dB and an absolute limit of −30 dBm power at and above 3.5-MHz frequency offset [1]. This kind of O-QPSK modulation with half-sine pulse shaping allows smooth phase transitions in the I/Q signal constellation, resulting in a constant envelope of output and avoidance of spectral regrowth when amplified by a less linear amplifier, while widening the main lobe [6].

The modulation accuracy of the transmitter is determined with an error vector magnitude (EVM) measurement. IEEE 802.15.4 specifies the transmitter should have EVM values of less than 35% (−9 dB) when measured for 1,000 chips. The EVM is measured on baseband I and Q chips after recovery through a reference receiver. The EVM in the transmit chain of a radio transceiver can be affected by several factors such as output-stage nonlinearity, DAC nonideality, LPF nonideality, and VCO nonideality. Figure 7 shows the simulated EVM performances by varying the DAC bit resolution, 1-dB gain compression power of the output driver amplifier, and the corner frequency of the DAC reconstruction filter. The simulation results show that increasing the DAC resolution beyond 3 b does not further improve EVM performance. Also, the EVM performance of the transmitter is not affected by the 1-dB gain compression point of the driver amplifier due to the use of the constant envelope modulation scheme, DSSS-OQPSK. The corner frequency of 1.5 MHz is set for the reconstruction filter.

Figure 6(b) and (c) shows the input power spectrum along with an AWGN and the received decoded data stream with different SNR, respectively. As shown in Figure 6(b), the dc offset problem of the direct conversion receiver can be relaxed by allowing the use of high pass filtering near the dc [8] since there is no dc component at the center frequency (i.e., null



6. IEEE 802.15.4-based 2.4 GHz radio receiver (a) system simulation setup, (b) the received input power spectrum along with an AWGN shown at point B, and (c) time domain data stream of original transmitted data at point A compared to the decoded data stream with SNR = 0 dB, and −10 dB at point C.



7. System simulation results in the 2.4 GHz PHY transmit path. EVM performances are simulated with different (a) DAC bit resolution, (b) 1 dB gain compression power, and (c) reconstruction filter corner frequency.

point at the center frequency). Figure 6(c) shows that the original input data (0000, 1000, 0100, . . .) at the transmitter is decoded correctly at the receiver with SNR = 0 dB while corrupted with SNR = −10 dB.

Figure 8(a) shows the sensitivity simulation by varying the input power level. Since the BER simulation takes such a long time, BER is extrapolated for above −94 dBm input level. For 1% PER, the sensitivity of the receiver would be about −90 dBm with a system NF of 20.5 dB. As shown in Figure 8(a), the insets show an eye diagram and a constellation of I/Q signals distorted by noise. In the constellation, the phase transitions are smoothed, resulting in constant envelope [4], [6]. Figure 8(b) and (c) shows the simulated BER performances by varying the ADC bit resolution and the channel filter corner frequency, respectively. The simulation results show that at least 4 b should be used for the ADC so as not to degrade the receiver BER performance significantly, and the corner frequency of 1.6 MHz can be set for the channel filter.

The mismatches between I and Q path of the receiver cause impairments of the down-converted signal constellation, thereby raising the BER. The simulations are performed with a reference transmitter and a receiver by introducing gain and phase errors in the receiver, and the EVM performances are plotted. As shown in Figure 8(d), the simulation results show that gain error affects receiver performance significantly. Gain error of less than 1 dB and phase error of less than 5° can be optimal for the transceiver implementation.

Recently, a commercial version of an IEEE 802.15.4-based 2.4-GHz radio transceiver chip was released [13]. Since the transceiver should satisfy both low-power consumption and low-cost, stringent trade offs are required for system NF, nonlinearity, gain, power consumption, and chip area. For low-power consumption, several circuit implementation methods have already been developed [14]–[15]. In [14], micropower CMOS front-end blocks, including an LNA and down-conversion active mixer, are implemented using high quality factor off-chip inductors fabricated in low-cost, low-temperature, cofired-ceramic (LTCC) technology. Also, a micropower CMOS VCO has been reported that has a single sideband phase noise of less than −100 dBc/Hz at 100 kHz offset frequency using the same technology. The other method for a low-power circuit is based on the current reused technique in which several blocks are stacked like a cascode configuration [15].

To meet low-cost requirements, it is necessary to minimize the use of on-chip spiral inductors that occupy a very large silicon area. Instead, off-chip high-Q inductors are used. With relaxed system requirements for the 2.4-GHz PHY, inductive loading for RF blocks is to be avoided as much as possible. Finally, the receiver front-end blocks can be designed using passive mixers to reduce power consumption. By adopting passive mixers, the 1/f noise problem can be avoided or reduced in the receive path, which can otherwise pose serious problems for direct conversion architecture since the 1/f noise corner frequency extends over 1 MHz for submicron CMOS technology. Based on the radio system specifications derived from IEEE 802.15.4, a direct conversion 2.4-GHz PHY is implemented in 0.18-μm CMOS technology by exploiting the current reused techniques and off-chip inductors. The implemented chip size can be reduced further by employing minimal use of on-chip inductors (for example, just one on-chip inductor for VCO) and, thus, can achieve great cost advantage.

CONCLUSIONS

In this article, 2.4-GHz radio transceiver RF/analog system requirements are derived from the emerging personal area network application standard, IEEE 802.15.4. Exploiting the derived radio requirements, top-down system level simulations have been realized to see how the RF/analog blocks affect entire system performances. The chip is then implemented in 0.18-μm CMOS technology based on a direct conversion scheme by exploiting the current reused techniques and off-chip inductors.

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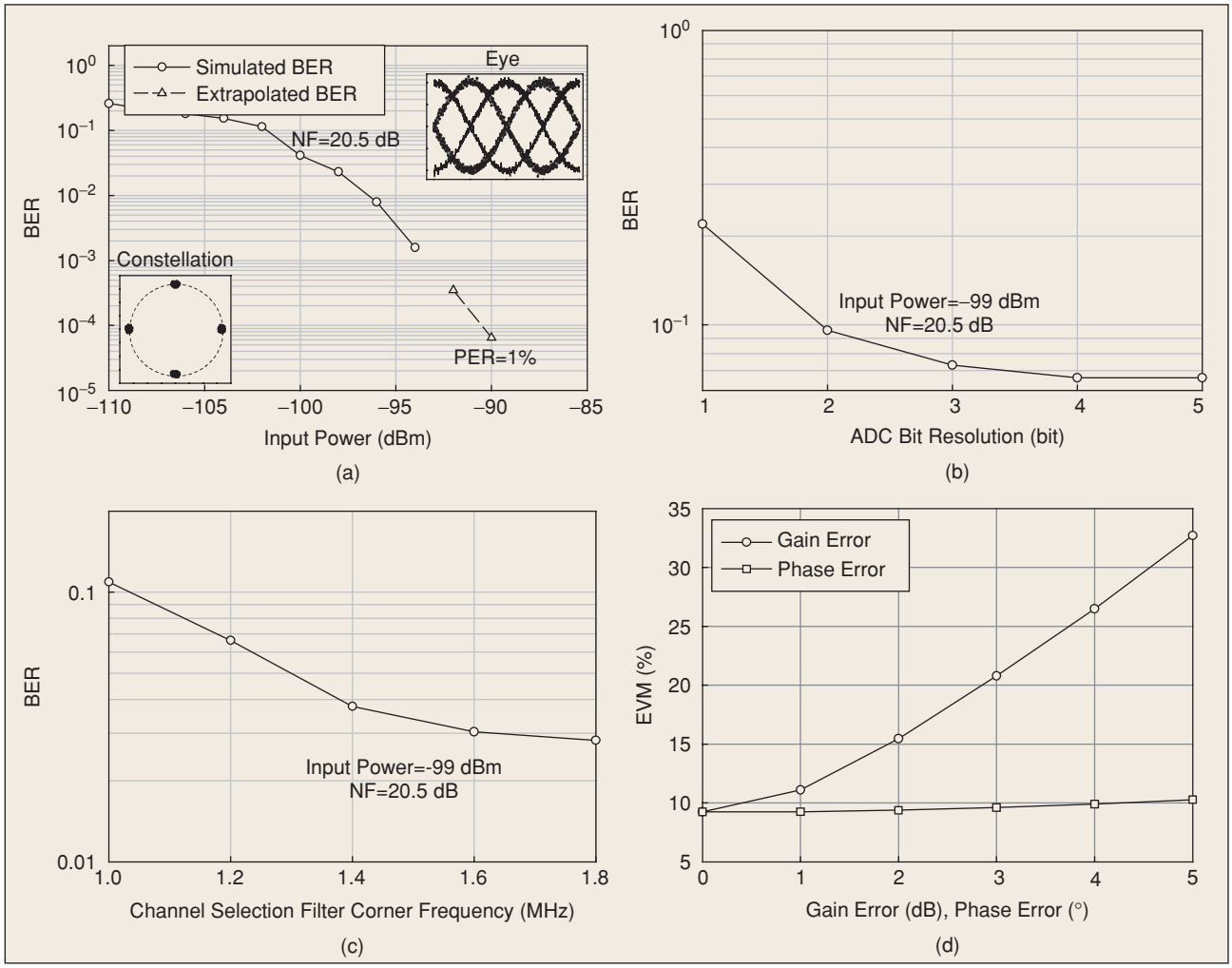

8. System simulation results in the 2.4 GHz PHY receive path. (a) Sensitivity performance with NF = 20.5 dB. The insets show an eye diagram, and a constellation distorted by noise, (b) BER performance with different ADC bit resolution, (c) BER performance with different corner frequency of the channel selection filter, and (d) EVM performance with different I/Q mismatch.