A Low-Power CMOS Direct Conversion Receiver With 3-dB NF and 30-kHz Flicker-Noise Corner for 915-MHz Band IEEE 802.15.4 ZigBee Standard

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***Abstract*—A low-power low flicker-noise receiver front-end for 915-MHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology is implemented. A power-constrained simultaneous noise and input matching low-noise amplifier (LNA) can be achieved by using a conventional inductive degeneration cascode amplifier with an extra gate–source capacitor. In combination with the LNA, a passive mixer showing low $1/f$ noise performance is adopted to convert the RF signal directly to the baseband signal. The measured results show a conversion gain of 30 dB and a noise figure of 3 dB with $1/f$ noise corner frequency of 30 kHz. Two-tone test measurements indicate -5-dBm input third-order intercept point and $+45$-dBm input second-order intercept point. The RF receiver front-end dissipates 2 mA from a 1.8-V supply.**

***Index Terms*—CMOS, direct conversion, IEEE 802.15.4, low power, noise optimization, $1/f$ noise, receiver.**

I. Introduction

RECENTLY, the demand for a low-cost low-power wireless transceiver utilizing standard CMOS technology has increased significantly [1], [2]. Especially with the introduction of the IEEE 802.15.4 ZigBee standard, which is a low-rate, low-cost, and low-power network [3], these demands tend to dominate transceiver developments. Table I shows the target markets and applications of the IEEE 802.15.4 ZigBee standard.

As can be seen in Table I, there are numerous applications for this low data-rate standard such as industrial and commercial, home automation, consumer electronics, personal health care, games, etc. that should be able to operate for six months or two years on just button cells or battery [4].

The direct conversion receiver (DCR) has recently attracted widespread attention for its simple architecture and easy integration with the baseband circuit, as well as for its low power consumption and potentially low manufacturing costs [5], [6]. However, the DCR has some disadvantages such as dc offset, even-order distortion, flicker noise, in-phase/quadrature (I/Q) mismatch, local oscillator (LO) leakage, etc. [6]. DC offset can be removed by using digital calibration [7] or a feedback-loop in the analog part [8]. The even-order distortion and I/Q issues can be solved by careful layout and symmetric tracing of RF and LO paths or by using digital calibration [9].

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TABLE I
TARGET MARKETS AND APPLICATIONS OF IEEE 802.15.4 STANDARD

Target Markets	Applications
Industrial & Commercial	Monitor, Sensors, Automation, Control
Home Automation	Security, Lighting, Locking, Heathing, Ventilation and air conditioning (HVAC)
PC peripherals	Mouse, Keyboard, Joystick, Gamepad
Consumer Electronics	TV, VCR, DVD, CD, Remote control
Personal Heath Care	Monitors, Diagnostics, Medical Sensors
Toy & Games	Pets, Games, Educational

TABLE II
FREQUENCY BAND AND DATA RATE OF IEEE 802.15.4 STANDARD

PHY (MHz)	Frequency band [MHz]	Speading Parameters		Data Parameters	
		Chip Rate (kchip/s)	Modulation	Bit rate (kb/s)	Symbol Rate (ksymbol/s)
868/915	868-868.6	300	BPSK	20	20
	902-928	600	BPSK	40	40
868/915 optional	868-868.6	440	PSSS	206.25	13.75
	902-928	1600	PSSS	250	50
868/915 optional	868-868.6	400	O-QPSK	100	25
	902-928	1000	O-QPSK	250	62.5
2450	2400-2483.5	2000	O-QPSK	250	62.5

With the key point of low-power and a low $1/f$ noise RF receiver front-end, the solution we are presenting is based on the low-power low-noise LNA followed by a passive mixer, which shows low $1/f$ noise performance [10]. This paper is organized as follows. Section II describes the receiver architecture and the radio specifications of the IEEE 802.15.4 standard such as the noise figure (NF), third- and second-order nonlinearity characteristics [input third-order intercept point (IIP3), input second-order intercept point (IIP2)], dc offset, and required filter characteristic. The receiver circuits design is described in Section III. Section IV summarizes experimental results of the implemented receiver front-end, and Section V concludes this study.

II. Receiver Architecture and Specifications

The 868/915-MHz-band IEEE 802.15.4 standard employ a direct sequence spread spectrum (DSSS) with three optional modulation types [3], i.e., binary phase-shift keying (BPSK), offset quadrature phase-shift keying (O-QPSK), and parallel sequence spread spectrum (PSSS) shown in Table II.

TABLE III
RECEIVER TARGET SPECIFICATIONS

Modulation Type	Sensitivity [dBm]	NF [dB]	IIP3 [dBm]	IIP2 [dBm]	SFDR [dBm]	Gain control range [dB]
BPSK	-92	19.5	-34	10	43.5	72
O-QPSK	-90	14.5	-32	10	41	70
PSSS	-92	18.5	-34	10	42.5	72

The overall performance of the ZigBee transceiver can be characterized by the packet error rate (PER) that defines the average fraction of transmitted packets that are not detected correctly. The required PER should be less than 1% measured over a random PHY service data unit (PSDU) data. The PER is related to the bit error rate (BER) by $\mathrm{PER} \approx N \times \mathrm{BER}$ where N is the number of bits per packet, which is approximately 20 B or 160 bits. Therefore, 1% PER corresponds to 0.00625% BER.

The probability BER of the BPSK modulation system is given by [11]

$$P_e = Q\left(\sqrt{2\mathrm{SNR}}\right) \tag{1}$$

where the signal-to-noise ratio is denoted by SNR. With 1% PER, the required SNR is approximately 8.5 dB. Employing the DSSS technique, the receiver has a processing gain of approximately 12 dB. The receiver processing gain can be calculated from the ratio of the chip to bit rate [12] (600 kchip/s to 40 kb/s). Therefore, the required minimum SNR, $(\mathrm{SNR}_{\min})$, is approximately -3.5 dB.

The sensitivity of the receiver system can be expressed as [13]

$$P_{\mathrm{in,min}} = -174\ \mathrm{dBm/Hz} + \mathrm{NF} + 10\log \mathrm{BW} + \mathrm{SNR}_{\min} \tag{2}$$

where the channel bandwidth in denoted by BW and NF is the total NF of the receiver system. Considering the minimum sensitivity of -92 dBm for BPSK and the bandwidth of 1.2 MHz for the 915-MHz band specified in the IEEE 802.15.4 ZigBee standard, the required NF of the receiver system calculated from (2) is approximately 24.5 dB. Assuming approximately 5-dB digital losses in the receiver, the maximum allowed system NF of the analog front-end (including RF and baseband sections) is approximately 19.5 dB.

Similarly, for the O-QPSK modulation scheme, the required SNR is approximately 8.5 dB, and then $\mathrm{SNR}_{\min}$ is 3.5 dB considering 6-dB processing gain (1000 kchip/s to 250 kb/s). With the minimum sensitivity of -90 dBm specified in standard and 5-dB loss of the digital part, the required maximum NF of the analog front-end is approximately 14.5 dB.

With the PSSS modulation scheme, the required SNR for 1% PER is approximately 5.8 dB [14]. Therefore, the required maximum NF of the analog front-end is 18.5 dB considering 8-dB processing gain (1600 kchip/s–250 kb/s), -92-dBm sensitivity, and 5-dB digital loss. The required NFs of analog for three different modulation schemes are compared in Table III.

The channel selection low-pass filter (LPF) requirement can be derived from the conditions of jamming resistance. The IEEE 802.15.4 standard requires 0-dB rejection at the adjacent channel (2 MHz apart) and 30-dB rejection at an alternate channel (4 MHz apart), which has some margin, 40-dB rejection at 4 MHz apart from the wanted signal is sufficient and, therefore, the third-order Butterworth-type LPF, which has approximately 47-dB rejection with corner frequency of 600 kHz, can be chosen for the channel selection filter.

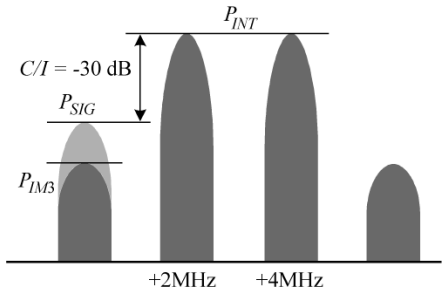

Fig. 1. Interferer profile.

The standard does not specify the receiver nonlinearity requirements such as IIP_3 or IIP_2. However, the nonlinearity requirements can be inferred from an interferer profile, as shown in Fig. 1, where two interfering channels are 2 and 4 MHz apart from the desired signal, respectively. As can be seen from Fig. 1, IIP_3 can be given by [13]

$$\mathrm{IIP}_3 = P_{\mathrm{SIG}} - \frac{3}{2}(C/I) + \mathrm{Margins} \tag{3}$$

where P_{SIG} is the signal power in dBm and C/I is the power ratio of carrier to interferer in decibels. Assume the signal power is 3 dB higher than the minimum sensitivity level, the calculated IIP3 for BPSK, O-QPSK, and PSSS modulation schemes are -34, -32, and -34 dBm, respectively, considering 10-dB reasonable margins.

Similarly, the second-order nonlinearity characteristic IIP_2 can be given by

$$\mathrm{IIP}_2 = P_{\mathrm{Bloc}} - (C/I) + \mathrm{Margins} \tag{4}$$

where P_{Bloc} is the power of the blocking interferer. With the blocking power of -30 dB, the calculated IIP_2 is 10 dBm for three different modulation schemes under the assumption that the reasonable margin is 10 dB.

The receiver spurious-free dynamic range (SFDR) is calculated from [13]

$$\mathrm{SFDR} = \frac{2}{3}(\mathrm{IIP}_3 - F) - \mathrm{SNR}_{\min} \tag{5}$$

where $F = -174\ \mathrm{dBm/Hz} + \mathrm{NF} + 10\log \mathrm{BW}$. From (5), the required SFDR is approximately 43.5, 41, and 42.5 dB for BPSK, O-QPSK, and PSSS modulation, respectively.

Fig. 2 shows the block diagram of the receiver path adopting a direct conversion scheme. The RF incoming signal is amplified by a low-noise amplifier (LNA) and then down-converted directly to the baseband by an I/Q mixer. The first stage in the baseband chain is the combination of the amplifier and first-order filtering. The baseband signal is then amplified by a variable gain amplifier (VGA) and filtered by a second-order LPF before it is fed into the digital part.

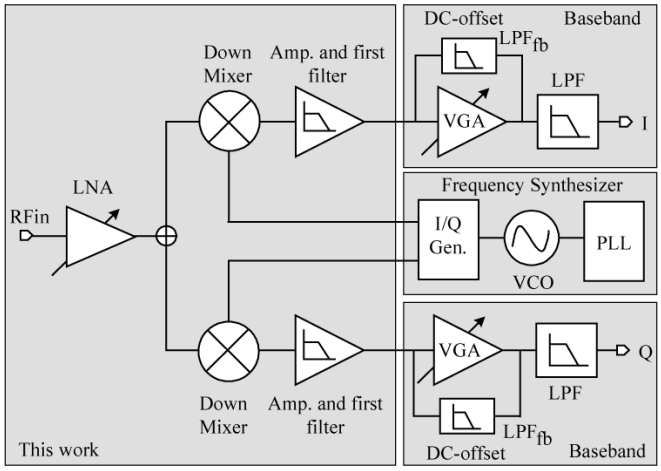

Fig. 2. Receiver architecture.

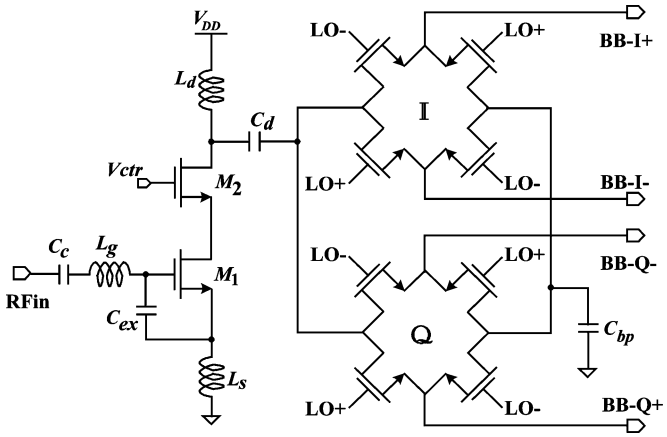

Fig. 3. Schematic of the RF Front-end.

For a DCR, strong interferers leaked to the LO port of the mixer or LO signal through various leakage paths (from the LO to RF port of the mixer, to the input of the LNA or to the antenna) can make self-mixing, thus producing a dc component at the mixer output. This dc component will corrupt the wanted signal and, hence, saturate the analog baseband amplifiers. To overcome this problem, a dc offset cancellation loop circuit is added in the analog baseband blocks. The dc offset loop is implemented by connecting a feedback loop ($\mathrm{LPF_{fb}}$) in the VGA, as shown in Fig. 2. The IEEE 802.15.4 standard requires the turnaround time to be less than 12 symbols [3]. With the 915-MHz band applications, the symbol rate is 40, 50, and 62.5 ksymbols/s for BPSK, PSSS, and O-QPSK modulation, respectively. As a result, the turnaround time is approximately 300, 240, and 192 μs for BPSK, PSSS, and O-QPSK modulation, respectively. A fast settling time of the dc offset cancellation loop is preferable and 1% setting time is set to be 30, 24, and 19 μs, the required corner frequencies of the LPF ($\mathrm{LPF_{fb}}$) need to be less than 25, 30, and 35 kHz for BPSK, O-QPSK, and PSSS modulation, respectively. Those required corner frequencies are calculated based on the relationship between the settling time and the bandwidth of the loop filter [15]. The relationship between the BER and the receiver power with several values of the cutoff frequency of $\mathrm{LPF_{fb}}$ has been simulated using Agilent's ADS simulator tool. The obtained results show that the cutoff frequency of $\mathrm{LPF_{fb}}$ can be chosen within 5% of the cutoff frequency of the LPF and the receiver needs only just 1 dB stronger signal power to have the same BER performance. With 600-kHz cutoff frequency of the LPF, the cutoff frequency of $\mathrm{LPF_{fb}}$ is 30 kHz. Although the required cutoff frequency of $\mathrm{LPF_{fb}}$ obtained from calculation is different for each modulation scheme, it has been found from simulation that 30-kHz cutoff frequency of $\mathrm{LPF_{fb}}$ can be used for three different modulation schemes with an acceptable increase in the received power. The overall target specification of the receiver is summarized in Table III. As can be seen in Table III, three modulation schemes have almost the same radio specifications, except the required NF. Therefore, this study attempts to design the receiver that satisfies the lowest NF requirement, meaning that the receiver can be used for three modulation schemes.

III. Circuits Design

In order to achieve the main goal of low-power and low $1/f$ noise, an RF front-end, shown in Fig. 3, is chosen. In this configuration, direct down-conversion is implemented by passive mixers without dc current. By this approach, the $1/f$ noise contribution from the mixers is made negligible. In this design, a single-ended RF drive of double-balanced mixers is used, which allows single-ended RF gain circuitry and reduces current consumption compared to a differential one. The output of the LNA is connected to one terminal of the differential RF input of the mixer via coupling capacitor C_d, while the second terminal of the mixer is connected to the ac ground through a bypass capacitor C_{bp}. From simulation results, we have found that, by using this approach, the gain of overall receiver front-end is reduced by 3 dB while taking full advantages of the differential circuitry.

A. LNA Design

The LNA has been designed to have very low-noise low-power consumption and to provide enough gain to sufficiently reduce the input referred noise contribution of the subsequent stages. Besides, the LNA should have 50-Ω input impedance to maximize the transferred signal from the antenna. Typically, an inductive degeneration cascode LNA topology is widely used since it provides high gain, low noise, wide-band, high isolation, etc. [16], [17]. In this configuration, the inductive degeneration L_s is used to achieve simultaneous noise and input matching since L_s generates the real part of the input impedance. This is important because there is no real part in the input impedance without degeneration, while there is in the optimum noise impedance [18]. Therefore, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, the imaginary part of input impedance is changed by $j\omega L_s$, and this is followed by nearly the same change in the optimum noise impedance, especially with advanced CMOS technology. However, under low power consumption, meaning low gate–source overdrive voltage or small transconductance g_m, the required L_s value that satisfies the simultaneous noise and input matching condition has to be very large. The problem is that for L_s to be greater than some value, the minimum NF ($\mathrm{NF_{min}}$) of a given technology can be increased significantly [19]. As a result, the minimum achievable

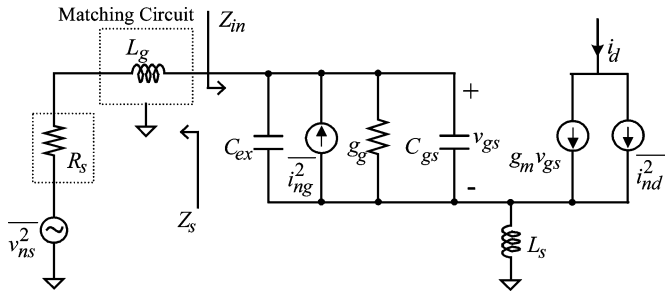

Fig. 4. Small-signal equivalent circuit of the LNA shown in Fig. 3 for noise analysis.

NF of the LNA can be considerably higher than its $\mathrm{NF}_{\min}$, spoiling the idea of simultaneous noise and input matching. To overcome this problem, the proposed LNA topology shown in Fig. 3 is used. As can be seen in Fig. 3, the LNA differs by one additional capacitor C_{ex} compared to the typical cascode LNA. The insertion of this capacitance adds a degree of freedom to play with to achieve a simultaneous noise and input matching at very low power consumption. This LNA topology was first introduced in [20] as a solution to reduce the NF of the LNA at low power dissipation; however, the potential and theoretical analysis as a power-constrained (i.e., low power) simultaneous noise and input matching (PCSNIM) LNA topology has not been recognized. Fig. 4 shows the simplified small-signal equivalent circuit of the LNA amplifier shown in Fig. 3 for noise analysis. In Fig. 4, the effects of common-gate transistor M_2 on the noise and frequency response are neglected [16], [17]. The noise parameter expressions for a circuit with series feedback, shown in Fig. 4, can be obtained by applying Kickoff's law and were derived by Nguyen *et al.* in [21] as follows:

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta\left(1-|c|^2\right)} \tag{6}$$

$$Z_{\mathrm{opt}} = \frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}} + j\left(\dfrac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\mathrm{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - sL_s \tag{7}$$

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{8}$$

where $C_t = C_{\mathrm{gs}} + C_{\mathrm{ex}}$ and other parameters are defined in Table IV.

As can be seen from (6) and (8), $F_{\min}$ and R_n are not affected by the addition of C_{ex}. In other words, by using C_{ex}, the minimum NF and noise resistance expressions of the LNA topology shown in Fig. 3 are the same as those in the conventional inductive degeneration topology [18]. From Fig. 4, the input impedance of the LNA is given by

$$Z_{\mathrm{in}} = sL_s + \frac{1}{sC_t} + \frac{g_m L_s}{C_t}. \tag{9}$$

In (9), the source degeneration generates a real part at the input impedance. Furthermore, from (9), the imaginary part of Z_{in} is changed by sL_s, and this is followed by nearly the same change in Z_{opt} in (8), especially with advanced technology considering the value of c is higher than 0.4 and α becomes lower than 1 [23], [24].

TABLE IV
LIST OF SYMBOLS

Symbols	Definition and Value
C_{gs}	Gate-source capacitor of transistor M_1
g_m	Transconductance of transistor M_1
V_{GS}	Gate-source voltage of transistor M_1
V_{DS}	Drain-source voltage of transistor M_1
ω_o	Operating frequency
ω_T	Cut-off frequency of M_1
δ	Constant, its value = 4/3 for long-channel devices
γ	Constant, its value = 2/3 for long-channel devices
c	Correlation coefficient between gate induced noise & channel noise, its value = 0.4 for long-channel devices

For the LNA circuit shown in Fig. 3, the conditions that allow the simultaneous noise and input matching are now

$$\frac{\alpha\sqrt{\dfrac{\delta}{5\gamma(1-|c|^2)}}}{\omega C_{\mathrm{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} = \mathrm{Re}[Z_s] \tag{10}$$

$$\frac{\left(\dfrac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)}{\omega C_{\mathrm{gs}}\left\{\dfrac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\dfrac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\dfrac{\delta}{5\gamma}}\right)^2\right\}} - \omega L_s = \mathrm{Im}[Z_s] \tag{11}$$

$$\frac{g_m L_s}{C_t} = \mathrm{Re}[Z_s] \tag{12}$$

$$\omega L_s + \frac{1}{\omega C_t} = -\mathrm{Im}[Z_s]. \tag{13}$$

As mentioned above, for the advanced CMOS technology parameters, (13) is approximately equal to (11). Therefore, (13) can be dropped, which means that, for the given value of L_s, the imaginary value of the optimum noise impedance becomes approximately equal to that of the input impedance with opposite sign. The design parameters that can satisfy (10)–(12) are now then V_{GS}, W (or C_{gs}), L_s, and C_{ex}. Since there are three equations and four unknowns, (10)–(12) can be solved for an arbitrary value of Z_s by fixing the value of one of the design parameters that can be the power dissipation or V_{GS}. In other words, this LNA design optimization technique allows us to design simultaneous noise and input matching at any given amount of power dissipation. The qualitative description of the PCSNIM design process is explained in details by Nguyen *et al.* in [21].

In this LNA topology, by changing the bias voltage of the cascode transistor V_{ctr}, we are able to vary the power gain. As the basic operating principle for the CMOS transistor suggests,

CMOS have high linearity with low gain in the linear region and low linearity with high gain in the saturation region. When $V_{\rm ctr}$ is in high-level state, two input transistors M_1, M_2 remain in the deep saturation region and high gain is obtained. Since the input signal is very small, the distortion is relatively low. On the contrary, when the input signal is high and $V_{\rm ctr}$ is in the low-level state, the input transistor M_1 stays in the linear region and low gain with low distortion can be obtained [25].

B. Mixer Design

High-performance mixers in CMOS are either active based on current switching or passive based on voltage switching mixers. One may argue that the passive mixer dissipates no dc current and gives high linearity. Besides, the absence of dc current through the switches also makes it possible to eliminate the $1/f$ noise, which otherwise is a problem for DCRs. Normally, nMOS transistors have better switch performance than pMOS transistors thanks to the higher mobility of electrons than holes [20]. Therefore, nMOS transistors were chosen for the switch.

In Fig. 3, the two parameters that designers can play with are the device's size and the LO characteristics. In order to have low noise performance, the width of the transistor should be large enough in order to provide a sufficiently low on resistance. However, when sizing the switches there will be tradeoff between the mixer noise performance and the gain of the LNA. The load impedance of the LNA consists of a parallel resonance circuit made up of the parasitic switch capacitance and the output inductor. If the switch capacitance is increased, the inductance must be decreased in order not to change the resonant frequency. The gain of the LNA will then decrease due to the lower load impedance. In this design, the optimum switching transistor's width is found to be 130 μm. The characteristics of the LO signal will affect the mixer performance [27]. The dc level of the LO signal is an important factor since it controls the switching mode. In the balanced drive case, the voltage conversion gain is theoretically equal to $2/\pi$. If the switches are set to have less on time than off time, often referred to as "break-before-make," the conversion gain will maximally equal 1 [27], but the mixer will also be less linear. Thus, there will also be a tradeoff between the mixer conversion gain and linearity. In order to eliminate $1/f$ noise, it is important that transistors are biased at the condition where there is no dc current flowing through the switch. In other words, the source and drain terminals are bias at V_{CM}, while their gate voltage is

$$V_G = V_{CM} + V_{\rm TH} \tag{14}$$

where $V_{\rm TH}$ is the threshold voltage of transistors. It has been found from simulation that when V_G is around 1.4 V with $V_{CM} = 900$ mV, this mixer shows $1/f$ noise-free operation. The conversion gain and NF of the passive mixer can be improved by applying high LO amplitude. However, in this study, 0-dBm LO power is applied considering the measured results of the fabricated voltage-controlled oscillator.

C. Baseband Amplifier and First Filter

The baseband amplifier and first filtering shown in Fig. 5 is implemented as a transimpedance amplifier with an *RC* combination as the feedback network. The bandwidth of this circuit

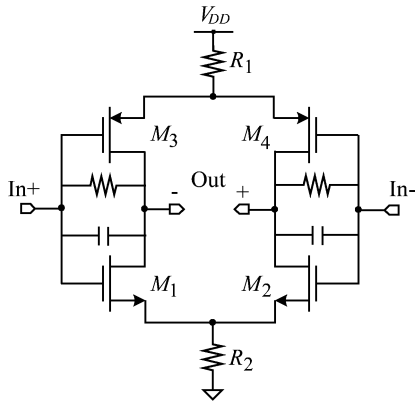

Fig. 5. Schematic of the baseband amplifier and first filter.

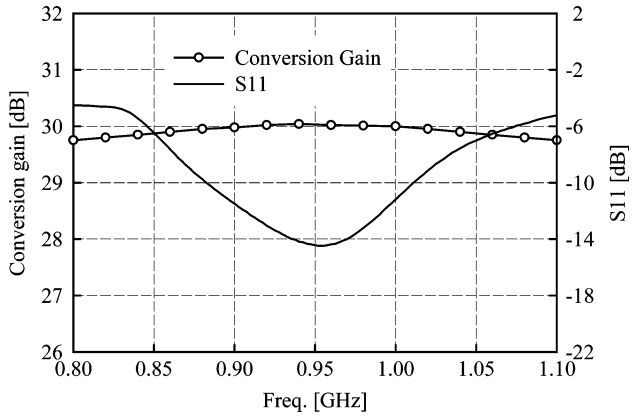

Fig. 6. Measured input return loss (S_{11}) and conversion gain of the RF receiver front-end.

can be controlled by capacitor; however, considering the bandwidth of the ZigBee standard, the bandwidth of this circuit is 1 MHz so that, in a zero-IF configuration, signals with a bandwidth of 2 MHz can be received. This circuitry not only provides some gain, but also filters high-order intermodulation products that affect the linearity of the following stages. To improve linearity of the circuit itself, the transistors have been degenerated resistively. From simulation, we have found that $1/f$ noise of the overall receiver front-end is mainly contributed by the first baseband amplifier and filter. In this design, the transistors were designed for a $1/f$ noise corner frequency below 30 kHz considering 30-kHz cutoff frequency of the dc-offset feedback loop used in the VGA. In other words, the $1/f$ noise caused by the baseband amplifier is removed by using the dc-offset feedback [22] with the lower cutoff frequency of 30 kHz.

IV. Experimental Results

The receiver front-end with ESD protection is fabricated in a 0.18-μm CMOS technology and consumed 2 mA from a 1.8-V supply. The testing board has been built by directly bonding the die on a two-layer FR4 substrate. To supply a differential signal at the input LO port, a commercial passive balun has been used and 5 dB of balun loss according to its measurement has been deembedded from the measurement.

Fig. 6 shows the measured input matching (S_{11}) and conversion gain of the receiver front-end sweeping the LO frequency

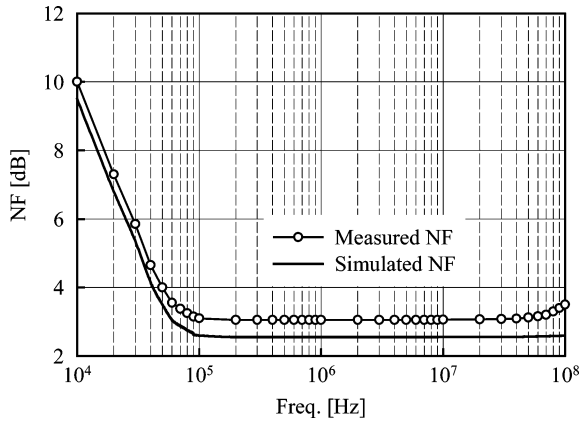

Fig. 7. Measured and simulated NF of the RF receiver front-end.

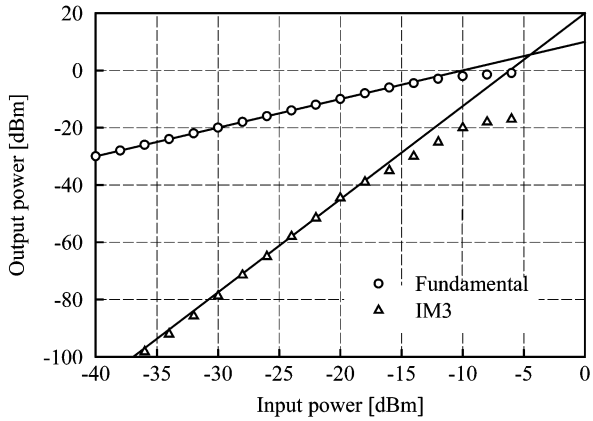

Fig. 8. Measured IIP3 of the RF receiver front-end.

across the entire target band (902–928 MHz). From Fig. 6, we can see that the input return loss of the receiver is lower than -13 dB and the conversion gain is approximately 30 dB and almost flat in the whole operating frequency band. The conversion gain variation of 10 dB is obtained by changing $V_{\rm ctr}$ of the LNA shown in Fig. 3. The receiver front-end NF was measured with the aid of a spectrum analyzer based on the method described in [29]. The measured NF result is shown in Fig. 7, which is approximately 3 dB in the center of the band with 30 kHz $1/f$ noise corner frequency. The simulated NF of this circuit is also plotted in Fig. 1 for comparison. As can be seen in Fig. 7, the measured NF result shows only 0.5 dB higher than the simulated one. Considering 30-kHz cutoff frequency of the dc-offset loop, we can conclude that the receiver front-end achieves very excellent noise performance. Fig. 8 shows the measured IIP3 result of the receiver front-end, which is approximately -5 dBm when the two-tone signal spaced by 500 kHz are applied. The other nonlinearity properties such as IIP2, input 1-dB compression point, and LO-RF leakage of the receiver front-end are also measured. The overall simulated and measured performances of the receiver front-end are compared and summarized in Table V. Fig. 9 shows the microphotograph of the fabricated receiver front-end, which has an active area of 1 mm^2. The silicon area is mainly occupied by the baseband amplifier and filter circuit.

TABLE V
SIMULATED AND MEASURED RF RECEIVER PERFORMENCES

Parameters	Simulated	Measured
Conversion gain [dB]	30	30
Input return loss [dB]	-20	-14
Gain variation [dB]	10	10
Noise figure [dB]	2.5	3
1/f noise corner frequency [kHz]	30	30
IIP3/IIP2 [dBm]	-5/50	-5/45
Input P-1dB [dBm]	-15	-15
LO-RF leakage [dB]	80	58
Current consumption [mA]	1.8	2
Operating frequency [MHz]	915	
Supply voltage [V]	1.8	
Technology [μm]	0.18 CMOS	

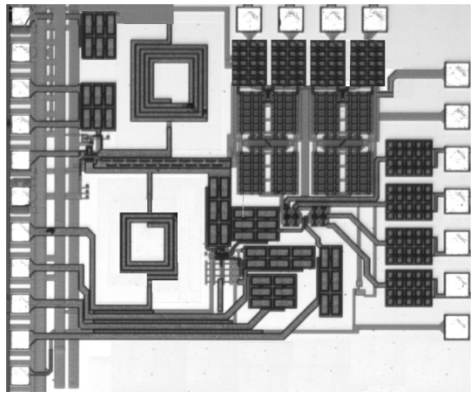

Fig. 9. Microphotograph of the fabricated chip.

V. CONCLUSION

An IEEE 802.15.4 ZigBee standard for low-cost low-power purposes has been finalized. Based on the physical layer requirements, the radio specifications for three modulation types, i.e., BPSK, O-QPSK, and PSSS, have been realized for a direct conversion architecture. The demonstrator receiver front-end is fabricated in a 0.18-μm CMOS process and consists of an LNA, a passive down-conversion mixer, and a combination of a baseband amplifier and first filtering circuit. For the LNA design, to achieve PCSNIM, the conventional inductive degeneration cascode amplifier with an extra gate–source capacitor is employed. With the main goal of low-power and low $1/f$ noise, a passive mixer dissipating no dc current and showing excellent $1/f$ noise is adopted to convert an RF signal directly to a baseband signal. The flicker-noise-free operation can be obtained by choosing the correct bias voltage of the switching transistors. The measured results show conversion gain of 30 dB and an NF of 3 dB with $1/f$ noise corner frequency of 30 kHz. Two-tone test measurements indicate -5-dBm IIP3, $+4$-dBm IIP2. The receiver front-end dissipates 2 mA from a 1.8-V supply.

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