RF CMOS LC-Oscillator With Source Damping Resistors

Seok-Ju Yun, Chong-Yul Cha, Hyoung-Chul Choi, and Sang-Gug Lee

***Abstract*—This letter proposes a new method to suppress the $1/f$ noise contribution of active devices in an oscillator using source damping resistors. The operational mechanism of the proposed source damping resistor method is analyzed through circuit simulation with a complementary LC-oscillator. The reduced $1/f$ noise leads to the phase noise improvement by suppressing $1/f$ noise up-conversion to phase noise. The measurement result shows that there is about 6.0 dBc and 4.0 dBc of phase noise improvement at 10 kHz and 100 kHz offset frequency with differential complementary LC-oscillator topology, respectively.**

***Index Terms*—Complementary metal oxide semiconductor (CMOS), damping resistors, $1/f$ noise, phase noise, voltage controlled oscillator (VCO).**

I. Introduction

With the improvement of radio frequency (RF) CMOS technology, active research to develop compact and multifunction wireless terminals is in process using one-chip CMOS radio transceivers. Recently, advanced RF silicon CMOS technologies have solved many problems related to the conductive substrate, interconnection line resistance, and operation speed of active devices, etc. But, even though the performances of RF CMOS transistors have been improved, the inherent $1/f$ noise is still an obstacle to the design of an integrated low phase noise VCO. The impact of $1/f$ noise becomes more severe with the decrease in channel length.

In prior research related to VCO design, many different approaches are used to decrease the $1/f$ noise to the phase noise contribution. The first method is to use p-channel devices which have a decade lower $1/f$ noise than n-channel devices [1], [2]. The second method is to use capacitive coupling to suppress the $1/f$ noise up-conversion in the differential LC oscillator [3]. The third method is to control the body node bias in the ring oscillator [4]. The fourth method is to replace the current source as an LC tank circuit to remove the $1/f$ noise contribution by the tail current [5]. The fifth method is the symmetric VCO design approach [6].

In this letter, a new and simple method using the source damping resistor is introduced to suppress $1/f$ noise in the oscillator. The new $1/f$ noise suppression method is then proven experimentally with a fully integrated complementary differential and single-ended oscillator using the 0.18-μm and 0.35-μm CMOS process, respectively.

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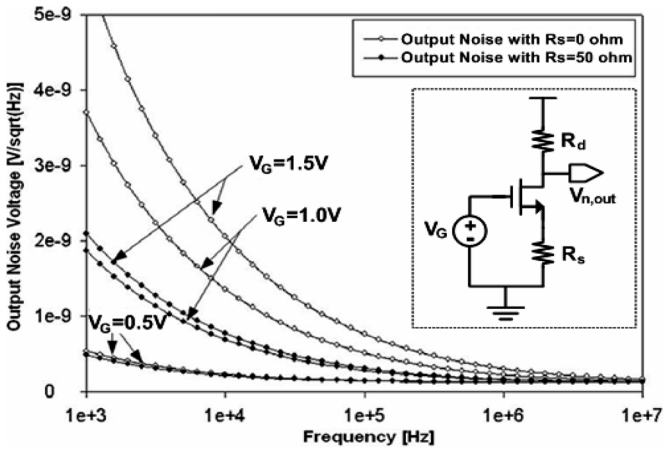


Fig. 1. Low frequency output noise voltage $(v_{\mathrm{n,out}})$ for common source topology with degeneration resistor, R_s.

II. 1/f Noise in CMOS Common-Source Topology

Low frequency $1/f$ noise is an inherent property of silicon transistors. Between CMOS and bipolar transistors, it is known that the CMOS transistor has the higher $1/f$ noise spectral density and that corner frequency reaches from several hundred kHz to several MHz. The $1/f$ noise of the CMOS transistor can be modeled as a voltage source in series with the gate, which is inversely proportional to the size of the transistor and frequency. Thus, the more CMOS technology is scaled-down, the more serious the effect of $1/f$ noise. As well, in CMOS oscillators, since the $1/f$ noise is the cause of the close-in phase noise near the carrier in the $1/f^3$ region, the phase noise performance below several MHz offset frequency is dominated by the $1/f$ noise of MOS transistors. In the MOS transistor, the output noise current increases in proportion to the square of the transconductance. Conventionally, an oscillator generates a large signal swing which leads to large transconductance (g_m) variation. Thus, the large signal swing may generate excess $1/f$ output noise current during oscillation. However a cautiously selected degeneration resistance can suppress the excess $1/f$ output noise current. Fig. 1 shows the simulated output noise voltage for a common-source topology with source degeneration resistor. In Fig. 1, R_s and R_d are the degeneration and load resistors, respectively. V_G is the gate bias voltage, and $v_{\mathrm{n,out}}$ the output noise voltage.

In Fig. 1, the output noise voltage is simulated for $R_s = 0$ and 50 Ω, where $R_d = 1\ \Omega$. As can be seen in Fig. 1, the degeneration resistor suppresses the low frequency output $1/f$ noise, especially for large gate bias voltage ($V_G = 1.0$ V and 1.5 V).

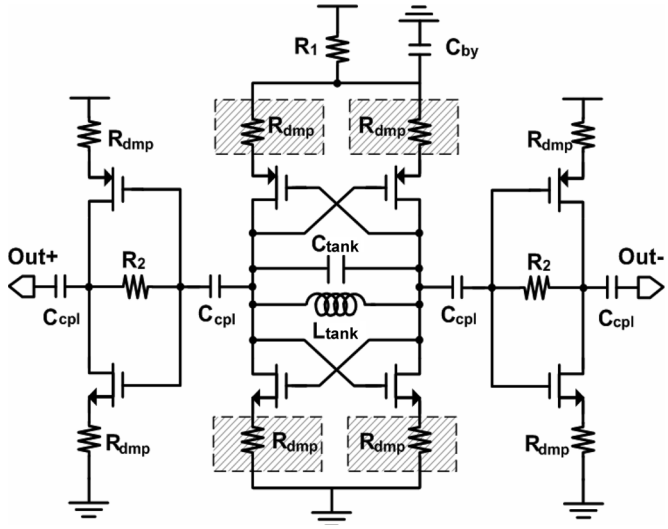


Fig. 2. CMOS complementary differential LC oscillator with damping resistors.

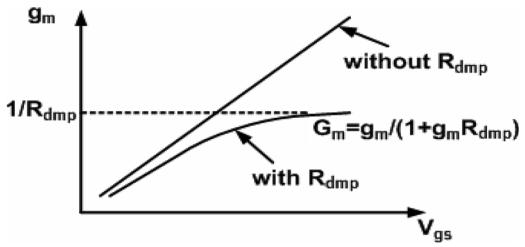


Fig. 3. Transconductance curve versus $V_{\rm gs}$ with $R_{\rm dmp}$ without $R_{\rm dmp}$.

This means that if the properly selected degeneration resistors are adopted in a CMOS oscillator, the $1/f$ noise output current of the CMOS transistor at oscillation peak can be suppressed and which lead to phase noise improvement.

III. CMOS LC Oscillators With Source Damping Resistors

Fig. 2 shows a complementary differential LC oscillator with source damping resistors. The source degeneration resistors are renamed "damping resistors" since they work as damping factors during oscillation [7]. As shown in Fig. 2, each NMOS and PMOS transistor has a damping resistor, $R_{\rm dmp}$, in series with source node. C_{by} is a bypass capacitor to the ground node and R_1 is used to control the dc bias current. Tank inductance, $L_{\rm tank}$, and capacitance, $C_{\rm tank}$, are selected to oscillate at the 2-GHz band. From [6], the $1/f^3$ corner in the phase noise spectrum can be given

$$\omega_{1/f^3} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2 = \frac{K}{C_{ox}WL} \cdot \frac{g_m^2}{\gamma \cdot g_{do}} \cdot \frac{1}{4kT} \cdot \left(\frac{c_0}{c_1}\right)^2 \quad (1)$$

where $\omega_{1/f}$ is the corner of the transistor $1/f$ noise and c_o and c_1 represent first and second Fourier series coefficient of the impulse sensitivity function (ISF). Equation (1) shows that the $1/f^3$ corner of the phase noise spectrum can be reduced by decreasing the g_m of the transistors. Fig. 3 shows the simulated g_m of transistor versus $V_{\rm gs}$. As shown in Fig. 3, the overall transconductance of transistor, G_m converges to $1/R_{\rm dmp}$ at the large gate voltage. Therefore, compared to the conventional oscillator, the oscillator which adopts $R_{\rm dmp}$ in Fig. 2 presents lower g_m variation over large voltage swing. The $1/f^3$ corner is also reduced by improved symmetry of the output swing, which is represented by c_o in (1) [6]. The complementary type oscillator provides more symmetric rise and falling time symmetry and addition of the $R_{\rm dmp}$ also results in improved symmetry of output current by reducing some amount of instant current [7]. Therefore, the reduction of transconductance, especially for a large voltage swing and improvement of symmetry with $R_{\rm dmp}$ improve the phase noise of the oscillator at low offset frequency. Fig. 4 shows simulated phase noise and tank voltage swing versus $R_{\rm dmp}$ at 100 kHz with the schematic shown in Fig. 2. As shown in Fig. 4, the tank voltage swing decreases linearly with an increase in $R_{\rm dmp}$ while the phase noise shows an optimum point at $R_{\rm dmp} = 40\,\Omega$. Considering that phase noise at low offset frequency is dominated by $1/f$ noise, optimum damping resistors effectively suppress the $1/f$ noise of active devices in the CMOS oscillator. The increases in phase noise in Fig. 4, at high $R_{\rm dmp}$ is due to the considerable decrease of voltage swing and increase of thermal noise in $R_{\rm dmp}$. Nevertheless, proper selection of the source damping resistor leads to phase noise reduction in the complementary LC-oscillator where $1/f$ noise dominates.

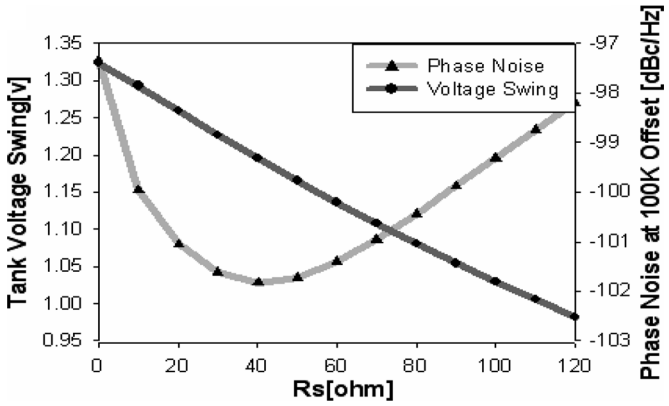


Fig. 4. Simulated phase noise at 100-kHz offset and tank voltage swing versus $R_{\rm dmp}$ value.

IV. Measurement Results

To prove experimentally the effectiveness of the proposed source damping resistor method, the differential LC oscillator in Fig. 2 and single colpitts oscillator in Fig. 5 are implemented using 0.18-μm and 0.35-μm CMOS technology, respectively. Two cases of source damping resistors a) $R_{\rm dmp} = 0\,\Omega$, and(b) $R_{\rm dmp} = 40\,\Omega$ are selected for oscillators as shown in Figs. 2 and 5. Each oscillator has an inverter amplifier as a buffer. With 1.8-V supply voltage, the differential oscillators with $R_{\rm dmp} = 40\,\Omega$ and $R_{\rm dmp} = 0\,\Omega$ oscillate at 2.2 GHz and 2.22 GHz, respectively, and the single oscillator with $R_{\rm dmp} = 40\,\Omega$ and $R_{\rm dmp} = 0\,\Omega$ oscillate at 1.84 GHz and 1.85 GHz, respectively.

Measured phase noise performances are plotted in Fig. 6. As shown in Fig. 6, better phase noise performance is achieved with $R_{\rm dmp} = 40\,\Omega$ than with $R_{\rm dmp} = 0\,\Omega$ in two different-type oscillators. As the offset frequency becomes lower, the phase noise with $R_{\rm dmp} = 40\,\Omega$ shows more improvement, which

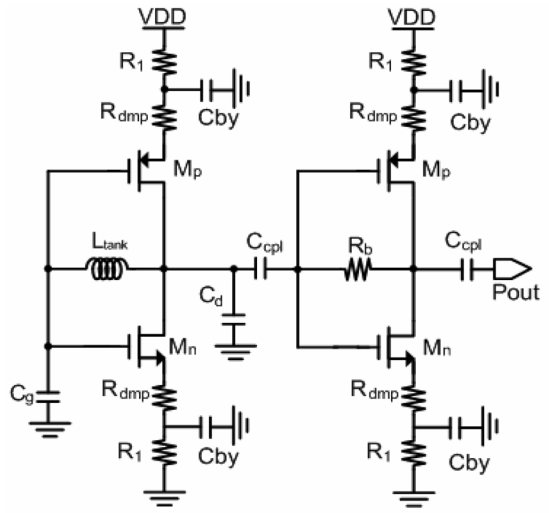


Fig. 5. CMOS complementary colpitts oscillator with damping resistors.

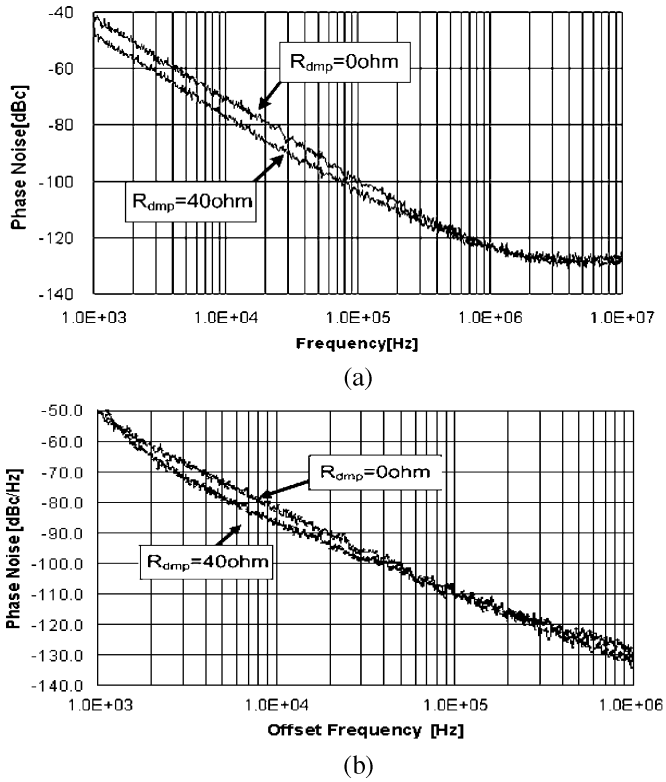
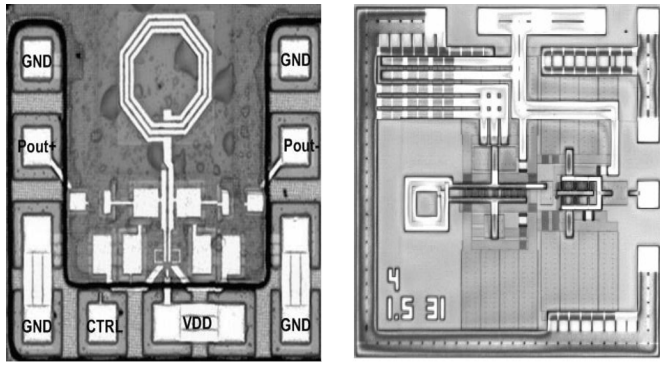


Fig. 6. Measured phase noise performance for the cases of $R_{\rm dmp} = 0\ \Omega$ and $40\ \Omega$ (a) differential (0.18-μm CMOS), (b) single-ended (0.35-μm CMOS).

proves that source damping resistors can effectively suppress the $1/f$ noise contribution of active devices in the CMOS oscillator. Compared to Fig. 6(b), more improvements and higher cross-over points of the phase noise in Fig. 6(a) can be explained by the fact that the scaled CMOS transistor has more serious $1/f$ noise than the less scaled one. From Fig. 6(a), the phase noise improvement with $R_{\rm dmp} = 40\ \Omega$ is shown to be about 6.0 dBc, 4.0 dBc, and 1.0 dBc of phase noise improvement at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. Fig. 7 shows the micrographs of the fabricated LC oscillators. In Table I, measurement results are summarized.



(a) (b)

Fig. 7. Micrograph of fabricated LC-oscillator (a) differential (b) single-ended.

TABLE I
MEASUREMENT RESULTS WITH 1.8-V SUPPLY VOLTAGE (a) DIFFERENTIAL (0.18-μm CMOS)(b) SINGLE-ENDED (0.35-μm CMOS)

	R_{dmp} [Ω]	I_{DC}* [mA]	Freq [GHz]	Phase Noise [dBc] 10kHz	100kHz	1MHz
a)	0	11.3	2.20G	-70.6	-99.9	-122.5
	40	10.3	2.22G	-77.1	-103.5	-122.2
b)	0	16.6	1.84G	-81.49	-110.7	-131.3
	40	15.5	1.85G	-86.88	-110.9	-129.8

I_{DC}* includes current of inverter buffer amplifier.

V. CONCLUSION

A new source resistor damping method to suppress $1/f$ noise up-conversion in a CMOS oscillator is proposed. The simulation results show that the amount of $1/f$ noise can be suppressed substantially using source damping (degeneration) resistors. Two kinds of complementary LC CMOS oscillators with different damping conditions, a) $R_{\rm dmp} = 0\ \Omega$ and b) $R_{\rm dmp} = 40\ \Omega$ are fabricated with 0.18-μm and 0.35-μm CMOS technology. In the differential LC oscillator, measurement results show that there is about 6.0 dBc, 4.0 dBc, and 1.0 dBc of phase noise improvement at 10 kHz, 100 kHz, and 1 MHz offset frequency with damping resistors, respectively.

REFERENCES

[1] C.-M. Hung and K. K. O. , "A 1.24-GHz monolithic CMOS VCO with phase noise of 137 dBc/Hz at a 3-MHz offset," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 3, pp. 111–113, Mar. 1999.

[2] Y.-K. Chu and H.-R. Chuang, "A fully integrated 5.8 GHz U-NII band 0.18- μm CMOS VCO," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 7, pp. 287–289, Jul. 2003.

[3] S.-W. Yoon and E.-C. Park, "5 ~6 GHz-band GaAs MESFET-based cross-coupled differential oscillator MMICs with low phase-noise performance," *IEEE Microw. Wireless Compon. Lett.*, vol. 11, no. 12, pp. 495–497, Dec. 2001.

[4] M. H. Kazemeini, M. J. Deen, and S. Naseh, "Phase noise in a back-gate biased low-voltage VCO," in *Proc. IEEE ISCAS'03*, May 2003, pp. 701–704.

[5] A. Ismail and A. A. Abidi, "CMOS differential LC oscillator with suppressed up-converted flicker noise," in *IEEE ISSCC Tech. Dig.*, Feb. 2003, pp. 98–99.

[6] A. Hajimiri and T. H. Lee, "Phase noise in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1998.

[7] C. Y. Cha and S. G. Lee, "RF CMOS differential oscillator with source damping resistor," in *Proc. IEEE RFIC Symp.*, 2005, pp. 339–402.