Spiral Inductor Design for Quality Factor

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Abstract − **A closed form expression for the quality factor of the spiral inductor, methodologically, is presented as a function of the inductance (L_{ind}), metal-line width (W), spacing (S), inner and the diameter (D_i). For a given inductance, the dependences of quality factor on W, S, and D_i are analyzed, and suggested the design optimization guidelines.**

Index Terms − **spiral inductors, silicon, RF Ics, quality factor.**

I. Introduction

Since the arrival of the silicon-based RF IC era, much effort has been put into the spiral inductor designs. The main focus of the endeavor was to improve the quality factor. The major concern for the silicon-based spiral inductors has been the resistivities of the metal and the silicon substrate. Numerous techniques have been proposed to reduce the resistivities of the interconnect lines and the silicon substrates [1,2]. Yet, many planar spiral inductor structures have been designed and evaluated without a clear understanding for the layout dependences of the quality factor. Simple and clear guidelines of inductor layout rules for optimum quality factor are presented for the required inductance and process information.

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II. Quality Factor Equation and Inductor Designs

Figure 1 shows the top view of a square spiral inductor layout. Mohan [3] reported a simple and very accurate expression for the planar spiral inductor inductances. Modifying the Mohan's work, for the inductor dimensions shown in Fig. 1, the inductance can be expressed as

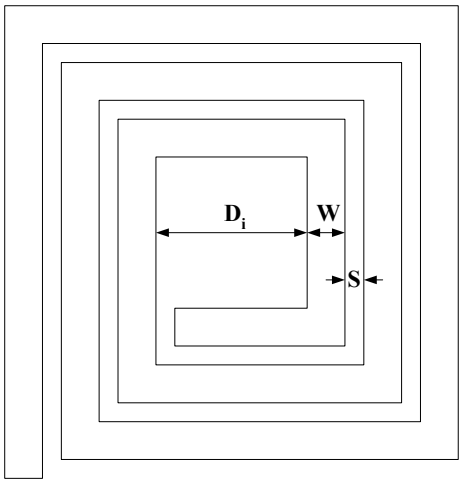

Fig. 1. A planar square spiral inductor structure.

$$L_{ind} = \frac{K_i \mu_0 n^2 \{D_i + nW + (n-1)S\}^2}{D_i(1+K_2)\{nW + (n-1)S\}} \quad (1)$$

where K_1 and K_2 are the constants of the value 2.34, and 2.75, respectively, μ_0 the permeability, n the number of turns, W the metal width, S the metal spacing, D_i the inner diameter, respectively. For the inductor dimensions of Fig. 1, the overall resistance of the inductor can be given by

$$R_{ind} = 4R_{\square}\left\{\frac{nD_i + n(n-1)(W+S)}{W} + 0.56n + 0.11\right\} \quad (2)$$

where $R_{\square}$ is the sheet resistance of the metal-line.

At frequencies low enough so that the inductor parasitic capacitances have negligible effects and/or the parasitic capacitances are small enough to neglect, the quality factor of the inductor can be expressed as a function of L_{ind} and R_{ind}

$$Q_{ind} = \varpi L_{ind} / R_{ind} = function(\varpi, W, S, D_1, n) \quad (3)$$

where ω is the frequency of operation. Solving equation (1) for n and substitute into (3), Q_{ind} can be expressed, though numerically complex, as a function of W, S, D_i, and L_{ind}

$$Q_{ind} = function(\varpi, W, S, D_1, L_{ind}) \quad (4)$$

With typical silicon-based planar spiral inductor, the metal to substrate capacitance, C_{ox}, dominates the parasitic capacitances. When the energy saved on the parasitic capacitances becomes non-negligible to the energy saved on inductor, the quality factor starts to degrade from what equation (3) predicts [4]. The amount of deviation depends on the frequency, inductor size, or the oxide thickness. With technology scaling, fortunately, the oxide thickness tends to increase as the process accommodates more metal layers. Practically, at RF frequencies (0.3 ~ 3 GHz), equation (3) would be a good approximation, for the inductors designed with top metal layer and inductances below 5 nH. Note that the typical sizes for the on-chip inductors are below 10 nH and often below 5 nH at frequencies around 2 GHz or higher. With high resistivity substrate or the compound semiconductor, equation (3) would be valid for most realistic cases. Generally, equation (3) offers the upper limit. As a 1st-order approximation, the C_{ox} can be estimated from the metal-area and the oxide-thickness, and incorporated to reflect the Q-factor degradation. Typically, at RF frequencies, the power losses through the silicon substrate are insignificant.

From equation (4), the dependences of Q_{ind} on design parameters can be experimented for a given inductance L_{ind}. The default values are assumed as $\omega = 2$ GHz, $R_{\square} =$ 40 mΩ/□, $W = 10$ μm, $S = 1$ μm, and $D_i = 50$ μm. It is obvious that the quality factor will increase with ω and $R_{\square}$.

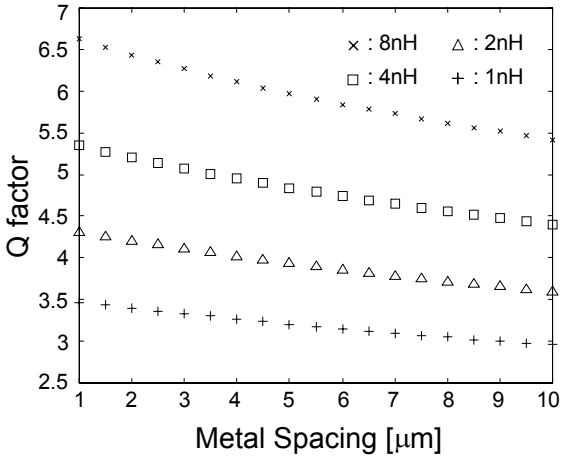

Fig. 2. The dependence of Q_{ind} on the metal spacing S where $\omega = 2$ GHz, $W = 10$ μm, $D_i = 50$ μm, and $\rho_{sh} = 40$ mΩ/□.

Figure 2 shows the dependence of Q_{ind} on the metal-spacing S for the inductances of 1, 2, 4, and 8 nH. Figure 2 justifies the minimum metal spacing that has been practiced in many RF IC designs. In Fig. 2, the Q-factor degrades about 15% for the metal spacing comparable to the metal width.

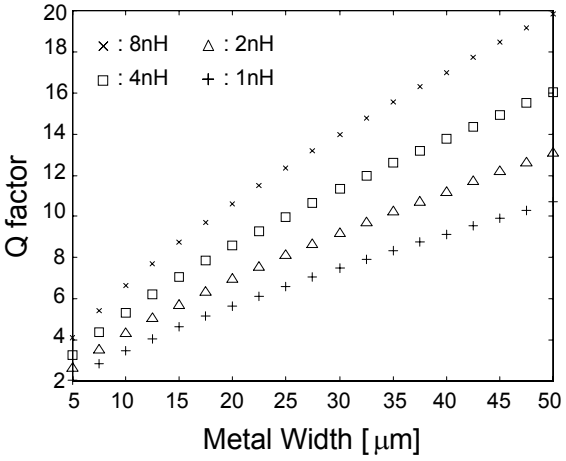

Fig. 3. The dependence of Q_{ind} on the metal width W where $\omega = 2$ GHz, $S = 1$ μm, $D_i = 50$ μm, and $\rho_{sh} = 40$ mΩ/□.

Figure 3 shows the dependence of Q_{ind} on the metal-width W. From Fig. 3, the Q-factor depends most strongly on W, nearly linear. Therefore, other than the concern for the C_{ox} and the inductor size, wider W is better for higher quality factor.

Figure 4 shows the dependence of Q_{ind} on the inner-diameter D_i. As can be seen from Fig. 4, there is an optimum inner diameter ($D_{i,opt}$) where the Q-factor peaks

for a given L_{ind}, S, W, and $R_{\square}$. The outer diameter of the inductors are estimated at each $D_{i,opt}$ points, and it is interesting that, for all cases, $D_{i,opt}$ are ~42% of the corresponding outer diameter. Contrary to the general belief, the Q-factor shows small percentage variations on the inner diameter, especially at higher inductances.

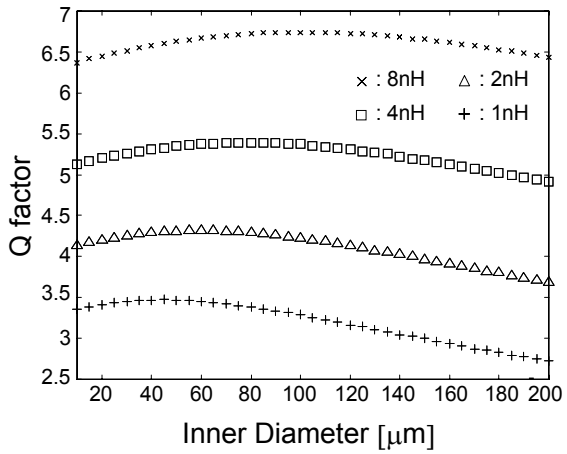

Fig. 4. The dependence of Q_{ind} on the inner-diameter D_i where $\omega = 2$ GHz, $S = 1$ μm, $W = 10$ μm, and $\rho_{sh} = 40$ mΩ/□.

CONCLUSIONS

A closed-form expression for the quality factor of the square spiral inductor is proposed as a function of the inductance, metal width, spacing, and inner diameter. Based on the Q-factor equation, the layout dependences are investigated. As a result, simple and clear guidelines for high-Q inductor design are suggested: minimize the metal spacing, maximize the metal width considering the area and the parasitic capacitances, and let the inner diameter be approximately 40% of the outer diameter. The metal width tends to dominate the Q-factor while the metal spacing and the inner diameter have minor effects.

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