A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-μm CMOS Technology

Trung-Kien Nguyen, *Student Member, IEEE*, Vladimir Krizhanovskii, Jeongseon Lee, Seok-Kyun Han, Sang-Gug Lee, *Member, IEEE*, Nae-Soo Kim, and Cheol-Sig Pyo

***Abstract*—This paper presents a low-power RF receiver/transmitter front-end for 2.4-GHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology. An RF receiver comprises a single-ended low-noise amplifier, a quadrature passive mixer, and a transimpedance amplifier. A current-mode passive mixer showing a very good $1/f$ noise performance is adopted to convert an RF signal directly to a baseband signal. Moreover, this type of passive mixer shows high-linearity performance, leading to overall RF receiver linearity improvement. A low-power, high-linearity transmitter front-end is implemented by using a passive mixer and two-stage driver amplifier in which the first stage is a conventional cascode amplifier and the second stage uses a folded cascode one. The receiver front-end achieves 30-dB voltage conversion gain, 7.3-dB noise figure with $1/f$ noise corner frequency of 70 kHz, -8-dBm input third-order intercept point, and $+40$-dBm input second-order intercept point. The transmitter front-end shows 12-dB power conversion gain, 0-dBm output power with 10-dBm output third-order intercept point, and -30-dB local-oscillator suppression. The receiver and transmitter front-end dissipate 3.5 and 3 mA from a 1.8-V supply, respectively.**

***Index Terms*—CMOS radio, dc offset, driver amplifier (DA), IEEE 802.15.4 transceiver, low-noise amplifier (LNA), low power, $1/f$ noise, passive mixer, transceiver front-end.**

I. Introduction

RECENTLY, the development of single-chip low-power CMOS transceivers for the 2.4-GHz band has been increasing significantly due to the demand of longer battery life and lower cost solutions for applications such as Bluetooth and IEEE 802.11b [1], [2]. In particular, with the introduction of the IEEE 802.15.4 standard [3], the demands for low cost and low power tend to dominate the transceiver developments. The IEEE 802.15.4 standard supports three operating frequency bands: 868-MHz band in European, 915-MHz band in America, and the 2.4-GHz band globally. The data rate of IEEE 802.15.4 varies from 20 to 250 kb/s depending on the operating frequency band. The applications of this standard are commercial, home automation, industrial, consumer electronics, personal health care, and game. These applications should operate from several months to a year on one button battery without changing.

There are several CMOS-based 2.4-GHz low-power receiver/transmitter implementations that have been reported in the last few years [4]–[9]. However, those works still dissipate quite high power consumption. Thus, it is desirable to achieve lower power dissipation. To deal with the aspect of low-power design, the most common solution is to employ a current reused technique [4]. Nevertheless, by going with the current reused technique, the linearity is limited due to the stack of several transistors.

This paper describes the design and implementation of low-power RF receiver/transmitters for 2.4-GHz-band IEEE 802.15.4 standard. With the main goal of low power, low $1/f$ noise, and high linearity receiver, the solution we are presenting is the use of a singled-ended low-power low-noise amplifier (LNA) followed by a quadrature passive mixer operating in the current mode [10]. In the transmitter chain, the low-power requirement is also taken into account by using a quadrature passive mixer and a single-ended two-stage driver amplifier (DA) in which the first stage is a conventional cascode topology and the second stage is a folded cascode one. This paper is organized as follows. Section II describes the proposed transceiver architecture, design considerations, and the radio specifications of the IEEE 802.15.4 standard. The RF receiver/transmitter circuit designs are explained in Section III. Section IV summarizes the experimental results of the implemented transceiver, and Section V concludes this study.

II. Transceiver Architecture, Design Considerations, and Specifications

In the typical wireless transceiver design, there are three common architectures: super-heterodyne, low-intermediate-frequency (low-IF), and direct conversion [11]. The super-heterodyne architecture is the most widely used architecture for the state-of-the-art transceivers in the modern handsets since this architecture is capable of providing high and stable performances [12], [13]. However, one of the main disadvantages in this architecture is the image problem. To solve this problem, normally, it is required to have off-chip surface acoustic wave (SAW) filters [13]. In addition, this architecture requires more than one mixer; consequently, it not only consumes more power but also makes the transceiver implementation more complicated. Undoubtedly, this architecture

Manuscript received February 11, 2006. This work was supported in part by the Development of Sensor Tag and Sensor Node Technology for RFID/USN Project of the Electronics and Telecommunications Research Institute through the IT Leading Research and Development Support Program of the Ministry of Information and Communication, Korea.

T.-K. Nguyen, V. Krizhanovskii, J. Lee, S.-K. Han, and S.-G. Lee are with the School of Engineering, Information and Communications University, Daejeon 305-714, Korea (e-mail: ntkienvn@icu.ac.kr).

N.-S. Kim and C.-S. Pyo are with the RFID/USN Research Group, Telematics and USN Research Division, Electronics and Telecommunications Research Institute, Daejeon 305-350, Korea.

Digital Object Identifier 10.1109/TMTT.2006.885556

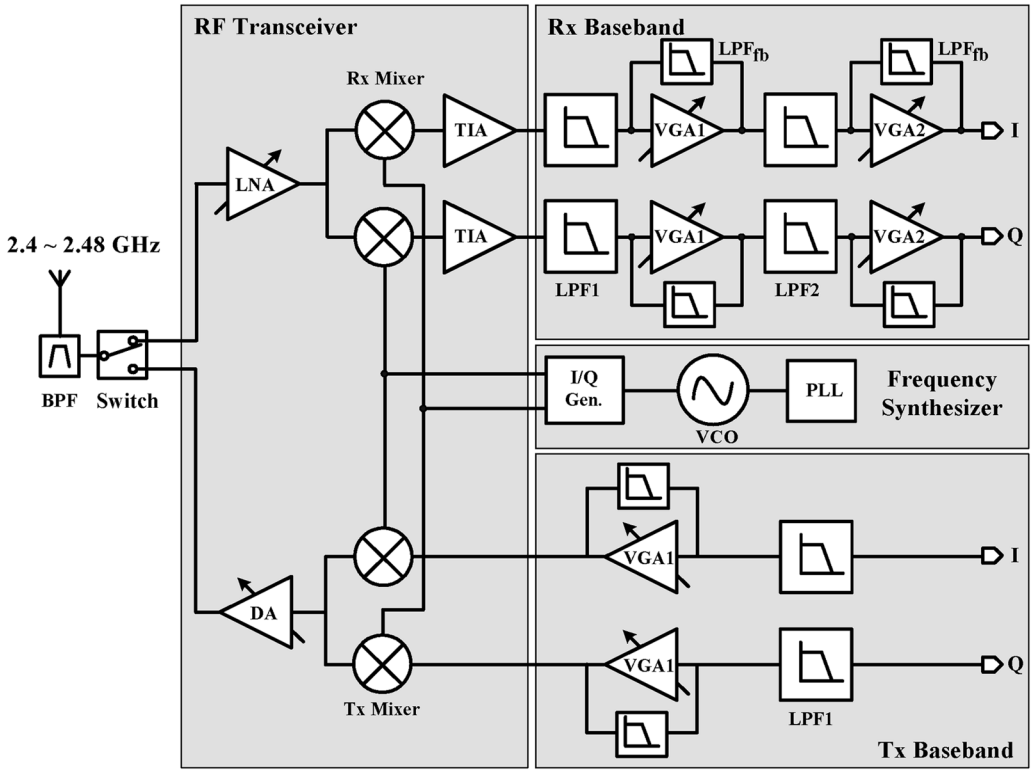

Fig. 1. Transceiver architecture.

is not suitable for low-power and low-cost applications. On the contrary, the direct-conversion architecture is very costly due to the high level of integration. In the direct-conversion architecture, the image rejection filter is not needed and the IF bandpass filter is replaced by the low-pass filter. However, this architecture has some disadvantages such as dc-offset, even- order distortion, flicker noise, I/Q mismatch, and LO leakage [14], [15]. Lately, an architecture called low-IF has been developed to avoid the drawbacks of the two architectures described above [16]. Nevertheless, the low-IF architecture still suffers from some issues such as a high analog-to-digital conversion (ADC) sampling rate and image rejection limitation due to the gain and phase mismatches [17] leading higher power consumption. In this design, considering a low-cost and low-power aspect, the direct-conversion architecture is chosen. The proposed transceiver architecture is shown in Fig. 1. As can be seen in Fig. 1, in the receiver chain, an RF incoming signal is amplified by an LNA and down-converted directly to baseband by a current-mode I/Q mixer. The current-mode mixer enhances the mixer linearity at low-power supply voltage and minimizes the noise contribution of the analog baseband simultaneously. Then, the current baseband signal after the downmixer is converted to the voltage signal by a transimpedance amplifier (TIA). At the baseband section, an alternative low-pass filter and variable gain amplifier (LPF-VGA) structure is adopted to obtain the optimum tradeoff performances under low power consumption [18]. In the transmitter chain, the baseband signal after a digital-to-analog converter (DAC) is filtered and amplified by the LPF and VGA. After that, the analog baseband signal is upconverted to the RF signal directly by an I/Q mixer and transferred to an antenna by an on-chip DA. In the frequency synthesizer block, a quadrature signal driving into an up/down mixer is obtained by using the conventional *LC* differential voltage-controlled oscillator (LC-VCO) operating at double the frequency of the incoming RF signal and the frequency divide-by-two circuit.

In this study, in order to go with the direct-conversion architecture, the following design aspects are taken into account.

- The dc-offset issue will be eliminated by using a feedback low-pass filter, $\mathrm{LPF_{fb}}$, acting as a feedback loop in the VGA stage, as can be seen in Fig. 1. The required cutoff frequency of the $\mathrm{LPF_{fb}}$ to meet the standard requirement will be explained later.
- The problem of $1/f$ noise can be minimized by both using a passive downconversion mixer and dc feedback loop which is used to cancel the dc-offset issue.
- Even-order distortion, which is mainly dominated by second-order distortion, is eliminated by using the double-balance downmixer, careful layout, and symmetric tracing of RF and local oscillator (LO) paths. Moreover, this issue is not as serious since the required $\mathrm{IIP_2}$ is relaxed.
- The I/Q mismatch problem can be solved by symmetric layout. In addition, the required error vector magnitude of the IEEE standard is not very high ($<35\%$); therefore, I/Q mismatch is not a critical issue.
- The issue of LO leakage can be eliminated by operating a VCO at double the frequency of the desired signal and then frequency divider. Using a cascode LNA and DA topology also helps to suppress this issue due to high input/output isolation.

TABLE I
SUMMARY OF TRANSCEIVER SPECIFICATIONS

Modules	Items	Specification
Rx	Sensitivity [dBm]	-85
	NF [dB]	< 15.5
	IIP3 [dBm]	> -32 @ high gain mode > -10 @ low gain mode
	IIP2 [dBm]	> 10.5
	Low pass filter	1.5 MHz, 3rd order Butterworth
	Gain control range [dB]	65
TX	Output power [dBm]	0
	$OP1_{dB}$ [dBm]	0
	OIP3 [dBm]	10
	Low pass filter	1.5 MHz, 2nd order Butterworth
	Total power gain [dB]	20
LO	Phase noise [dBc]	-102 dBc @ 3.5 MHz offset
	Power [dBm]	> 0

- In the case of the transmitter, thanks to the relatively high input signal level, the problems of dc-offset and flicker noise, which are the main obstacles in implementing a direct-conversion receiver, become less critical. Even so, the dc-offset needs to be minimized as it gives rise to LO feedthrough, which overlaps with the modulated carrier. In this architecture, again, the dc-offset is implemented inside the VGA by using a low-pass filtering feedback loop as it is implemented in the receiver chain.

The transceiver specifications such as noise figure (NF), nonlinearity, selectivity, and channel-selection LPF characteristic satisfying IEEE 802.15.4 standard were described in [19] and summarized in Table I. The required cutoff frequency of $\mathrm{LPF_{fb}}$ can be found by simulating the receiver BER performance with the number of cutoff frequency of $\mathrm{LPF_{fb}}$. As reported in [20], the corner frequency of $\mathrm{LPF_{fb}}$ can be chosen within 5% of the corner frequency of LPF, and the receiver needs only 1-dB gain more to obtain the same bit-error-rate (BER) performance. Consequently, the result of corner frequency of $\mathrm{LPF_{fb}}$ in this transceiver system is set to 75 kHz.

After the overall transceiver specifications are derived, the next step of the system-level design is to determine the specifications of the individual block in our transceiver system. As can be seen in Fig. 1, the proposed transceiver will be divided into five separate blocks: Rx-RF including LNA, downmixer, and TIA, Tx-RF consisting of upmixer and DA, Rx-Baseband, Tx-Baseband, and Frequency Synthesizer. These abbreviations will be used in the text of this study for convenience.

Normally, to determine the NF specifications of individual blocks in the cascade system, Friis's equation [21] will be used. According to the abbreviations in the proposed transceiver, we have [22]

$$\mathrm{NF_{total}} = \mathrm{NF_{Rx-RF},}_{R_S} + \frac{\mathrm{NF_{Rx-Baseband,R_{out,Rx-RF}}} - 1}{A_{P,\mathrm{Rx-RF}}} \tag{1}$$

TABLE II
SUMMARY OF RX-RF AND RX-BASEBAND SPECIFICATIONS

Parameters		Rx-RF	Rx-Baseband
Voltage Gain [dB]		30	-20 ~ 65
NF [dB]		8	20
IIP3 [dBm]	@ high gain mode	-12	-30
	@ high low mode	-8	10
IIP2 [dBm]		> 20	> 20
I/Q mismatch	Gain [dB]	< 2	< 2
	Phase [deg.]	< 2	< 2

TABLE III
SUMMARY OF TX-RF AND TX-BASEBAND SPECIFICATIONS

Parameters		Tx-RF	Tx-Baseband
Gain [dB]		10	-20 ~ 20
OP-1dB [dBm]		2	15
OIP3 [dBm]		10	12
OIP2 [dBm]		> 30	> 30
I/Q mismatch	Gain [dB]	< 2	< 2
	Phase [deg.]	< 2	< 2

where $\mathrm{NF_{Rx-RF}}$ and $A_{P,\mathrm{Rx-RF}}$ are the NF and the available power gain of the Rx-RF block, respectively. The available power gain of the Rx-RF block is given by

$$A_{P,\mathrm{Rx-RF}} = \left(\frac{R_{\mathrm{in,Rx-RF}}}{R_S + R_{\mathrm{in,Rx-RF}}}\right)^2 A^2_{v,\mathrm{Rx-RF}} \frac{R_S}{R_{\mathrm{out,Rx-RF}}} \tag{2}$$

where R_s is the source impedance, and R_{in}, R_{out}, and A_v are the input impedance, output impedance and voltage gain of the Rx-RF block, respectively.

To calculate the total input third-order intercept point, $\mathrm{IIP_3}$, the following expression is used [22]:

$$\frac{1}{A^2_{\mathrm{IIP3,total}}} \approx \frac{1}{A^2_{\mathrm{IIP3,Rx-RF}}} + \frac{A^2_{v,\mathrm{Rx-RF}}}{A^2_{\mathrm{IIP3,Rx-Baseband}}}. \tag{3}$$

As can be seen from (1) to (3), there are so many possible combinations of block specification that meet the requirements. A set of specifications are specified based on our experience and the experimental results of the last successful blocks. Then, during the design process, some of the values are revised based on the design experimental results. Therefore, the authors believe that the given specifications have reached a certain optimal point for low-power-consumption transceiver design. The final specifications of the individual block in the receiver chain are listed in Table II. Similarly, the specifications of the individual block in the transmitter chain are shown in Table III.

III. CIRCUITS DESIGNS

A. RF Receiver

The proposed RF receiver front-end is shown in Fig. 2, which consists of a single-ended LNA, a current-mode double-balance passive mixer, and a TIA. This configuration is chosen due to

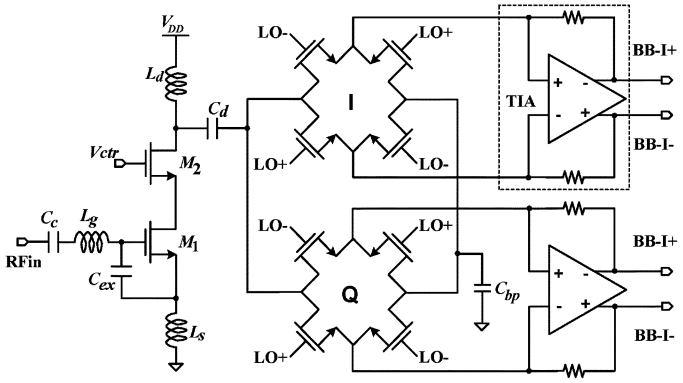

Fig. 2. Schematic of the RF receiver.

TABLE IV
LIST OF SYMBOLS

Symbols	Definition and Value
C_{gs}	Gate-source capacitor of transistor M_1
g_m	Transconductance of transistor M_1
V_{GS}	Gate-source voltage of transistor M_1
V_{DS}	Drain-source voltage of transistor M_1
ω_o	Operating frequency
ω_T	Cut-off frequency of M_1
δ	Constant, its value = 4/3 for long-channel devices
γ	Constant, its value = 2/3 for long-channel devices
c	Correlation coefficient between gate induced noise & channel noise, its value = 0.4 for long-channel devices

a number of reasons. A single-ended LNA dissipates lower dc current than a differential one. A passive mixer dissipates no dc current, therefore, the total power consumption of the receiver can be reduced. In addition, with the absence of dc current in the passive mixer, the $1/f$ noise contribution from the mixers can be neglected [23]. A double-balanced mixer is used to reduce the LO leakage. The single-ended LNA driving the double-balanced mixer can be used since the required input second-order intercept point (IIP_2) performance of the IEEE 802.15.4 standard is not as high compared with other wireless communications standards. As can be seen in Fig. 2, the output of the LNA is connected to one terminal of differential RF input of the mixer via coupling capacitor C_d, while the second input terminal of the mixer is connected to ac ground through the bypass capacitor C_{bp}. From simulation results, we have found that, by using this approach, only the overall conversion gain is reduced by 3 dB while maintaining most of the advantages of the differential circuitry such as the second-order distortion and the LO leakage.

1) LNA: The main goals of LNA are low noise figure, high gain to sufficiently reduce the input referred noise contribution of the subsequent stages, and high linearity to accommodate high input signal and strong interferences. In addition, LNA should have a 50-Ω input impedance to match with the output impedance of the off-chip components such as RF bandpass filter or T/R switch. Typically, an inductive degeneration cascode LNA topology is widely used since it provides high gain, low noise, wideband, and high input/output isolation [24], [25]. In this configuration, the inductive degeneration L_s is used to achieve simultaneous noise and input matching since L_s generates a real part at the input impedance. This is important because there is no real part in the input impedance without degeneration, while there is in the optimum noise impedance. Therefore, L_s helps to reduce the discrepancy between the real parts of the optimum noise impedance and the LNA input impedance. Furthermore, the imaginary part of the input impedance is changed by $j\omega L_s$, and this is followed by nearly the same change in the optimum noise impedance, especially with the advanced technology [26]. However, under low-power consumption, meaning low gate–source overdrive voltage or small transconductance g_m, the required L_s value that satisfies the simultaneous noise and input matching condition has to be very large. The problem is that, for the L_s to be greater than some value, the minimum noise figure $\mathrm{NF}_{\min}$ of a given technology can be increased significantly [27]. As a result, the minimum achievable NF of the LNA can be considerably higher than its $\mathrm{NF}_{\min}$, spoiling the idea of simultaneous noise and input matching. To overcome this problem, the proposed LNA topology shown in Fig. 2 is used [28]. As can be seen in Fig. 2, the proposed LNA differs by one additional capacitor C_{ex} compared to the conventional cascode LNA. The insertion of this capacitance adds a degree of freedom to play with to achieve a simultaneous noise and input matching at very low-power consumption. If the noise contributions of the cascode transistor and the Miller effect are assumed to be neglected, the noise figure of LNA at the operating frequency can be approximated by the following expressions, which are corrected in comparison with what has been reported in the original paper [26]:

$$F = 1 + \frac{1}{g_m^2 R_s} \cdot \left\{ \gamma g_{d0} \cdot \begin{Bmatrix} \left[1 + s^2 C_t (L_g + L_s)\left(1 + |c|\alpha\sqrt{\frac{\delta_{\mathrm{eff}}}{5\gamma}}\right)\right]^2 \\ -(sC_t R_s)^2 \left(1 + |c|\alpha\sqrt{\frac{\delta_{\mathrm{eff}}}{5\gamma}}\right)^2 \\ -\frac{\alpha\delta_{\mathrm{eff}}}{5}\left(1 - |c|^2\right) g_m (sC_t)^2 \left[R_s^2 - s^2 (L_g + L_s)^2\right] \end{Bmatrix} \right\} \tag{4}$$

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta\left(1 - |c|^2\right)} \tag{5}$$

$$Z_{\mathrm{opt}} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}\left(1 - |c|^2\right)} + j\left(\frac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{\mathrm{gs}} \left\{ \frac{\alpha^2\delta}{5\gamma}\left(1 - |c|^2\right) + \left(\frac{C_t}{C_{\mathrm{gs}}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2 \right\}} \tag{6}$$

$$R_n = \frac{\gamma}{\alpha} \cdot \frac{1}{g_m} \tag{7}$$

where $C_t = C_{\mathrm{gs}} + C_{\mathrm{ex}}$, $\delta_{\mathrm{eff}} = \delta \cdot (C_{\mathrm{gs}}^2 / C_t^2)$, and the other parameters are defined in Table IV.

From Fig. 2, the input impedance of the LNA is

$$Z_{\mathrm{in}} = s(L_s + L_g) + \frac{1}{sC_t} + \frac{g_m L_s}{C_t}. \tag{8}$$

One can see from (8) that, with the use of C_{ex}, the required L_s and L_g values that are used to fulfill the imaginary part of the input impedance can be reduced. Consequently, the NF of

the LNA is improved further since the parasitic resistance is reduced.

In this LNA design, the optimum size of an input transistor M_1 and the optimum values of inductive degeneration L_s, extra capacitor $C_{\rm ex}$, and the dc bias voltage of the M_1 are chosen based on the power-constrained simultaneous noise and input matching design technique as described in [26], while the gate inductor L_g is added to match the real value of input impedance to be 50 Ω. In this design, L_s is implemented by a wire bonding. To reduce the off-chip components, and since the required NF of the overall receiver is relaxed, L_g can be implemented by using an on-chip spiral inductor. In addition, by employing an on-chip L_g, it is easier for on-chip T/R switch integration. In Fig. 2, the loading inductor L_d is also implemented on-chip.

Under low power consumption, in order to accommodate a high input level, the LNA needs to have gain control function. In this LNA topology, the gain control function is implemented by adjusting the value of bias voltage of the cascode transistor $V_{\rm ctr}$. As the basic operating principle for CMOS transistor suggests, CMOS has high linearity with low gain in the linear region and low linearity with high gain in saturation region. When $V_{\rm ctr}$ is in a high-level state, two transistors M_1, M_2 remain in the deep saturation region, and high gain is obtained. Since the input signal is very small, the distortion is relatively low. On the contrary, when the input signal is high and $V_{\rm ctr}$ is in a low-level state, the input transistor M_1 stays in linear region and low gain with low distortion can be achieved [29].

In the simulation, the proposed LNA achieves NF of 3.0 dB, $\rm IIP_3$ of -8 dBm (at maximum gain), and power gain of 16 dB while consuming 1 mA from a supply voltage of 1.8 V. The NF of the LNA can be improved further by using the off-chip inductor L_g, which has higher quality factor in comparison with the on-chip one.

2) Downconversion Mixer: One may argue that a passive mixer dissipates no dc current and gives high linearity. In addition, the absence of dc current through the switches also makes it possible to eliminate the $1/f$ noise [23], which otherwise is a problem for direct-conversion receivers. Normally, nMOS transistors have better switch performance than do pMOS transistors thanks to the higher mobility of electrons than holes [30]. Therefore, in this design, nMOS is chosen. In this mixer, there are two parameters with which designers can play: the device size and the LO signal characteristics.

In order to have low noise performance, the width of the transistor should be sufficiently large to provide a sufficiently low on-resistance. However, when sizing the switches, there will be a tradeoff between the mixer noise performance and the gain of the LNA. The load impedance of the LNA consists of a parallel resonance circuit that is made up by the parasitic switch capacitance and the output inductor. If the switch capacitance is increased, the inductance must be decreased in order to not change the resonant frequency. The gain of the LNA will then decrease due to the lower load impedance. In this design, the optimum switching transistor's size is found to be 130/0.18 μm. The characteristics of the LO signal will affect the mixer performance [31]. The dc level of the LO signal is an important factor since it controls the switching mode. In the balanced drive case, the voltage conversion gain is theoretically equal to $2/\pi$. If the switches are set to have less on-time than off-time, which scenario is often referred to as break-before-make, the conversion gain will maximally equal to 1 [32], but the mixer will also be less linear. Thus, there will also be a tradeoff between the mixer conversion gain and the linearity. In order to eliminate $1/f$ noise, it is important that transistors are biased at the condition where there is no dc current flowing through the switch. In other words, the source and drain terminals are biased at $V_{\rm CM}$, while their gate voltage is

$$V_G = V_{\rm CM} + V_{\rm TH} \tag{9}$$

where $V_{\rm TH}$ is the threshold voltage of transistors. It has been found from simulation that, when V_G is around 1.43 V with $V_{\rm CM} = 900$ mV, this mixer shows $1/f$ noise-free operation.

The conversion gain and noise figure of the passive mixer can be improved by applying high LO amplitude. However, in this study, 0-dBm LO power is applied considering the measured results of the fabricated quadrature VCO.

To improve the linearity of the passive mixer, there exist two opposite opinions. In [31] and [32], the authors suggested using high-impedance loading for the passive mixer in order to decrease current flowing through the nonlinear drain–source resistance of the switching transistors in the on-state, thus decreasing nonlinear distortion and improving linearity. In this mode, the mixer operates as a voltage switch. Nevertheless, authors noticed that, as the amplitudes of the RF and downconverted signals grow, the voltage swing at RF and baseband ports starts to modulate the switching instances of the mixer, thus introducing additional distortion. Another approach, called the current-mode passive mixer, sought to eliminate this voltage swing by synthesizing low impedance at the output of the mixer [33], [34]. The reduction of the voltage swing at RF and baseband ports proved to be effective for linearity improvement. Therefore, the latter approach was selected for this design.

Assuming that a sinusoid is applied at the LNA input and the transconductance of LNA the is G_M, the current signal at the mixer input is given by [34]

$$i_{\rm RF}(t) = G_M v_{\rm RF} \sin(2\pi f_{\rm RF} t). \tag{10}$$

Also, assume that the voltage signal driving the mixer LO port is

$$v_{\rm LO}(t) = v_{LO} \sin(2\pi f_{\rm LO} t). \tag{11}$$

The switching function $S(t)$ produced by $v_{\rm LO}(t)$ applies to the RF signal current $(i_{\rm RF}(t))$ coming from the LNA is

$$S(t) = \frac{4}{\pi} \sum_{n=0}^{\infty} \frac{1}{2n+1} \sin\left[2(2n+1)\pi f_{\rm LO} t\right]. \tag{12}$$

The output current amplitude is given by [31]

$$i_{\rm IF}(t) = i_{\rm IF}(t) \sin(2\pi f_{\rm IF} t) = \frac{2}{\pi} G_M v_{\rm RF} \sin(2\pi f_{\rm IF} t). \tag{13}$$

This output current signal will be converted to the voltage signal by a TIA, which is the subject of Section III-A.3.

3) TIA: The architecture of the TIA is shown in Fig. 3. Low input impedance and the current-to-voltage conversion function of the first baseband stage are implemented by inclosing a

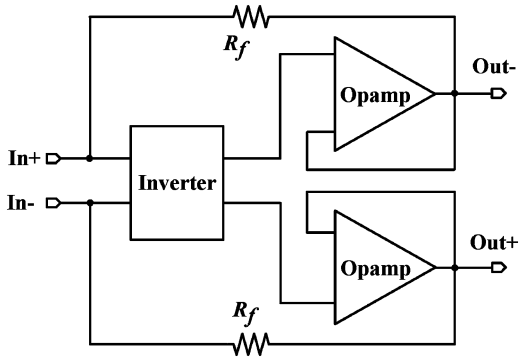

Fig. 3. Block diagram of the proposed TIA.

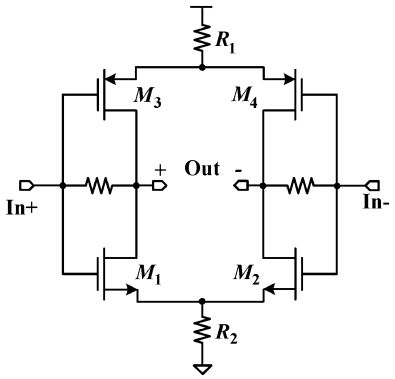

Fig. 4. Schematic of the inverter used in a TIA synthesizer system.

differential operational amplifier (Opamp) in shunt–shunt feedback. For TIA stability and sufficient loaded gain, an architecture with two stages, gain and buffer stages, was selected. The gain stage is a differential inverter composed of large devices in order to minimize flicker noise, as shown in Fig. 4. The self-biased inverter also sets the quiescent output voltage of the TIA and therefore biases the input of subsequent baseband stages, which should be used with the given front-end. The gain of the TIA is determined by the feedback resistance which is equal to 2 kΩ. Since the first stage is an inverter, the buffer has to be a noninverting amplifier. Also, the TIA must operate with equal input and output quiescent voltages. Thus, those voltage in turn were set to half of the supply voltage $\mathrm{V_{DD}}$ (here it is equal to 0.9 V) to maximize the voltage swing that the inverter and subsequent baseband circuits can handle. Under these conditions, and taking into account the requirements for the voltage swing, a simple source follower cannot be used as the buffer due to gate–source voltage V_{GS} level shift associated with it. An opamp in unity-gain feedback operates without level shifting and can, therefore, satisfy all of the requirements for the buffer.

For the opamp in unity-gain feedback, the requirement for output voltage swing automatically translates to the requirement of common-mode voltage swing. Therefore, opamps of a wide-common-mode-swing topology shown in Fig. 5 [35] were used as output buffers to prevent nonlinear distortions at a high input power levels. Implementing the buffers without a voltage-level shift allows alleviating voltage headroom constraint and maintaining a unified supply voltage of 1.8 V throughout the device, as opposed to similar front-end implementation in [33] and [34],

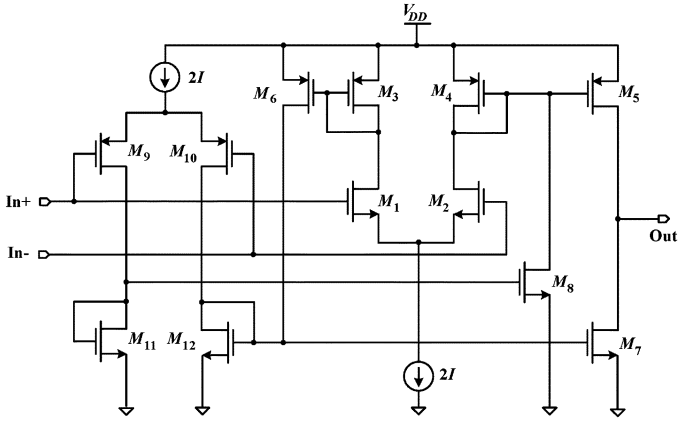

Fig. 5. Schematic of the operation amplifier used in the TIA.

where TIAs operate at a supply voltage of 2.5 V, which is higher than that of RF blocks.

The overall simulated NF of the receiver front-end is 6.3 dB at 2.5 MHz and 8.3 dB at 10 kHz. From simulation, it is found that the very low frequency noise (below the $1/f$ noise corner frequency) and the overall NF of the receiver front-end are significantly degraded by the TIA. The large increase receiver NF is due to the conversion loss of the passive mixer and the high NF of the TIA. To reduce NF contribution from the TIA, large-size MOS devices are adopted for the TIA. However, considering the 75-kHz corner frequency of the dc-offset feedback loop discussed in Section II, the transistor sizes are chosen for $1/f$ noise corner frequency of below 70 kHz.

B. RF Transmitter

The proposed transmitter front-end is shown in Fig. 6 which includes an I/Q upconversion mixer followed by a single-ended two-stage DA. To minimize the total power consumption of the transmitter front-end, a conventional passive mixer dissipating no dc current is adopted. Transmitter-wise, the mixer's linearity is one of the most critical parameters that need to be maximized. In this design, the size of the switches is chosen to be equal to that of the downconversion mixer for simplicity. To trade off the conversion gain against the linearity of the mixer, the switches are set to have balanced drive cases, meaning that switches have an equal amount of time in both the on and off states. In this design, switching size of 80/0.18 μm has been numerically optimized.

A DA consists of two stages: gain and output stages, as shown in Fig. 6. The gain stage uses a conventional inductive-load cascode topology with feedback resistor and a capacitor for stability, while the output stage is a folded-cascode one. The folded-cascode topology is chosen because it allows higher voltage headroom, thereby improving the linearity. As can be seen in Fig. 6, an additional capacitor C_2 is added between the first and second stages to boost the input voltage level. This can reduce the entire transmitter current consumption. In the second stage, the parasitic capacitances at node X can easily be eliminated by the adoption of inductor L_b to the supply voltage. The elimination or the reduction of these parasitic capacitances helps to avoid the signal loss into the silicon substrate, leading to higher power gain [36]. The linearity of the amplifier is

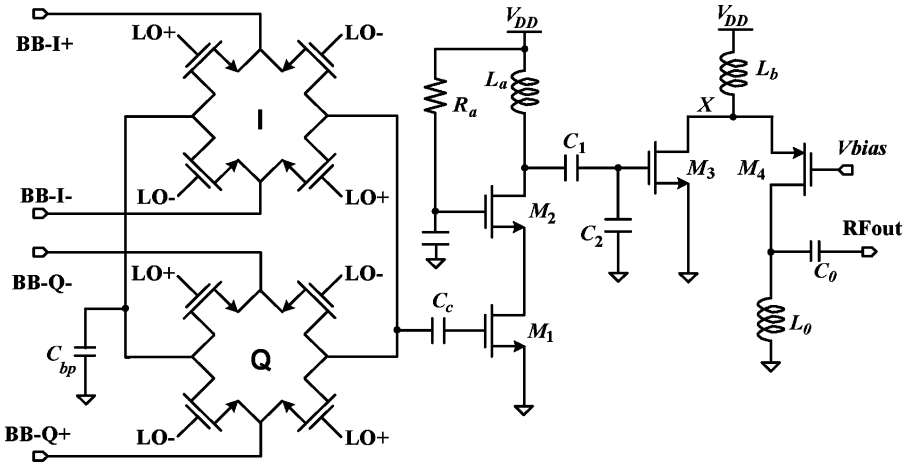

Fig. 6. Schematic of the RF transmitter.

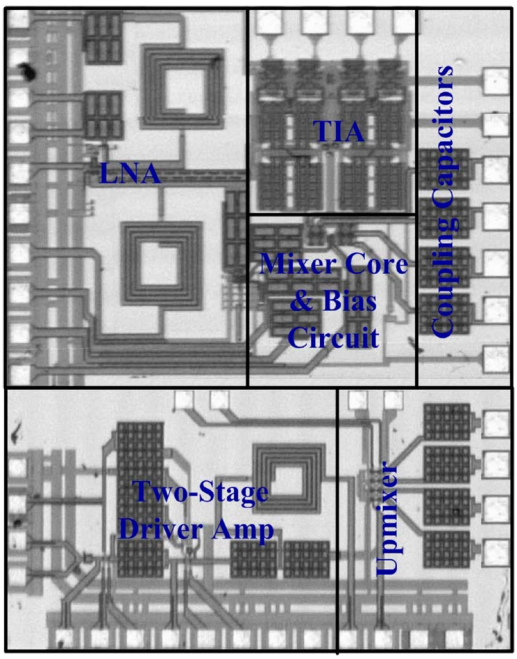

Fig. 7. Microphotograph of the proposed RF receiver/transmitter front-end. (Color version available online at http://ieeexplore.ieee.org.)

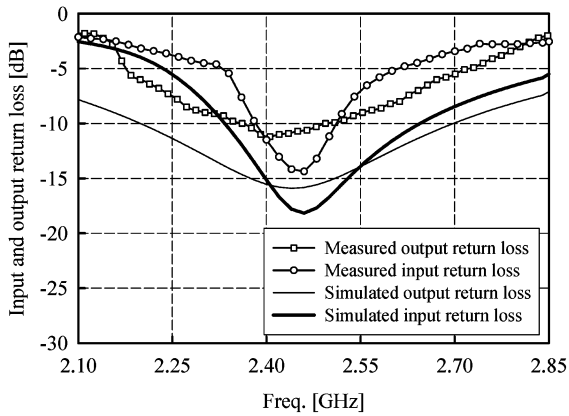

Fig. 8. Measured and simulated input return loss of the receiver and output return loss of transmitter front-end.

affected by the quality factor of the inductor [37]; therefore, L_b and L_o are implemented as off-chip inductors since they are located in the second stage, which dominates the linearity of the overall amplifier. Simulation results indicate that, with a bias current of 3 mA, the circuit can deliver 0 dBm to a 50-Ω load with an output third-order intercept point ($\mathrm{OIP_3}$) of 12 dBm.

IV. Experimental Results

The transceiver front-end with electrostatic discharge (ESD) protection is fabricated in a standard 0.18-μm CMOS technology. The microphotograph of the RF receiver and RF transmitter front-ends are shown in Fig. 7. Their die areas are 1.66 mm × 1.25 mm and 1.8 mm × 0.9 mm, respectively. The testing board has been built by directly bonding the die on a two-layer FR4 substrate. To supply differential signal at the input LO port, a commercial passive balun has been used, and 5 dB of balun loss according to its measurement has been de-embedded from the measurement. The receiver and transmitter dissipate 3.5 and 3 mA from a 1.8-V supply, respectively. Fig. 8 shows the simulated and measured input return loss of the receiver and output return loss of the transmitter front-end. From Fig. 8, it can be seen that the measured input and output return losses are lower than −14 and −10 dB, respectively. There is a considerable amount of discrepancy between the measurement and simulation, however, the overall shapes are within the reasonable amount of agreement. The discrepancy might be the result of the inaccurate modeling of the parasitic (e.g., on-chip, wire-bonding, and PCB board).The voltage-conversion gain variation of the receiver front-end sweeping the LO frequency across the entire target band (2.3–2.5 GHz) is also measured by varying V_{ctr} of the LNA shown in Fig. 2, and the obtained results indicate that the conversion gain is about 30 dB with a 10-dB variation and almost flat in the whole operating frequency band.

The receiver front-end NF was measured with the aid of a spectrum analyzer based on the method described in [38]. The measured and simulated NF of the front-end are shown in Fig. 9. The measurement shows about 7.3 dB with 70-kHz $1/f$ noise corner frequency. As can be seen in Fig. 9, the measured NF

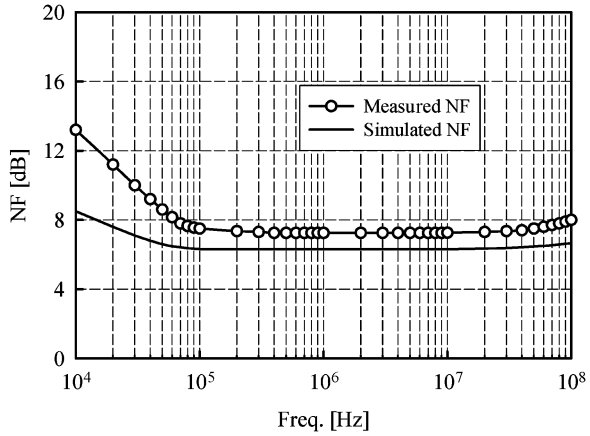

Fig. 9. Measured and simulated NF of the RF receiver front-end.

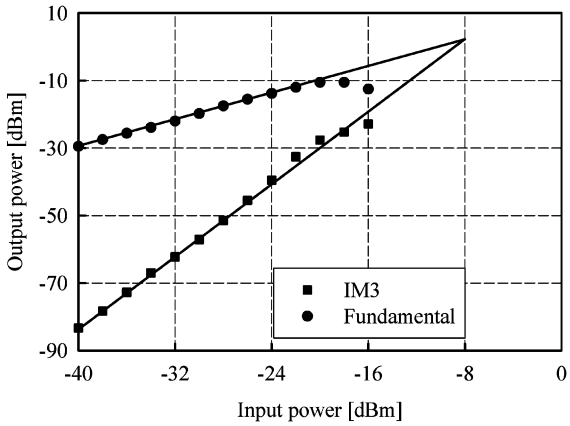

Fig. 10. Measured IIP_3 of the RF receiver front-end.

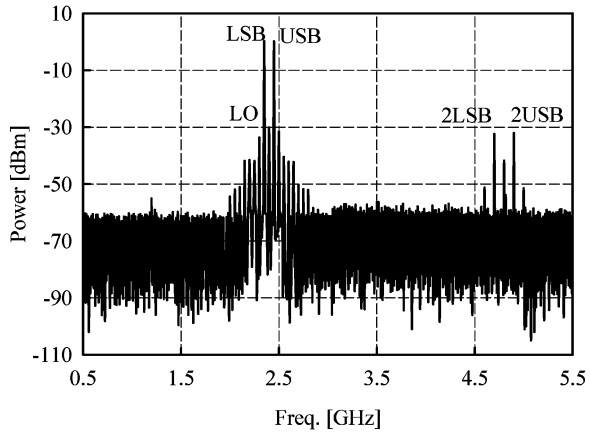

Fig. 11. Output spectrum of the RF transmitter front-end with −12-dBm input power.

is about 1 dB higher than that of the simulated NF. The discrepancy can be referred to the inaccuracies in the noise model (especially the $1/f$ noise) and the mixer noise analysis algorithm of the simulation tool. Other than that, the overall behavior of the NF is in good agreement with the simulation. Considering a 75-kHz cutoff frequency of the dc-offset loop, we can conclude that the receiver front-end achieves excellent noise performance. The receiver NF can be further improved by implementing the matching inductor L_g as an off-chip one

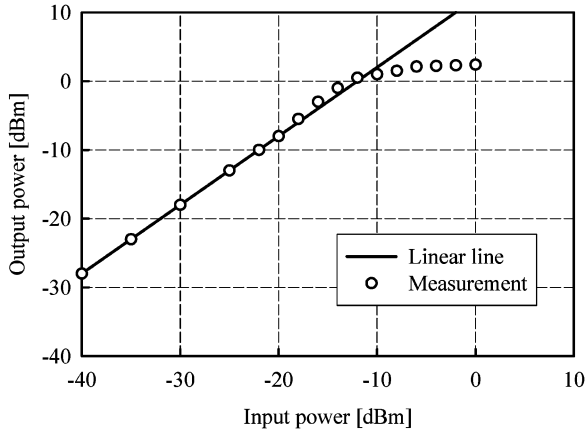

Fig. 12. Measured output 1-dB compression point of the RF transmitter front-end.

TABLE V
SUMMARY OF RX-RF AND TX-RF PERFORMANCES

Receiver Performance (RF = 2.405 GHz, LO = 2.4 GHz)	
Conversion gain @ 5 KΩ[dB]	30
Input return loss [dB]	-14
Gain variation [dB]	10
Noise figure [dB]	7.3
1/f noise corner frequency [kHz]	70
IIP3/IIP2 [dBm]	-8/40
Input P-1dB [dBm]	-18
LO-RF leakage [dB]	58
Power dissipation @ 1.8V [mW]	6.3
Die size [mm^2]	2.075
Transmitter Performance (BB = 50 MHz, LO = 2.4 GHz)	
Conversion gain [dB]	12
Output return loss [dB]	-10
Output 1-dB [dBm]	0
OIP3 [dBm]	10
LO leakage [dB]	30
Sideband rejection [dB]	30
Power dissipation @ 1.8V [mW]	5.4
Die size [mm^2]	1.62

because the lower parasitic resistance of an off-chip inductor will cause an improvement in the NF of the LNA and, thus, the receiver. Fig. 10 shows the measured IIP_3 result of the receiver front-end, which is about -8 dBm when a two-tone signal spaced by 500 kHz is applied. The other properties such as second-order input-referred intermodulation product IIP_2, input 1-dB compression point, and LO-RF leakage of the receiver front-end are also measured. The obtained results show -18-dBm input P-1 dB, 58-dB LO-RF leakage, and 40-dBm IIP_2.

Fig. 11 shows the measured transmitter front-end output spectrum when 50-MHz baseband signals with the power of -12 dBm and 0-dBm LO signal at 2.4 GHz are applied.

TABLE VI
PERFORMANCES COMPARISON

Module	Parameters	[4]	[5]	[6]	[7]	**This work**
Rx-RF	Technology CMOS [μm]	0.25	0.18	0.18	0.13	0.18
	Voltage conversion gain [dB]	50	30	21.4	14.5	30
	NF [dB]	6	NA	13.9	24.5	7.3
	IIP3 [dBm]	NA	-4	-18	-21	-8
	IIP2 [dBm]	NA	NA	NA	18	40
	Power dissipation, LNA+Mixer [mW]	6.25	5.4	6.5	1.68	1.8
	Architecture	SHD	Low-IF	Low-IF	DCR	DCR
Tx-RF	Parameters	[4]	[5]	[8]	[9]	**This work**
	Technology CMOS [μm]	0.25	0.18	0.18	0.18	0.18
	Output power [dBm]	0	0	-4	0	0
	Power dissipation, Mixer+DA [mW]	12	18	17	25*	5.4
	Architecture	SHD	DCT	DCT	DCT	DCT

SHD: Superheterodyne
DCR: Direct conversion receiver
DCT: Direct conversion transmitter
* Include DLL

As can be seen in Fig. 11, the measured result shows 12-dB power conversion gain, 30-dB LO suppression, and 30-dB other unwanted signal suppression. Although the low sideband signal still appears in Fig. 11 it can be removed when the input I and Q signals are applied. Fig. 12 shows the measured output 1-dB compression point of 0 dBm for the transmitter front-end at its highest gain mode. A two-tone test measurement of the RF transmitter shows +10-dBm (OIP_3). The obtained measurement results satisfy the IEEE 802.15.4 standard requirement specified in Section II. The overall performances of the transceiver are summarized in Table V. The comparison of the results in this study with those of other works is given in Table VI. As can be seen in Table VI, this work has low power dissipation while still achieving relatively good performances compared with the others.

V. CONCLUSION

A low-power and low-cost RF receiver/transmitter front-end for the IEEE 802.15.4 standard is reported and fabricated in a 0.18-μm CMOS technology. The RF receiver and transmitter with 2-mm^2 and 1.62-mm^2 die size consume 3.5 mA in receiver mode and 3 mA in transmitter mode under a supply voltage of 1.8 V. The RF receiver/transmitter front-ends employ direct-conversion architecture. To achieve a simultaneous noise and input matching, the conventional inductive degeneration cascode amplifier with an extra gate–source capacitor is implemented. With the main goal of low power and low-$1/f$ noise, a current-mode passive mixer dissipating no dc current and showing very good $1/f$ noise performance is adopted to convert the RF signal directly to a baseband signal. In the transmitter chain, a low-power consumption concept is also taken into account with the adoption of a passive mixer and a single-ended two-stage DA. The receiver shows 30-dB conversion gain with 10-dB gain variation, 7.3-dB noise figure, with $1/f$ noise corner frequency of 70 kHz. In the transmitter chain, 0-dBm transmit power and 10-dBm OIP_3 were obtained.

REFERENCES

[1] B. Razavi, "A low-power 2.4-GHz receiver CMOS for 802.11b," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 176–183, Feb. 2003.

[2] H. Darabi, S. Khorram, H.-M. Chien, M.-A. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, and A. Rofougaran, "A 2.4-GHz CMOS transceiver for Bluetooth," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2016–2024, Dec. 2001.

[3] *Low Rate Wireless Personal Area Networks*, IEEE P802.15.4/D18, Jan. 2005, draft standard.

[4] A. Zolfaghari and B. Razavi, "A low-power 2.4-GHz transmitter/receiver CMOS IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 176–183, Feb. 2003.

[5] P. Choi, H. C. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. K. Park, and K. Lee, "An experimental coin-size radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4 GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[6] F. Beffa, R. Vogt, W. Bachtold, E. Zellweger, and U. Lott, "A 6.5-mW receiver front-end for Bluetooth in 0.18 μm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2002, vol. 1, pp. 501–504.

[7] J. A. M. Jarvinen, J. Kaukovuori, J. Ryynanen, J. Jussila , K. Kivekas, M. Honkanen, and K. A. I. Halonen, "2.4 GHz receiver for sensor applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1426–1433, Jul. 2005.

[8] S. Kim, I. Nam, T. Kim, K. Kang, and K. Lee, "A single-chip 2.4 GHz low-power CMOS receiver and transmiter for WPAN applications," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2003, pp. 163–166.

[9] S. Byun, C.-H. Park, Y. Song, S. Wang, C. S. G. Conroy, and B. Kim, "A low power CMOS Bluetooth RF transceiver with a digital offset canceling DLL-based GFSK demodulator," *IEEE, J. Solid-State Circuits*, vol. 39, no. 10, pp. 1609–1618, Oct. 2004.

[10] K. Vladimir, T.-K. Nguyen, S.-G. Lee, and J.-C. Choi, "A direct conversion CMOS front-end for 2.4 GHz band of IEEE 802.15.4 standard," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2005, pp. 449–451.

[11] J. Crols and M. S. J. Steyaert, *CMOS Wireless Transceiver Design*. Boston, MA: Kluwer, 1997.

[12] B. Razavi, "Challenges in portable RF transceiver design," *IEEE Circuits Devices Mag.*, vol. 12, no. 12, pp. 12–25, Dec. 1996.

[13] T. H. Lee, "5-GHz CMOS wireless LANs," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 268–280, Jan. 2002.

[14] A. A. Abidi, "Direct conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec. 1995.
[15] B. Razavi, "Design considerations for direct conversion receivers," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 44, no. 6, pp. 428–435, Jun. 1997.
[16] J. Crols and M. S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1483–11492, Dec. 1995.
[17] S. Mirabbasi and K. Martin, "Classical and modern receiver architecture," *IEEE Commun. Mag.*, vol. 38, no. 11, pp. 132–139, Nov. 2000.
[18] M. Lee, I. Kwon, and K. Lee, "An integrated low power CMOS baseband analog design for direct conversion receiver," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2004, pp. 79–82.
[19] N.-J. Oh and S.-G. Lee, "Building A 2.4-GHz radio transceiver using IEEE 802.15.4," *IEEE Circuits Devices Mag.*, vol. 43, no. 6, pp. 43–51, Nov./Dec. 2005.
[20] N.-J. Oh, S.-G. Lee, and J. Ko, "A CMOS 868/915 MHz direct conversion ZigBee single-chip radio," *IEEE Commun. Mag.*, vol. 43, no. 12, pp. 100–109, Dec. 2005.
[21] H. T. Friis, "Noise figures of radio receivers," *Proc. IRE*, vol. 32, no. 7, pp. 419–422, Jul. 1944.
[22] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.
[23] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[24] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–758, May 1997.
[25] S. P. Voinigescu, M. C. Maliepaard, J. L. Showell, G. E. Babcock, D. Marchesan, M. Schroter, P. Schvan, and D. L. Harame, "A scalable high-frequency noise model for bipolar transistors with application optimal transistor sizing for low-noise amplifier design," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1430–1439, Sep. 1997.
[26] T.-K. Nguyen, C.-H Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.
[27] J. K. Goo, H.-T. Ahn, D. J. Ladwig, Z. Yu, T. H. Lee, and R. Dutton, "A noise optimization technique for integrated low noise amplifiers," *IEEE J. Solid-Stage Circuits*, vol. 37, no. 8, pp. 994–1002, Aug. 2002.
[28] P. Andreani *et al.*, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 9, pp. 835–841, Sep. 2001.
[29] W. C. Song, C. J. Oh, G. H. Cho, and H. B. Jung, "High frequency/high dynamic range CMOS VGA," *Electron. Lett.*, vol. 36, pp. 1096–1098, Jun. 2000.
[30] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.
[31] A. R. Shahani, D. K. Shaeffer, and T. H. Lee, "A 12 mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-Stage Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.
[32] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*. Boston, MA: Kluwer, 1999.
[33] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz $1/f$ corner direct conversion CMOS receiver," in *Proc. IEEE Custom Integrated Circuit Conf.*, Sep. 2003, pp. 459–462.
[34] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz $1/f$ noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.
[35] R. J. Baker, *CMOS, Circuit Design, Layout, and Simulation*, 2nd ed. New York: IEEE Press/Wiley-Interscience, 2005.
[36] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5 GHz CMOS wireless LAN receiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.
[37] J.-P. Kim, S.-S. Park, and S.-G Lee, "Linearity vs Q-factor of loads for RF amplifiers," *Microw. Opt. Technol. Lett.*, vol. 37, pp. 286–288, May 2003.
[38] National Instruments, Development Library [Online]. Available: http://zone.ni.com/devzone/conceptd.nsf/webmain/78A610B94390680486256D0B005403E8

Trung-Kien Nguyen (S'04), photograph and biography not available at time of publication.

Vladimir Krizhanovskii, photograph and biography not available at time of publication.

Jeongseon Lee, photograph and biography not available at time of publication.

Seok-Kyun Han, photograph and biography not available at time of publication.

Sang-Gug Lee (M'04), photograph and biography not available at time of publication.

Nae-Soo Kim, photograph and biography not available at time of publication.

Cheol-Sig Pyo, photograph and biography not available at time of publication.