A CMOS Multi-LO Frequency Synthesizer Block for MB-OFDM UWB systems

Chang-Wan Kim, Bong-Hyuk Park, Seung-Sik Lee, Sang-Sung Choi, and *Sang-Gug Lee

Electronics and Telecommunications Research Institute (ETRI)
161 Gajeong-dong, Yuseong-gu, Daejeon, 305-700, Korea
Tel: +82-42-860-6624, E-mail: cwkim@etri.re.kr
*School of Engineering, Information and Communications University (ICU),
119 Munjiro, Yuseong-gu, Daejeon, 305-714, KOREA

***Abstract*—A multi-LO frequency synthesizer block for MB-OFDM UWB systems is proposed, which is implemented in 0.18 μm CMOS technology. The proposed frequency synthesizer can provide three LO tones and quadrature IF LO tone from only one VCO. Based on an optimized frequency plan, it uses fewest nonlinear components like divide-by-N and mixer to suppress unwanted spurious tones. Its measured in-band sideband suppression ratio is more than 30 dBc for three sub-bands and it consumes only 17.6 mA from a 1.8 V supply.**

***Index Terms*—CMOS, RFIC, mixer, UWB, and frequency synthesizer.**

I. INTRODUCTION

RECENTLY, the interest in the Ultra-wideband (UWB) systems for short-range and high-rate data communication applications has been significantly increased, though the international standard has not been finalized; DS-CDMA (Direct sequence code division multiple access) and MB-OFDM (multi-band orthogonal frequency division multiplexing) approach [1]. The MB-OFDM approach divides the full 7.5 GHz UWB band (3.1 ~ 10.6 GHz) into fourteen sub-bands with its bandwidth of 528 MHz. With adoption of fourteen sub-bands, the MB-OFDM approach can increase the flexibility of spectrum and friendly comply with other wireless systems like 802.11a/b/g. However, MB-OFDM UWB transceivers needs a unique frequency synthesizer, which is required to provide multi-LO tones. Performances of frequency synthesizers for MB-OFDM UWB systems strongly depend on its frequency plan and architecture [2]-[6]. One or two PLL approaches [2]-[5] use divide-by-Ns and single-side-band (SSB) mixers to generate multi-LO tones from one VCO. One major technical issue in this scheme is unwanted spurious tones generated from non-linear components like divide-by-Ns and SSB mixers. Other approach [6] uses three PLLs to provide three LO tones, where each VCO oscillates at three different LO frequency respectively. For above both approaches [2]-[6], however, the sideband suppression requirement is very strict for MB-OFDM UWB systems, due to its wideband characteristics. Fig. 1 shows spurious requirements for the MB-OFDM UWB frequency synthesizer [2]. Based on [2], for the direct-conversion frequency synthesizer, the sideband suppression ratio for in-band frequencies is required to be more than 30 dBc. In addition, to allow co-existence with other wireless systems 2.4 and 5 GHz WLAN, out-of-band spurs at 2.4 and 5 GHz frequencies from the synthesizer also must be below 45 dB and 50 dB compared to the wanted LO tone,

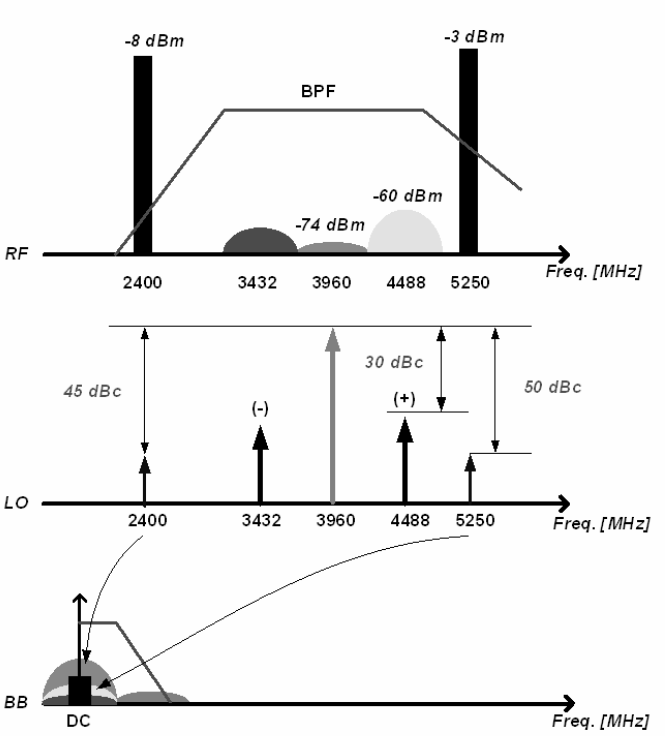


Fig. 1. Spurious requirement in the MB-OFDM UWB frequency synthesizers for the direct-conversion architecture.

respectively. However, these strict requirements can be mitigated with an optimized frequency plan and architecture.

This paper proposes architecture of frequency synthesizer and also reports its implementation results. The proposed frequency synthesizer is designed for the dual-conversion receiver, which can provide three differential LOs and one pair of quadratrue LO signal. Based on an optimized frequency plan, it adopts fewest nonlinear components like divide-by-N and mixer to suppress unwanted spurious tones.

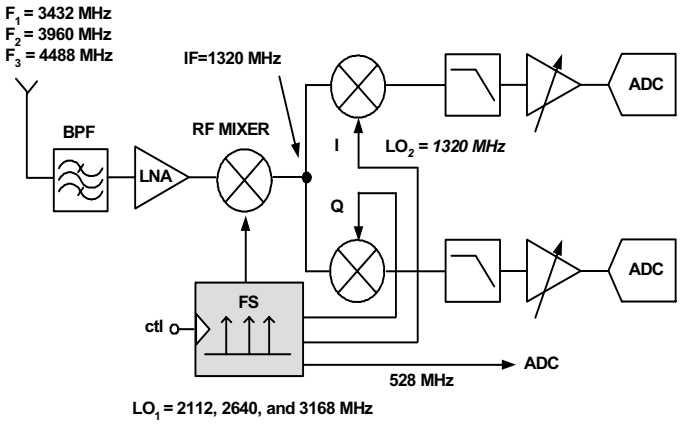


Fig.2. Proposed dual-conversion architecture for the MB-OFDM UWB receiver.

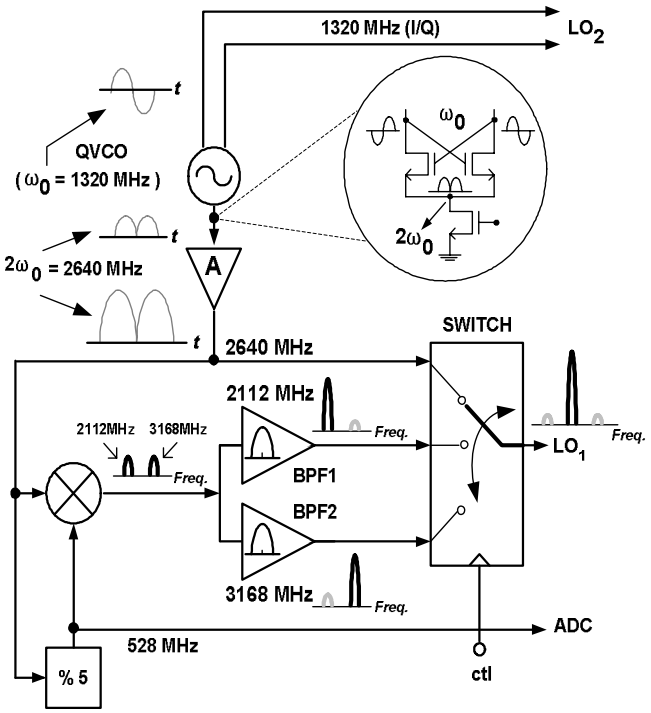


Fig. 3. Simplified block diagram of the proposed frequency synthesizer.

II. Architecture

MB-OFDM UWB transceivers can be implemented as the direct-conversion or the heterodyne architecture. The direct-conversion architecture can remove off-chip IF filters, so that all circuits can be intensively integrated on the silicon chip. However, its inherent problems (DC offset, I/Q mismatch, and so on) must be solved. In addition, the frequency synthesizer for the MB-OFDM UWB must provide exact I/Q LO tones at high frequencies to prevent cross-talk between the two bit streams [7]. The heterodyne architecture can overcome these disadvantages of the direct-conversion. In addition, the frequency synthesizer for the heterodyne architecture does not need I/Q LO signals, leading to its simple architecture. The image problem in the heterodyne can be solved with adoption of image rejection filters in the receiver signal path.

Fig. 2 shows the proposed dual-conversion architecture for the MB-OFDM UWB receiver, which is focused on the mandatory mode (frequency band: 3432, 3960, and 4488 MHz) [1]. As can be seen in Fig. 2, incoming RF signals (3432, 3960, and 4488 MHz) from the UWB antenna are first downconverted by the RF mixer to the IF of 1320 MHz, and then downconversion to DC. The selection of the IF frequency is carefully decided in this work, considering both image problem and architecture of the frequency synthesizer. From the IF of 1320 MHz, all image frequencies (528 ~ 2112 MHz) for LO_1 (2112, 2640, and 3168 MHz) can be located at out-of-band of BPF, removing additional image rejection filter and multi-LO tones in the frequency synthesizer can be synthesized from only one VCO. Thus, the frequency synthesizer in Fig. 2 can be designed with low power, due to its simpler architecture than those of direct-conversion receiver [2]-[5]. The frequency synthesizer in Fig. 2 does not need to generate quadrature LO_1 tones but just differential form, so that some burden of I/Q mismatch at high frequency are considerably mitigated. Moreover, it just generates only one pair of I/Q IF signal (LO_2), improving I/Q matching in the receiver signal path.

III. Frequency Synthesizer

The block diagram of the proposed frequency synthesizer for the double-conversion UWB receiver is shown in Fig. 3, which supports three RF sub-bands of 3432, 3960, and 4488 MHz (the mandatory mode). As can be seen in Fig. 3, three LO_1 signals (2112, 2640, and 3168 MHz) are oriented from the 2nd-order harmonic (2640 MHz) at common-source node of the 1320 MHz QVCO. The 2nd-order harmonic signal 2640 MHz is amplified and directly applied to the input of the switch circuit. The 2112 MHz and 3168 MHz signals are synthesized from 2640 MHz using a divide-by-five and a passive mixer, respectively. The 2112 and 3168 MHz signals at the output of the passive mixer simultaneously are filtered and amplified by BPF1 and BPF2, respectively. BPF1 and BPF2 are two-stage differential pairs with LC-tank loads, and the center frequency of the BPF1(2) is 2112 MHz (3168 MHz). The 1 GHz distance

between 2112 and 3168 MHz permits the adoption of LC-BPFs in this work. The isolation between 2112 MHz and 3168 MHz signals strongly depends on the quality factor (Q) of the on-chip BPFs. As can been in Fig. 6, to suppress inductive coupling between two on-chip BPFs, two on-chip BPFs are separated and layout in the opposite direction. Finally, one of three LO_1 signals is selected by the switch circuit and provided to the gate nodes of switching transistors of the RF mixer in Fig. 2. In Fig. 3, quadrature 1320 MHz LO_2 for the quadrature IF mixer is directly provided from the output of the QVCO.

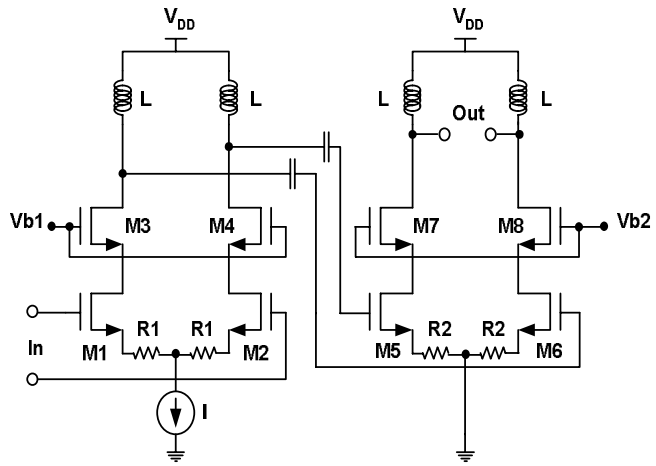


Fig. 4. Schematic of the two-stage BPF1 centered at 2112 MHz.

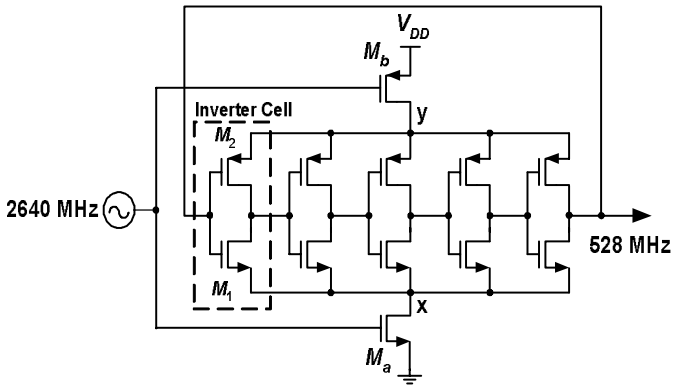


Fig. 5. Schematic of the divde-by-five.

Fig. 4 shows simplified schematic of the on-chip BPF1 centered at 2112 MHz, which is a two-stage differential pair with LC-tank loads. The BPF2 is same to the BPF1 with exception of load inductance values. For input signals at 2112 and 3168 MHz generated from a passive mixer, the on-chip BPF1 gives high impedance for 2112 MHz but lower impedance for 3168 MHz input signal. In Fig. 4, to provide undistorted output voltage swing for the RF mixer, differential pairs adopt the resistive degeneration technique, and the common-source node of the 2nd-stage amplifier is directly connected to the ground. The quality factor of the on-chip spiral inductor used in the BPF1s is about 12 at 2 GHz. Cascoded transistors (M_3, M_4, M_7, and M_8) are used to improve isolation between input and output of the BPF1.

Fig. 5 shows the divide-by-five circuit, modified from [8], which is a ring oscillator-based injection-locked frequency divider (ILFD). This ILFD, which consists of five inverter-based (M_1 and M_2) delay cells, consumes less DC power and chip area compared to other dividers using the LC-tank circuit. To increase injection efficiency, the 2640 MHz signal from the QVCO is simultaneously injected into nodes X and Y through the current sources M_a and M_b.

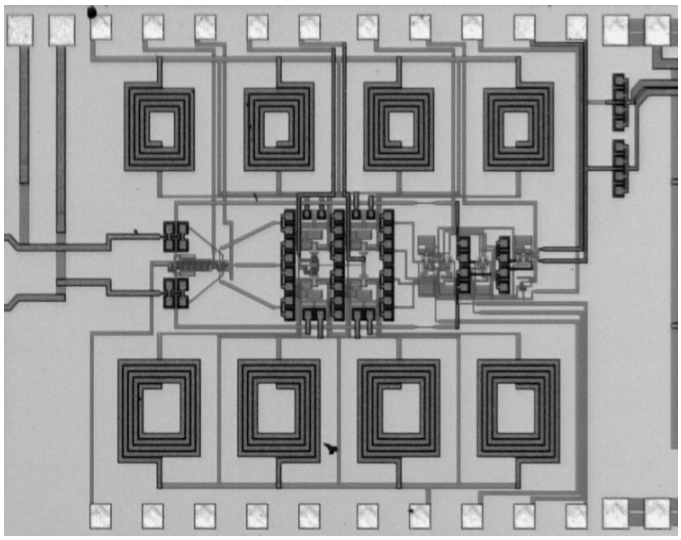


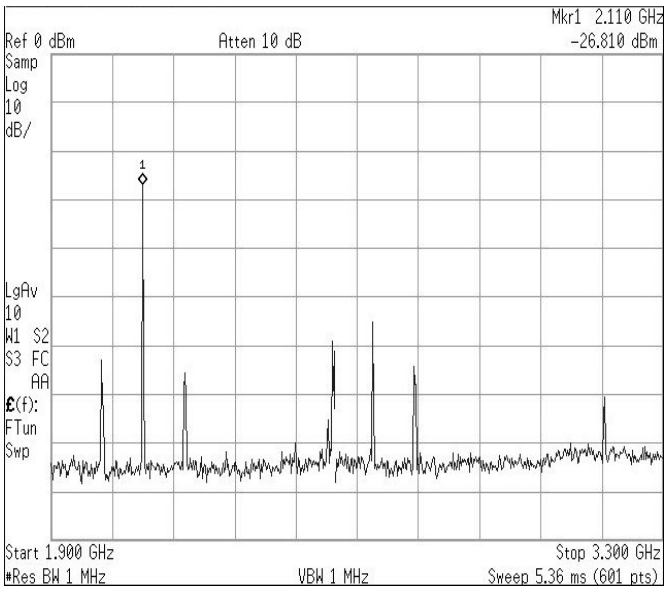
Fig. 6. Photograph of the proposed frequency synthesizer (the chip area is 0.9 X 1.1 mm^2).

IV. Measurement Results

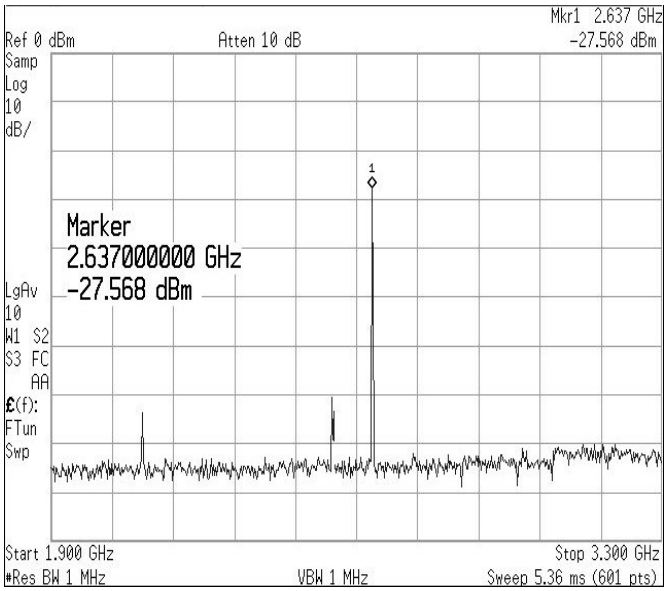
The proposed frequency synthesizer is implemented in 0.18 μm CMOS technology. It consumes 17.6 mA from a 1.8 V supply voltage. Its chip micrographic is shown in Fig. 6 and the die area with pads is 0.9 x 1.1 mm^2. In Fig. 6, a divide-by-five, a passive mixer, a switch circuit, and two LC-BPFs are integrated in this work to evaluate its feasibility. The 1320 MHz QVCO is separately implemented and not included and the 2640 MHz LO signal is externally provided for the evaluation.

Fig. 7 shows measured output spectrums from the frequency synthesizer for 2112 and 2640 MHz LO tones, respectively. The 3168 MHz spectrum shows very similar that of 2112 MHz LO tone. As can be seen in Fig. 7, the measured in-band sideband suppression ratio is 30 dBc for 2112 MHz and 42 dBc for 2640 MHz. These measured values well satisfy the MB-OFDM UWB requirement. The measured in-band sideband suppression ratio is coming from the quality factor (Q) of the on-chip BPFs and isolation characteristics of the switch. In the future, the adoption of advanced on-chip spiral inductors with high Q can more improve the sideband suppression ratio. Especially, unlike the direct-conversion as can be seen in Fig. 1, some spurious at 2.4 GHz and 5.25 GHz bands generated from the fabricated frequency synthesizer can not access with out-of-band strong

interferers in 802.11a/b/g bands in the double-conversion architecture. Accordingly, the requirement of the sideband suppression ratio for out-of-band is considerably alleviated and only in-band sideband suppression requirement is important factor in the proposed frequency synthesizer.



(a)



(b)

Fig. 7. Output spectrum of the frequency synthesizer: (a) 2112 MHz and (b) 2640 MHz.

V. Conclusions

A frequency synthesizer for MB-OFDM systems is proposed, which is implemented in 0.18 µm CMOS technology. With careful frequency planning in the dual-conversion architecture, the proposed frequency synthesizer can be simply implemented with fewest nonlinear components. Its measured sideband suppression ratio is more than 30 dBc for three sub-bands and well satisfies the MB-OFDM requirement. It consumes only 17.4 mA from a 1.8 V supply.

References

[1] http://www.ieee802.org/15/pub/TG3a.html.

[2] D. Leenaerts et al., "A SiGe BiCMOS 1ns fast hopping frequency synthesizer for UWB Radio," *ISSCC Dig. Tech. Papers*, 6-10 Feb. 2005, pp.202-203.

[3] A. Ismail and A. Abidi, "A 3.1 to 8.2 GHz direct conversion Receiver for MB-OFDM UWB transceiver," *ISSCC Dig. Tech. Papers*, 6-10 Feb. 2005, pp.208-209.

[4] Jri Lee, Da-Wei Chiu, "A 7-band 3-8 GHz frequency synthesizer with 1ns band-switching time in 0.18um CMOS technology," *ISSCC Dig. Tech. Papers*, 6-10 Feb. 2005, pp.204-205.

[5] Chien-chih Lin, Chorng-Kuang Wang, "A Regenerative semi-dynamic frequency divider for mode-1 MB-OFDM UWB hopping carrier generation," *ISSCC Dig. Tech. Papers*, 6-10 Feb. 2005, pp.206-207.

[6] Behzad Razavi et al., "A 0.13 µm CMOS UWB Transceiver," *ISSCC Dig. Tech. Papers*, 6-10 Feb. 2005, pp.216-217.

[7] Behzad Razavi, RF Microelectronics, Prentice Hall PTR, 1998.

[8] Wei-Zen Chen and Chien-Liang Kuo, "18 GHz and 7 GHz superharmonic injection-locked dividers in 0.25 µm CMOS technology," *Proceedings of the 2002 European Solid-State Circuits Conference*, Sep. 2002, pp.89-92.