A 2.2-mW Backgate Coupled LC Quadrature VCO With Current Reused Structure

Jong-Phil Hong, Seok-Ju Yun, Nam-Jin Oh, and Sang-Gug Lee

***Abstract*—This letter presents a backgate coupled quadrature voltage-controlled oscillator (QVCO) which consists of a pair of current reused LC-VCOs. The proposed QVCO is designed for 2-GHz operation based on a 0.18-μm triple-well CMOS technology. Measurements show -102 and -124 dBc/Hz at 100-kHz and 1-MHz offset, respectively. Compared to the conventional QVCO, the proposed QVCO dissipates significantly lower power (1.74 mA from a 1.25-V supply) while showing good $1/f^3$ close-in phase noise.**

***Index Terms*—CMOS, low power, quadrature voltage-controlled oscillator (QVCO), radio frequency (RF).**

I. Introduction

SINCE many of the current wireless communication standards require quadrature modulation, several circuit techniques have been developed to obtain in-phase (I) and quadrature-phase (Q) signals from a local oscillator (LO) [1], [2]. The quadrature signals can be generated from a master-slave flip-flop (divide-by-two circuit) or by quadrature-coupling of two LC-tuned differential VCOs. The flip-flop based quadrature generation circuit has the disadvantages of additional phase noise degradation, poor high frequency operation, and additional power dissipation. Quadrature-coupling based quadrature VCOs (QVCOs) tend to dissipate more power than that of the flip-flop based. As a low power implementation of a QVCO, Kim [3] proposed a backgate-coupled QVCO which couples the two LC-tank VCOs through the backgates of the switching transistors.

This letter reports a QVCO that can achieve better phase noise and lower power dissipation by combining the backgate coupling principle and current-reused VCO structure [4].

II. QVCO Design

Fig. 1(a) shows the conventional parallel-coupled QVCO (P-QVCO) where the I and Q signals are generated by coupling two differential VCOs through coupling transistors M_{cpl} in parallel with switching transistors M_{sw}. Fig. 1(b) shows the small signal equivalent circuit of the switching and corresponding coupling transistors [3]. From Fig. 1(b), the coupling strength α between the two VCOs of the P-QVCO can be defined as [2]

$$\alpha = \frac{g_{cpl}}{g_{sw}} = \frac{W_{cpl}}{W_{sw}} \tag{1}$$

Manuscript received November 1, 2006; revised November 14, 2006. This work was supported by the IT R&D Project funded by the Korean Ministry of Information and Communications.

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Digital Object Identifier 10.1109/LMWC.2007.892988

where g_{cpl} and W_{cpl} are the transconductance and width of the coupling transistor, and g_{sw} and W_{sw} the transconductance and width of the switching transistor, respectively. In P-QVCO, the coupling strength α has a strong effect on phase noise and phase error which defines the phase difference from 90° between I and Q signals. For example, the increase in α degrades the phase noise significantly while the phase error is reduced, or vice versa [2]. The phase noise degradation is induced by the increase in transconductance of the coupling transistors. In addition, the increase in α leads to a higher amount of power dissipation.

Fig. 2(a) shows the circuit schematic of the proposed backgate-coupled QVCO. In Fig. 2(a), each pair of series connected N- and P-MOS transistors (M1–M3 and M2–M4) with LC-tanks constitutes the current-reused differential VCO [4]. $R_{s,n}$ and $R_{s,p}$ are adopted as current sources which also function as degeneration for the switching transistors [5]. In Fig. 2(a), the two VCOs are coupled through the backgate of the switching transistors [3].

In the proposed QVCO, the current-reused VCO dissipates half the amount of power of the conventional differential VCO [4]. In addition, since quadrature coupling is achieved through the backgate, no additional power dissipation is required for the coupling compared to the case of P-QVCO. Therefore, the proposed QVCO resolves the power dissipation issue which is the key deficiency of the conventional P-QVCO.

As mentioned above, the P-QVCO has trade-off between phase noise and phase error. The reduction in phase error warrants higher power dissipation as well. However, in the proposed QVCO, phase error can be reduced without sacrificing phase noise as the coupling involves no additional transistors.

Fig. 2(b) represents the equivalent circuit of the backgate coupled transistor with the resistor R_s as a current source. From Fig. 2(b), the coupling strength α_B through the backgate can be given by

$$\alpha_B = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2\Phi_F - V_{BS}}} \tag{2}$$

where γ, Φ_F, and V_{BS} are the body-effect coefficient, work function, and backgate (body) to source bias voltage, respectively. From (2), it can be seen that the coupling strength α_B is a function of V_{BS}. Therefore, the body-to-source reverse bias should be minimized (that is, enough to prevent from being forward biased by the coupling signals) in order to increase α_B, which leads to phase error reduction.

In Fig. 2(a), small signal wise, the resistors $R_{s,n}$ and $R_{s,p}$ function as current sources. However, during the large signal switching operation, these resistors effectively provide degeneration to the switching transistors. This degeneration not only

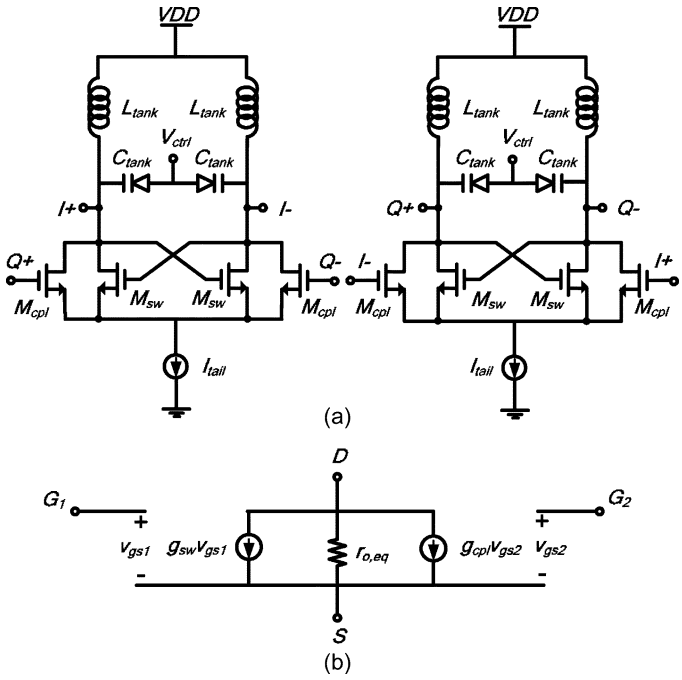

Fig. 1. (a) Conventional parallel QVCO topology and (b) small signal equivalent circuit of the switching- and parallel-coupling transistors.

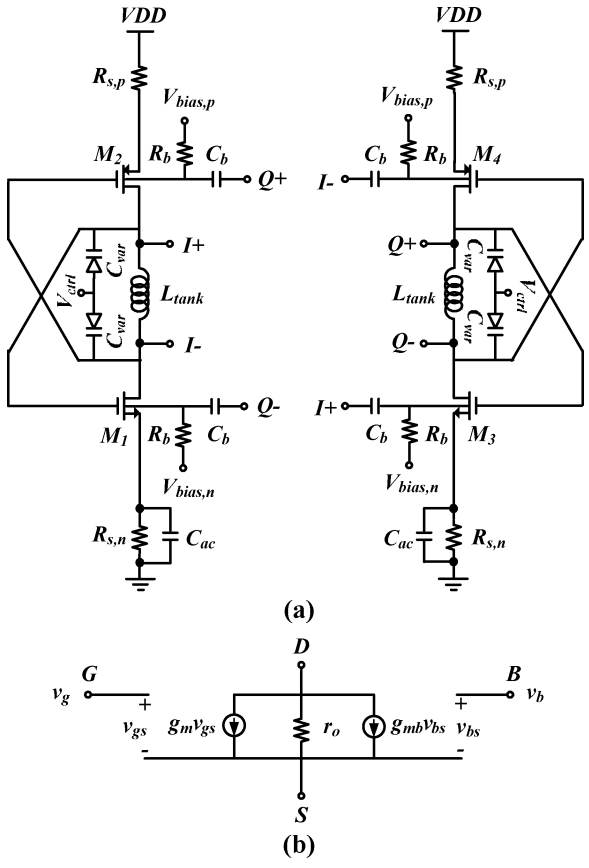

Fig. 2. (a) Proposed backgate coupled QVCO and (b) small signal equivalent circuit of the backgate-coupling transistor.

reduces but limits the transconductance of the switching transistors during the large signal operation. The reduction of the transconductance leads to the reduction of the $1/f^3$ corner of the phase noise spectrum [5].

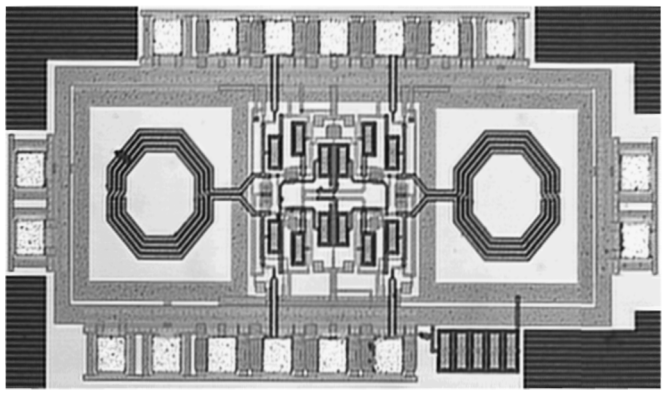

Fig. 3. Chip microphotograph of the proposed QVCO (1500 × 700 μm°).

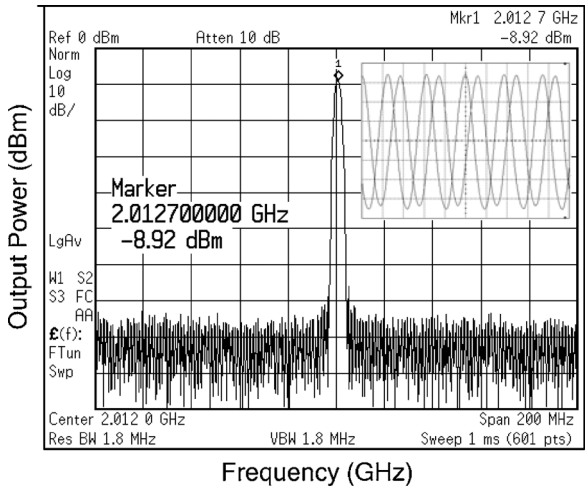

Fig. 4. Measured output spectrum and voltage swing of the proposed QVCO.

III. QVCO Design and Measurement Results

In Fig. 2(a), the topology consists of cross-connected pair transistors $M_1 \sim M_4$, inductors $L_{\rm tank}$, and varactors $C_{\rm var}$. The resistors R_b are adopted for dc biasing of the backgate and the capacitors C_b for ac coupling. For a fully differential output swing, size of the cross-connected N- and P-MOS transistors M_1, M_3 and M_2, M_4 are carefully selected to generate the same transconductance in LC-tank, respectively. In addition, since characteristic of the backgate in N- and P-MOS transistors is different, dc voltage $V_{\rm bias,p}$ and $V_{\rm bias,n}$ of the backgate in Fig. 2(a) are also cautiously biased to provide the same coupling strength. The large capacitor $C_{\rm ac}$ attenuates the high frequency thermal noise of the source degeneration resistors. As a design optimization, the value of R_s should reflect the symmetry issue as well. The properly ratioed values of the degeneration resistors $R_{s,n}$ and $R_{s,p}$ can provide additional phase noise reduction as they help to improve the symmetry of the impedances looking into the P- and N-MOS transistors [5].

The proposed QVCO shown in Fig. 2(a) is implemented in a 0.18-μm CMOS process. Fig. 3 shows a fabricated chip microphotograph with size of 1500 × 700 μm^2 including the pads. For measurement, open drain output buffers are used in the QVCO. The QVCO dissipates a total current of 1.74 mA from a 1.25-V supply. The measured frequency oscillation covers from 1.83 to 2.02 GHz with control voltage 0 and 1.2-V. Fig. 4

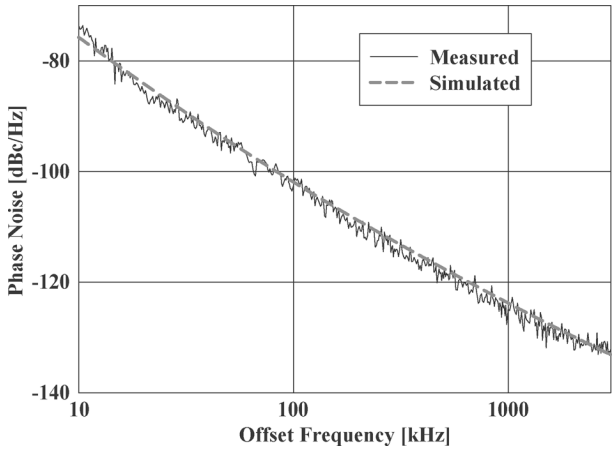

Fig. 5. Measured and simulated phase noise of the proposed QVCO.

TABLE I
PERFORMANCE COMPARISON OF LOW POWER QVCOS

QVCO	Power [mW]	Tech. [μm]	Freq. [GHz]	Phase Noise [dBc/Hz]	FOM [dBc/Hz]
[3]	5.4	0.18	1.1	-120@1MHz	-173.5
[6]	8.6	0.18	2	-127@1MHz	-183.6
[7]	7.2	0.18	2.45	-119@1MHz	-178.0
[8]	6.8	0.18	6	-106@1MHz	-173.2
[9]	6.0	0.7	1.8	-116@600kHz	-177.8
This work	2.2	0.18	2.01	-124@1MHz	-186.7

shows the measured output spectrum and transient output waveform when the QVCO oscillates at 2.013 GHz with 1.2-V tuning voltage. The amplitude and phase error are 0.2 dB and 5°, respectively.

The phase noise performance of implemented QVCO is measured using 4352B VCO/PLL signal analyzer. Fig. 5 shows the measured phase noise of the proposed QVCO in comparison with the simulation. The measurement results match well with the simulation and show good $1/f^3$ close-in phase noise. In Fig. 5, the measured phase noise are -102 and -124 dBc/Hz at 100 kHz and 1-MHz offset frequency, respectively.

Table I summarizes the performances of the proposed QVCO compared to those of previously reported low power QVCOs [6]–[9]. The proposed QVCO demonstrates excellent performance as a low power QVCO with a figure-of-merit of -186.7 dBc/Hz.

IV. CONCLUSION

A backgate coupled QVCO that adopts current-reused LC–VCOs is presented. This work describes the phase error dependence on the body-to-source bias voltage of the switching transistors. The proposed QVCO consumes only half the amount of power and shows better phase noise performance compared to the conventional P-QVCO. The proposed QVCO is designed for 2-GHz operation based on a 0.18-μm triple-well CMOS technology. Measurements show -102 and -124 dBc/Hz at 100-kHz and 1-MHz offset, respectively, while dissipating a total current of 1.74 mA from a 1.25-V supply.

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